Alternative technologies for interlocking: HIMA hardwired

Tomasz LADZINSKI

Questions and Answers:

1- Cost compared to a PLC? 15K€ current rack with 14 cards.
2- Future plans? Small project, requested from operations, implementation was fast. The use in the SPS access system is a candidate, but shall be analysed.
3- Response time? 60 ms, from detection from actuation (only HIMA planar 4)
4- How feasible can be a system with 7 to 8 thousand of I/Os? Is the technology selected for nuclear safety system at ITER, and the current number of input/outputs are in these figures… we do not observe such size for a project using this technology at CERN.
5- PLC vs HIMA? How to apply the diversity? Previously we used relays. This is a good starting project to compare, but is early to compare. At the moment is working properly.
6- Response time? It is highly dependent on the number or modules that are involved in your functionality. Each card requires 5~10 ms, so the more complex the slower. 10 ms is the response time for the AND card, which is the slowest.

Development of redundant and reliable Fast Interlock Controllers using COTS based on IEC 61508

Luis FERNANDEZ HERNANDO

Questions and Answers:

1- How the input or the output diagnostics are performed? The input/outputs diagnostics are generated in the operation cycle. Two behaviours can be configured before compiling. If there is a problem it can be defined a failsafe state (de-activation of the outputs) or an alarm can be raised alarm, continue the operation in degraded mode.
2- How often do you run the diagnostics? Once per cycle. Before the functionality is achieved the inputs, outputs and the information from the other chassis is evaluated. The inter-chassis communication, for diagnostics, takes 12 us.
3- How do you analyse the SFF? The behaviour of the components has been already analysed to calculate the reliability figures. The calculation can be provided if demanded.
4- How the reliability requirements are defined? They come from the project requirements, they has been already redefined to be applied to the interlock system.
5- How do you define the Fail-safe status? The fail-safe is defined as “false” so the systems are designed in a way that the deactivation of the outputs means “stop”.

Fast beam interlock system for machine protection at ESS

Angel MARTINEZ MONERA et al.

Questions and Answers:

1- How the slow and fast response times requirements are managed within the architecture? They are implemented in different systems.
2- The functionality is achieved by COTS or tailor made equipment? Tailor made for the project
3- Do you use embedded IOCs in the FPGA, as it is considered for the conventional systems? The cost of the solution can be reduced if similar approaches are considered…
   Not in this case, but there will be an analysis. The interlocks are managed independently from the conventional. The drivers will be shared, so the cost of development will be reduced. The solution will be based in uTCA architecture. One option under analysis, for the implementation, is to take the original schematics of the conventional control cards and, removing the FPGA, use the CPU as the interface to the EPICs IOCs.
   Additionally, the CPU and the FPGA are running in sequence, we are trying to parallelize to improve the performance and the reliability of the application.

High Performance Computing platform for predictive interlocks using PLCs at ESS

Manuel ZAERA SANZ

Questions and Answers:

1- How you already measure the performance? The network topology is a critical for performance. The main advantage is that all the addressing of the shared memory is made by the operating system of the PLC, so is transparent. The i-devices are working reliably in many industrial applications. The main problem for i-devices is the limitation of 1kb, despite you can define as many i-devices as you want. There is additional limitation on the number of processors linked to an i-devices is up to 4.
2- The concept of predictive interlock is not “traditional”, as the validation of the functionality requires to be activated within a defined behaviour.
   The approach is to have a parallel computation, in fact the current platform only use the standard part of the program.
3- How do you synchronize the conventional/interlock systems with the predictive approach? The general idea is that the predictive interlock will have more priority in some actions, and the analysis shall be performed in order to analysis case by case.
4- How this predictive interlock will be different of a model of a system? The implementation will be quite complicated, as this model needs to be implemented in a distributed control system.
   The cluster of PLCs platform, using neural networks can improve the interlock capacity of the interlock system.
5- Predictive interlock stopping the beam, via the beam interlock, in case of a future event that has not even happen? (It will be excessive)
   The prediction can be wrong, but we don’t want to avoid the interlocks.
6- Prediction and neural networks? How you considered other techniques? The PLC finally is a computer, so any technique can be tried. Other technique that can be explored is the Bayesian networks.