DE LA RECHERCHE À L'INDUSTRIE

cea

CMOS PIXELS SENSORS ACTIVITIES AT IRFU

FCC-Saclay meeting

F. Orsini

26th November 2015

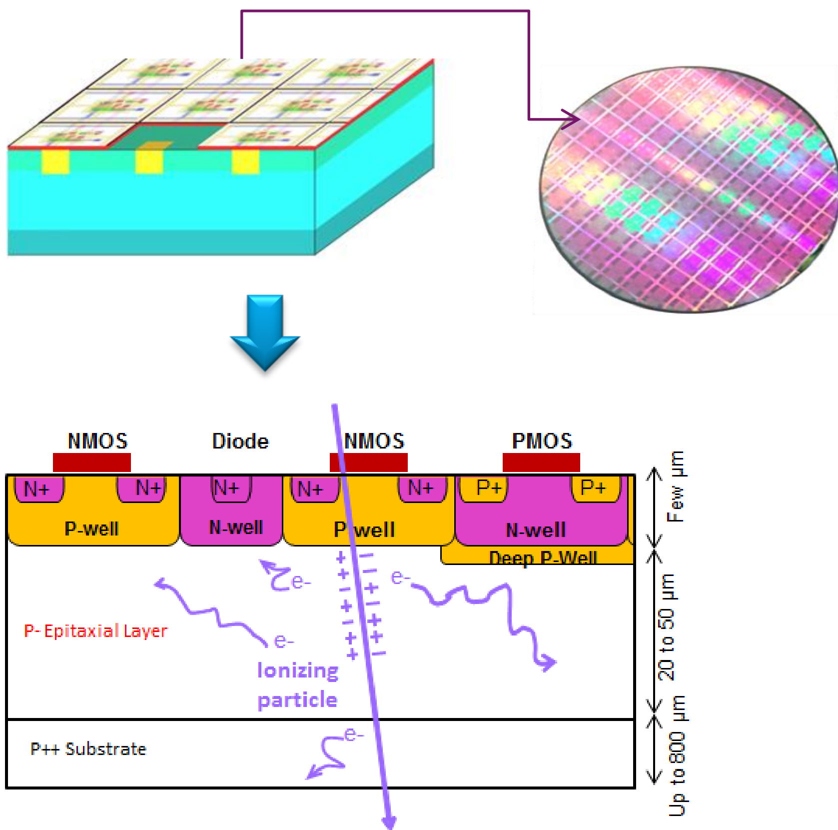
Irfu

MAPS DEFINITION AND DETECTION PRINCIPLE

MAPS = Monolithic Active Pixels Sensor

Solid detector in Silicon

Sensible volume (detection part) + signal processing circuit share same substrate, using standard CMOS electronic components = ‘CMOS Monolithic’

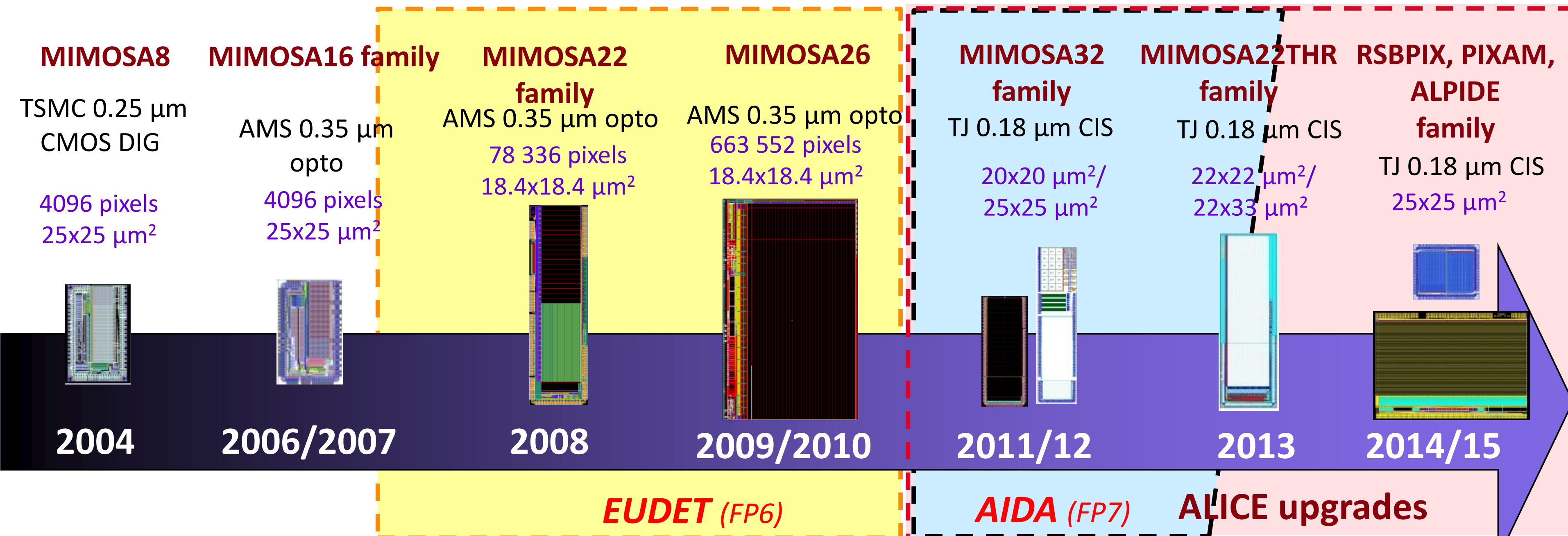


Main advantages

- ❑ High Granularity
- ❑ Monolithic and ultra-thin
- ❑ Low noise, low power
- ❑ Work at ambient temperature
- ❑ Low cost (CMOS process)

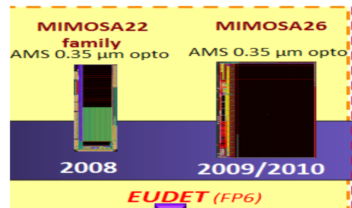
HISTORIC – CMOS MONOLITHIC PIXELS SENSORS DEVELOPMENT AT IRFU

- Since ~2002 IRFU has launched a R&D program on CMOS MAPS technology starting in the framework of the ILC project (vertex detector)
- Y. Degerli (SEDI) has designed the first digital MAPS (MIMOSA 8) jointly with IPHC
- ~20 MAPS with digital outputs have been designed, realized and tested in the past 10 years (from small prototypes to large sensors) in collaboration with IPHC for ILC VX, EUDET (FP6), AIDA (FP7) and recently for ALICE-upgrade projects (MAPS design effort driven by CERN consortium)
- It has demonstrated the validity, maturity and the excellent performances of this detection technology for charged particles tracking

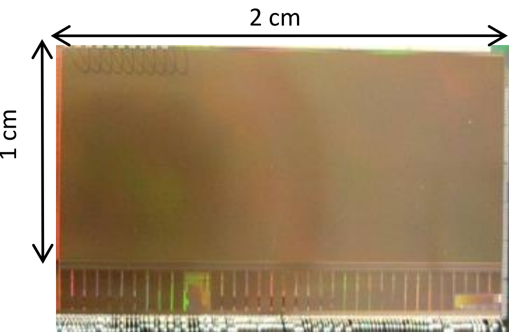


EUDET BEAM TELESCOPE

FP6

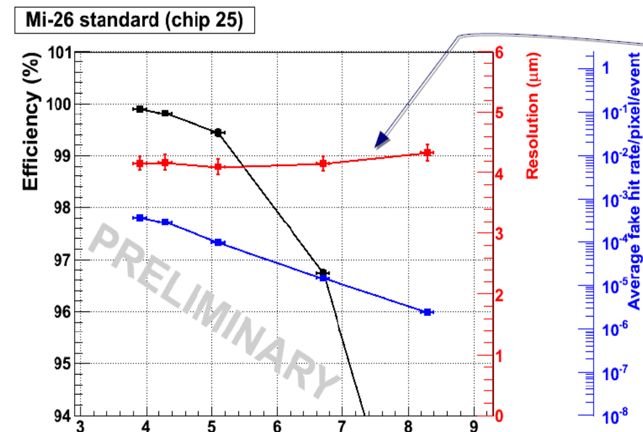


Technology: *AMS 350 nm (opto)*
Designed by IPHC-IRFU (Y. Degerli for IRFU)



MIMOSA 26
663 552 pixels – pitch = 18.4 µm

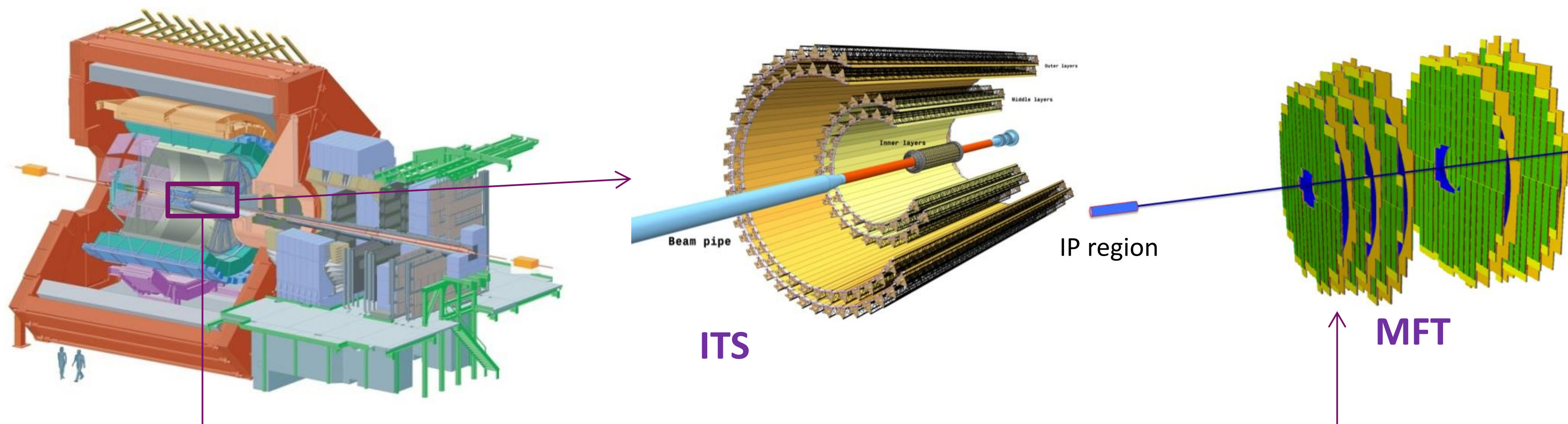
EUDET (JRA1) Beam Telescope
6 planes composed of MIMOSA26 sensors



- Large size Digital MAPS integrated for the first time in a physics experiment (MIP tracking)
  → work with success → few copies of the telescope around the world (DESY, CERN, US)
- Performances achieved:
  - Integration/readout time: 115 µs (per frame)
  - Detection efficiency > 99.5%
  - Spatial resolution (digital output): 4 µm
  - Rad tolerance: Dose of 500 kRad and neutron fluence of ~1.10^{13} n_{eq}/cm^2

➡ AIDA, ALICE upgrades

CMOS MONOLITHIC PIXELS SENSOR FOR ALICE UPGRADE: ITS & MUON FORWARD TRACKER



ITS upgrade:

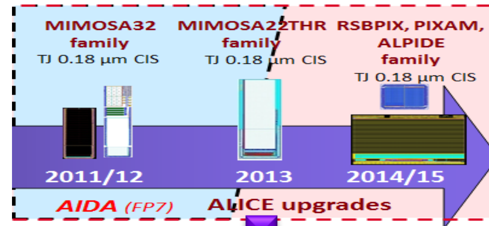
- 7-layers barrel geometry based on MAPS (~25 000 sensors ~10 m^2)
- η coverage: $|\eta| \leq 1.22$

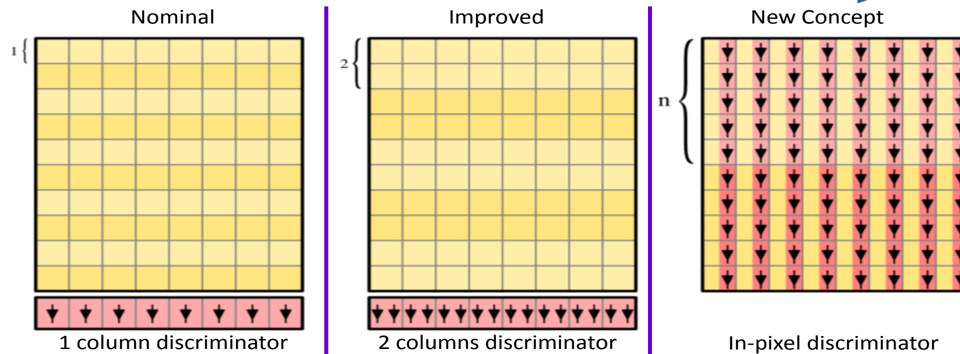
Muon Forward Tracker: vertexing for the ALICE Muon Spectrometer at forward rapidity

- 5-planes geometry based on MAPS (~900 sensors, ~0.5m^2)
- η coverage: $-3.6 < \eta < -2.45$

Parameter	Value
Spatial Resolution	~ 5 μm
Detection Efficiency	> 99.5%
Integration Time	< 20 μs
Sensor Thickness	50 μm
Power dissipation	< 150 mW/cm²
Radiation Tolerance (10-years operation)	~ O(10^{13}) n_{eq}/cm^2 ~ O(800) kRad

MAPS DEVELOPMENT FOR ALICE MFT



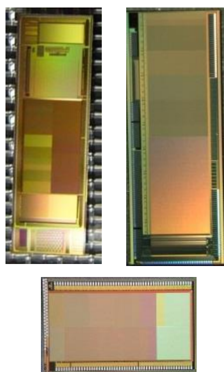


Techno choice

Tower Jazz 180 nm

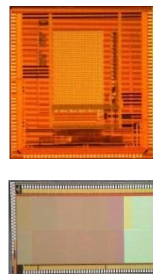
High Resistivity epi-layer (> 1 kΩ.cm)

M32, M32Ter, M32v4
M22THRA2



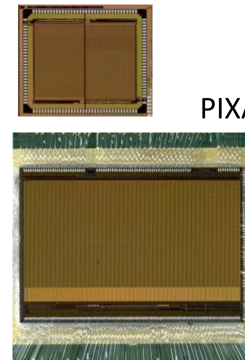
Digital outputs
Medium size proto.
1 discri. / column
RO speed X1

M32v4 (analog part)
M22THRB2



Digital outputs
Small size proto.
2 discri. / column
RO speed X2

M32v4 (analog part)
RSBPIX1, RSBPIX2



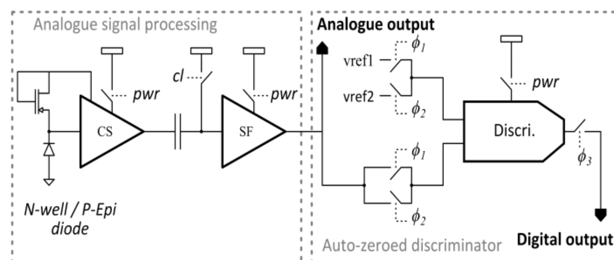
PIXAM

Digital outputs
Small and large size proto.
1 discri. / pixel
RO speed X2

PIXAM (FSBB prototype) *for the ALICE - Muon Forward Tracker*

- 1/3 of final matrix (10 mm × 7 mm)
- 2 lines readout simultaneously
  - **Readout time nominal : 15.36 µs**
  - Evaluation for readout : 10 µs
- Rolling Shutter Binary Pixel architecture
  - **25 µm pitch**
  - **In each pixel: amplification, CDS, discriminator with continuous offset compensation**
- **Zero suppression logic**
  - **Cluster 3x3 pixels**
  - 7 clusters / row/ FSBB
- Digital Outputs
  - Compatible with Pxi DAQ

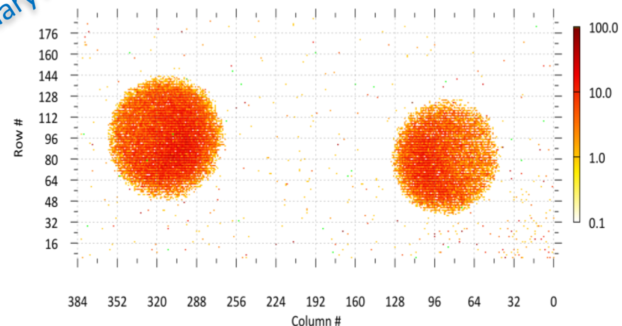
Tower Jazz 0.18 µm CIS technology



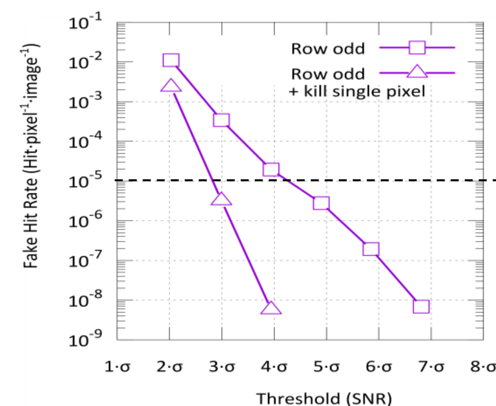
Submitted in May 2014

Tests in-lab Preliminary results

With Fe^{55} source



Fake Hit Rate



Power Dissipation (estimation)

- Analog: 105 mW/cm² (not optimized)
- Digital: 45 mW/cm²

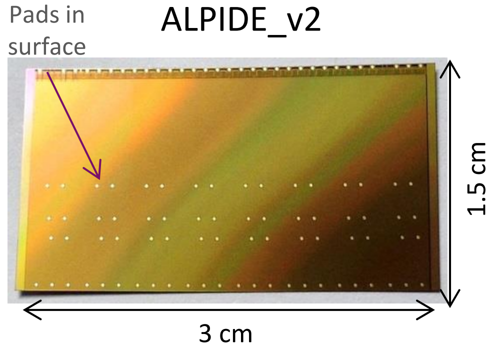
Y. Degerli, C. Flouzat, F. Guilloux

MAPS DEVELOPMENT FOR ALICE MFT

L. Musa (ITS-CERN) – June 2015

Pads in surface

ALPIDE_v2

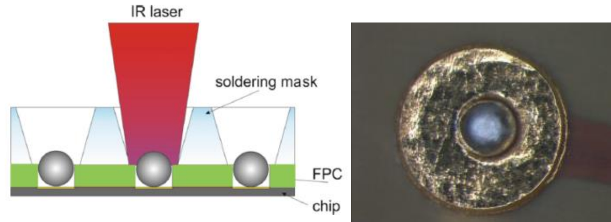


3 cm

1.5 cm

Readout time = 4 µs

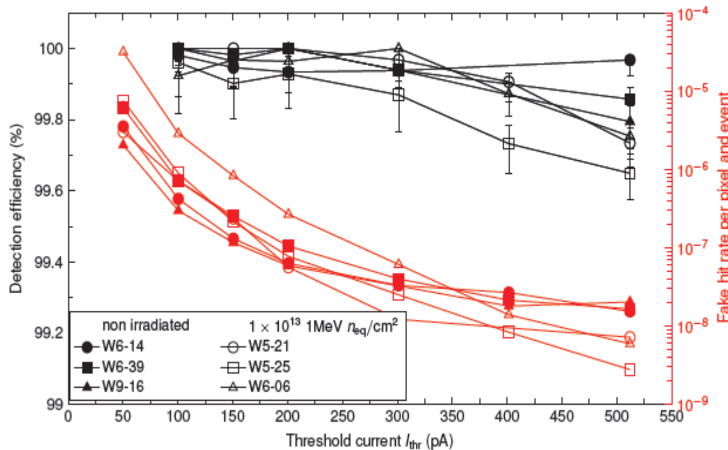
Interconnection of CMOS sensor to Flex PCB by laser soldering technique

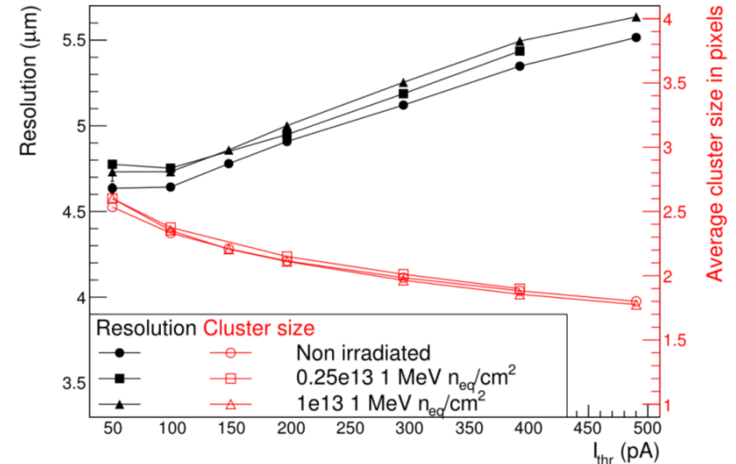


MFT Ladder prototype with fake sensors

⇨High resistivity (> 1kΩ cm), p-type epitaxial layer (20 µm – 40 µm thick) on p-type substrate

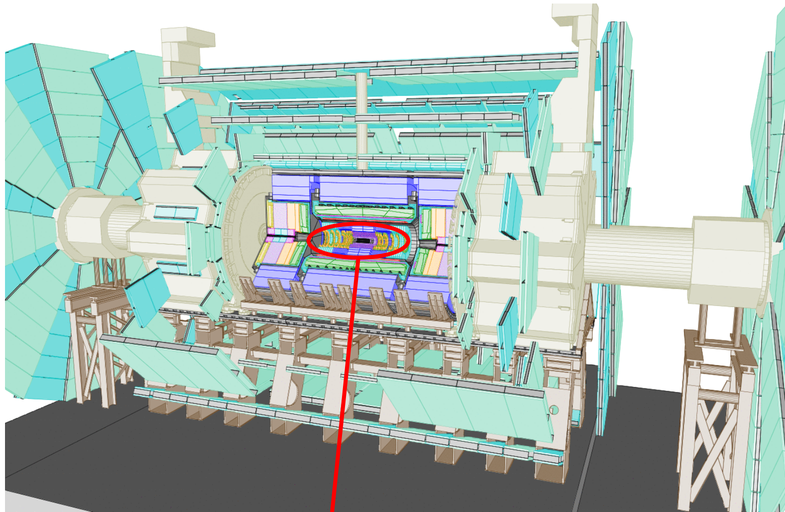
Example of measurement at PS (5 – 7 GeV π-) test beam with pALPIDEfs_v1 (Dec 2014/March 2015)

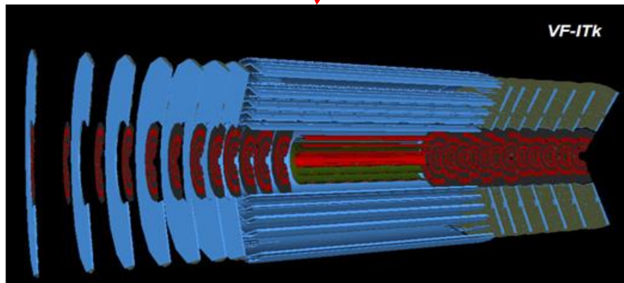




with 50 µm thick chips: non irradiated and irradiated with neutrons (0.25x10^{13} and 1x10^{13} 1MeV n_{eq} / cm^2)

ATLAS PHASE II INNER TRACKER





Challenges for phase II

- Radiation hardness
- Readout time (high rates)

	ATLAS-LHC	ATLAS-HL-LHC
Bunch crossing [ns]	**25**	**25**
Particles rate [kHz/mm^2]	1000	10000
Neutrons flux [n_{eq}/cm^2]	**2x10^{15}**	**2x10^{16}**
Dose (ionizing part) [MRad]	**80**	**>500**

Inner barrel

- High resistivity wafer
- Application of high voltage → complete depletion of bulk possible

\+

- Material budget improvement
- Thinner granularity
- Cost improvement

=

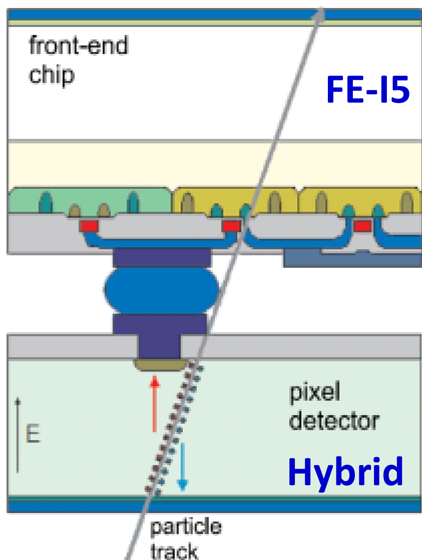
HV/HR CMOS Pixels

ATLAS PHASE II INNER TRACKER: CANDIDATES

Present = hybrid pixels for inner layers and strips for outer layers → to be replaced

BASELINE

'Standard' Hybrid Pixels + FE-I5

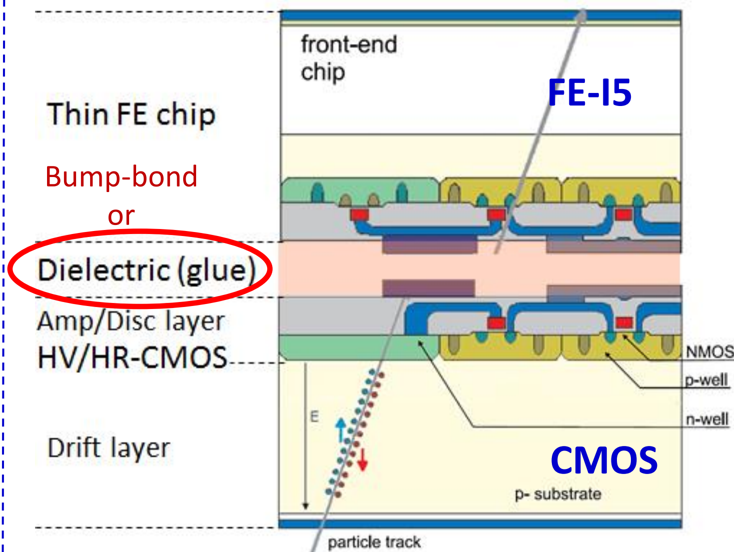


- Rad hardness
- Fast readout
- Thick, Low granularity
- High Cost
- QA pb for large prod

CONCURRENCE

[Middle-Outer layers]

HV-(HR)CMOS + FE-I5

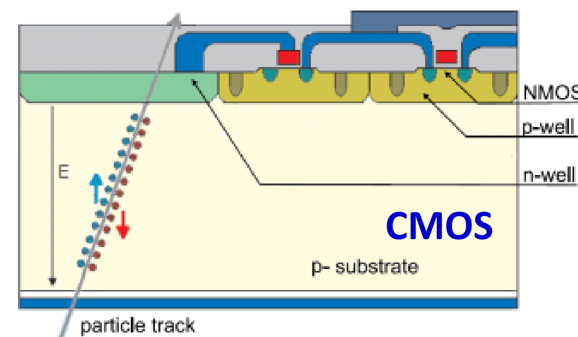


- More granular
- Less expensive (cheaper bonding process)
- Thinner
- Low power, low noise
- Rad hardness

OUTSIDER

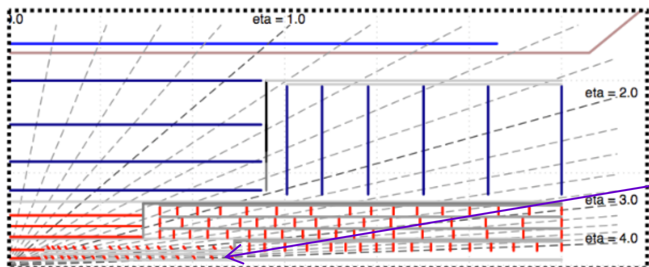
[Middle-Outer layers]

HV-(HR)MAPS (full monolithic)

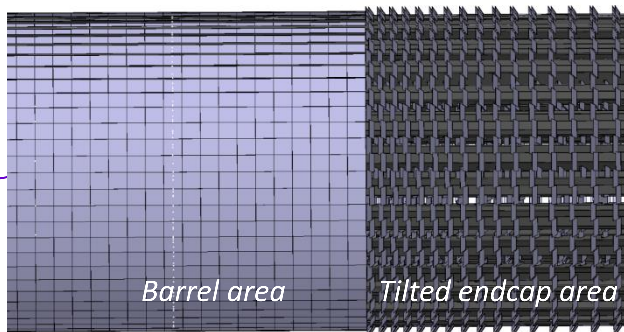


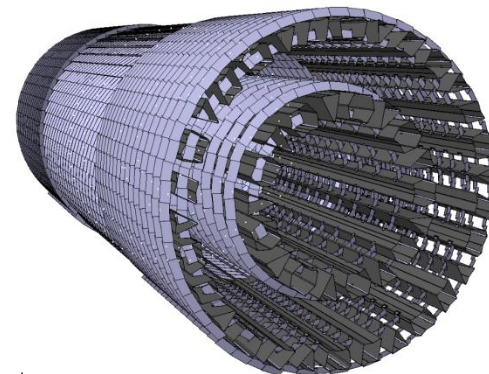
- Highest granularity
- Thinnest (material budget ↘)
- Lower cost (intelligent detector)
- Low power, low noise
- Rad hardness, fast readout

PARTICIPATION OF IRFU TO ATLAS ITK R&D EFFORT



ITK possible layout: Inclined@4.0

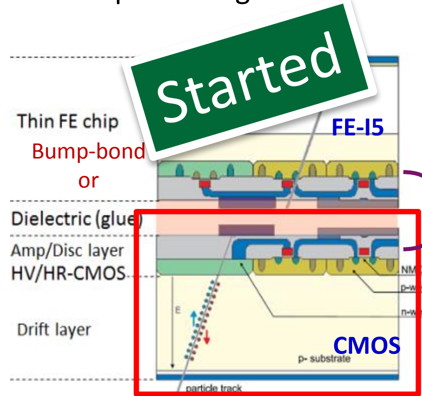




SLIM concept

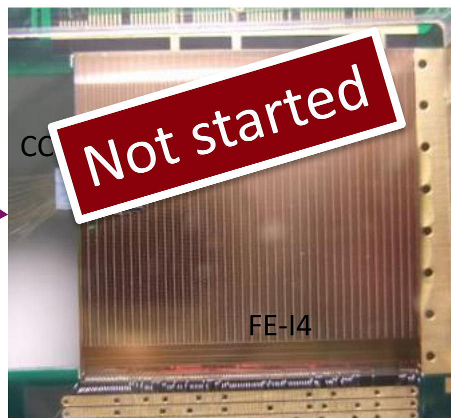
1 HVCMOS pixels sensor design

Design and validation of HVCMOS pixels sensors concept
(incl. 1rst amplifier stage + add circuits)



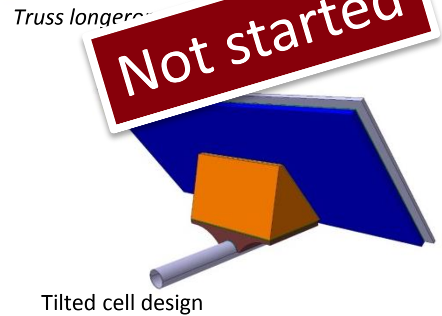
2 Interconnection studies

Readout via ATLAS pixel chip FE-I4 capacitively coupled



3 Thermomechanical studies

Truss longeron



Tilted cell design

HVCMOS PROTOTYPES SUBMITTED (FEW MM2)

S. Rozanov – CPPM

	A	B	C	D	E	F	G	H	I
Node	180nm	350nm	150 nm	180nm SOI	180nm	130nm	150nm	130nm	160nm
Wafer Resistivity	10 ohm	10 ohm 1 khom availab	2 kohm	100 ohm 2k poss.	1-3 k Epi/bulk	3k	2k	10 ohm 3k ???	Select epi
Full CMOS	No	No	Yes	yes	Yes	No	Yes	Yes	Yes
Backside implant	No	No	Yes	No	No	No	Yes	No	No
HEP experience	4 subm Lab Test beam	2 subm Labor Also strips Demo 11/2015	2 subm Lab	Subm Lab	Subm Lab	Subm 6/2014	Receiv 2/2015 Demo 12/2015	Receiv Lab	tbd
Groups	Heidelb Geneva CPPM Bonn CERN	Karlsruh. Geneva	Bonn Prag.	Bonn CERN	Bonn (Strasb)	Bonn	Bonn, Heidel. CPPM, IRFU CERN, SLAC	CPPM Heidel.	INFN

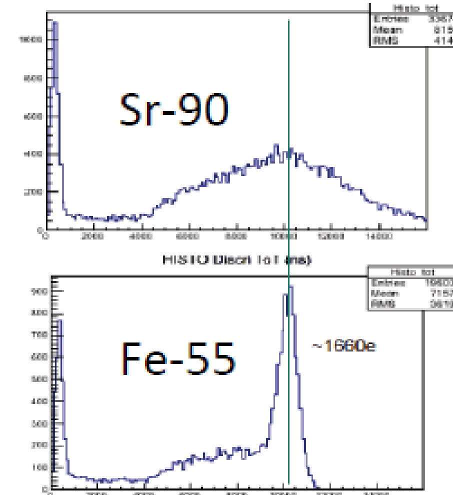
RESULTS OBTAINED WITH CCPDV4 PROTO

AMS 180 nm (bonded to FE-I4)

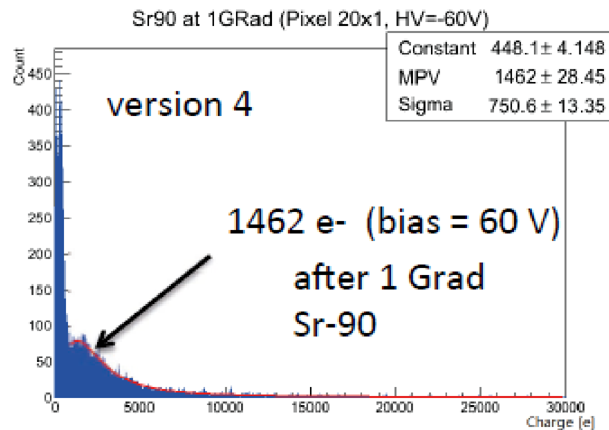
universitätbonn

some encouraging results

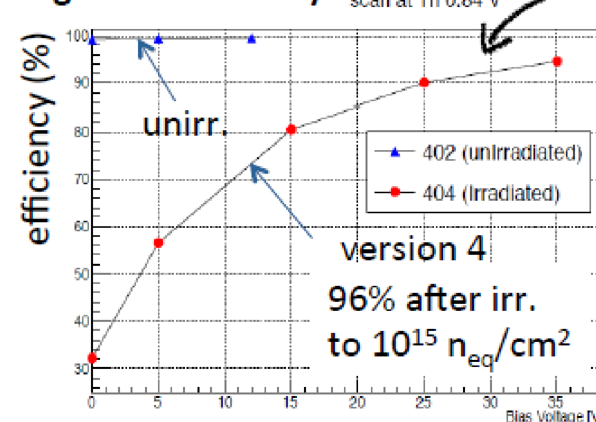
- **capacitive coupling** seems to work in principle, whether it is competitive in terms of reliability and price is unclear
- chips stand **TIDs up to 1 Grad**
- proton irradiation 10^{15} n_{eq}/cm^2 performed
- efficiency (time integrated): 99% -> **96%**
- **in-time efficiency** not yet met (τ_{rise}~100 ns)
- signal ~1500 e ; SNR ~ 25
- characterizations w/o FE-I4 ongoing



version 2 **before** irradiation



time integrated efficiency



Need to reach the plateau

N. Wermes, Elba_2015

HVCMOS SENSORS DESIGN & PERFORMANCES CHARACTERIZATION ACTIVITIES

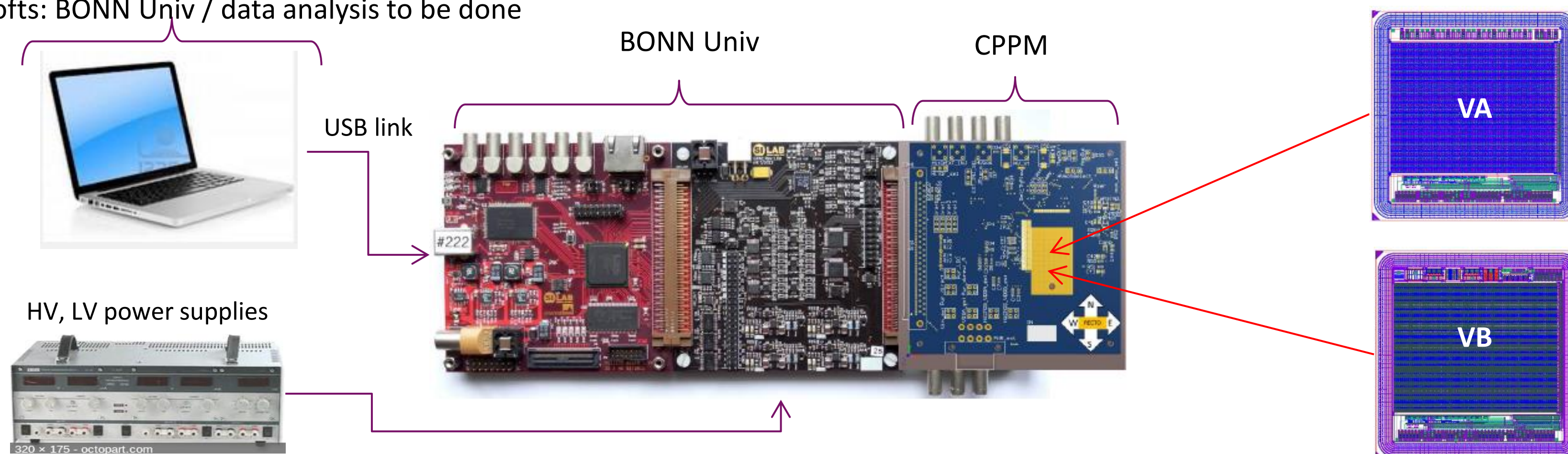
Current Team (2015)

- Microelectronic Design, techno process:
  Yavuz Degerli (+ punctual help from F. Guilloux and F. Bouyjou)
- Project coordination, techno process, protos performance tests:
  Fabienne Orsini
- ATLAS physicists:
  Claude Guyot, Philippe Schwemling
- PhD student:
  Mohamed Lachkar (since October 2015; design, tests and TCAD simulations)

HVCMOS Activities

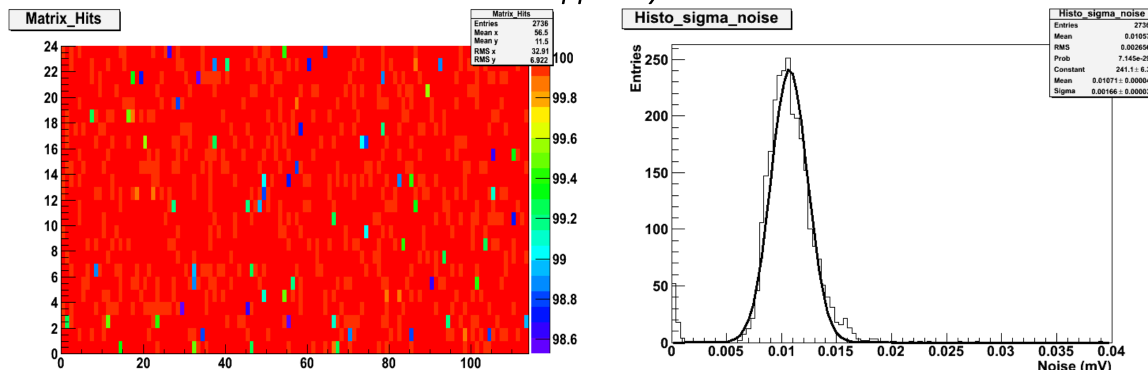
- Started with the GF 130 nm process in collaboration with CPPM, and then switched to the LF 150 nm process with CPPM and Bonn
- Participation to the tests of CCPD_LF prototypes (*just started…*)
- Currently, active participation to the design of a demonstrator in LF 150nm HV techno process
- Participation to H2020 project (start in June 2015):
  AIDA2020 *WP6 "Novel high voltage and resistive CMOS sensors"*

CCPD_LF PROTOTYPES PERFORMANCES CHARACTERIZATION TESTS



Very first scan tests to check testbench assembly and softs functioning at IRFU

No HV applied yet



LF 150 nm HV technology

- Chip size: 5 mm × 5 mm
- Matrix: 24 × 114 pixels
- Pixel size: 33 µm × 125 µm
- VA: negative HV applied on P-substrate
- VB: positive HV applied to DNWell

Objectives:

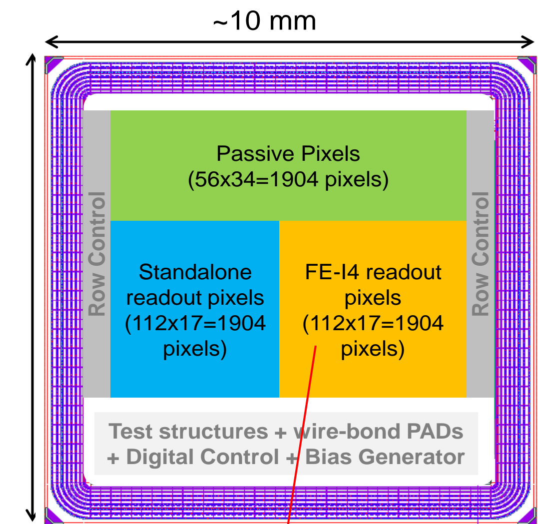
- Participate and provide to the collaboration tests results of the different CCPD_LF prototypes config.
- Better understanding of the chip architecture (strengths, weaknesses)

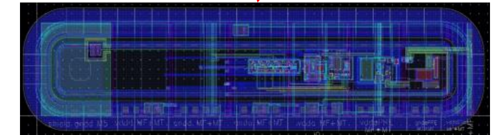
DESIGN OF LFCPIX DEMONSTRATOR

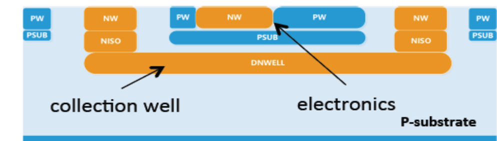
Demonstrator Process: **LFoundry 150nm HVCMOS**

Bonn, CPPM, IRFU collaboration

- ❑ Based on experience with 2 previous CCPD_LF prototypes designed by Bonn&CPPM in 2014
- ❑ Passive, Standalone digital and analog/digital output pixels (FE-I4 readable)
- ❑ A more performant pre-amplifier is proposed by IRFU
- ❑ Pixel properties:
  - Pitch: **250µm x 50µm**
  - Peaking time: **~20 ns**
  - Power dissipation: **~20 µW** (analog)
- ❑ Re-use of already validated peripheral circuits
- ❑ Close to being completed, submission planned in Dec. 2015







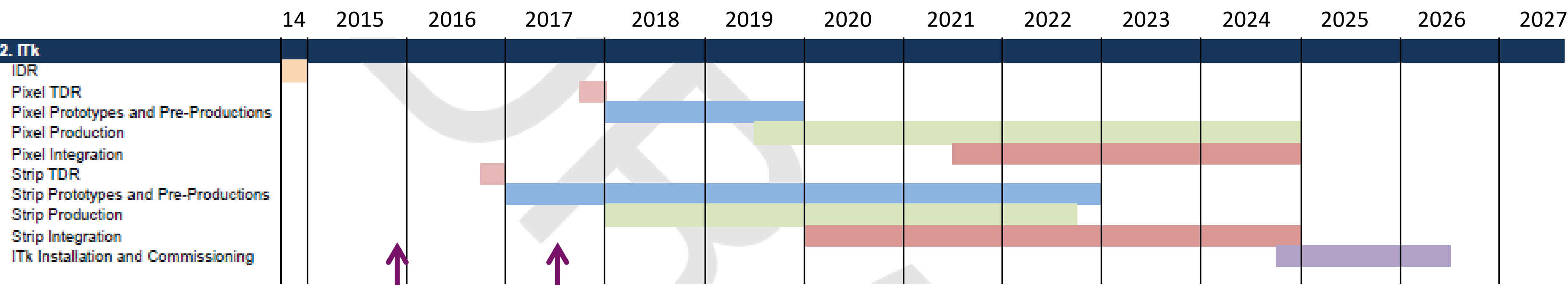
Digital pixel layout

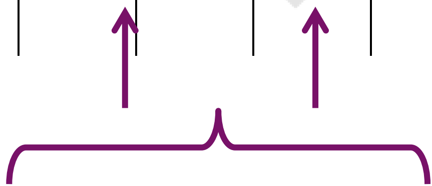
Objectives:

- Demonstrate the performances of HVCMOS chips to expected ITK irradiations level
- Be ready for pixels techno choice in 2017 and for Pixels-TDR in Q4 2017

ITK PIXELS SCHEDULE

Time-line of ITK upgrade project





HVCMOS main tasks

- Demonstrator back from foundry (5 m) — May 2016
- Post processing of circuits (1 m) — June 2016
- Demonstrator performances validation (4 m) — Oct 2016
- 2nd demonstrator submission — Dec 2016
- ….
- Preparation of pixels TDR — June 2017
- Pixels TDR submission — Q4 2017

Choice for techno

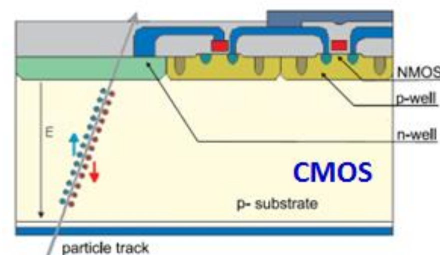
OTHER POSSIBLE PARTICIPATION IN MICRO-ELECT ACTIVITIES FOR ATLAS ITK (PROPOSAL)

❑ Participation to the design of a HVMAPS demonstrator (full-monolithic)

A full-monolithic version is already under study by some other research institutes (BONN, SLAC, KIT)

Few technologies under evaluation

- Option under discussion for ATLAS ITK external layers
- Very attractive for other experiments (@FCC) and other application (medical imaging)



❑ Participation to R&D effort on FE-I5 chip design (through RD53 collaboration)

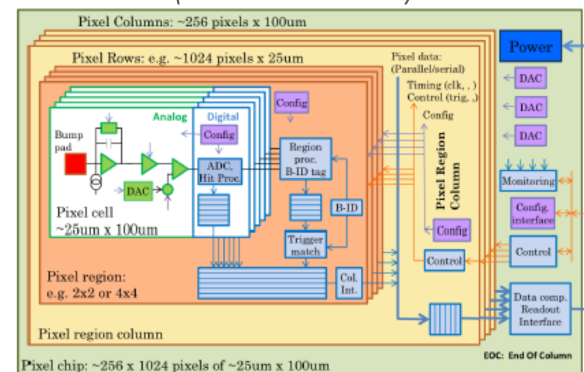
R&D program aims at developing Front End Elect ASIC for ATLAS and CMS through RD53 collaboration ⇨ FE-I5

Technology chosen: TSMC 65 nm

Back-up solution to consider in case of absence of HVCMOS (or HVMAPS) in the inner tracker

"Analog islands in digital sea"

(M. Garcia-Sciveres)



Pixel chip hierarchical organization

INTERCONNECTION STUDIES (PROPOSAL)

SEDI perimeter + SIS expertise

Capacitive coupling by glue is an innovative/recent concept

- ❑ Interconnecting process studies
  - Tools design, real. and tests with chips protos
  - Assembly Process
  - Material choice
- ❑ Develop and/or test some diagnostics to characterize glue quality layer
- ❑ Prototypes mech. characterization (ageing effect, fatigue effects,…)
- ❑ Reproducibility, yield
- ❑ Investigate options for future industrialization of the interconnection process

Example of glue deposition with pilars (G. Darbo-INFN Genoa)

Spin SU-8 photoresist
Pattern pillars by mask

R/O CHIP

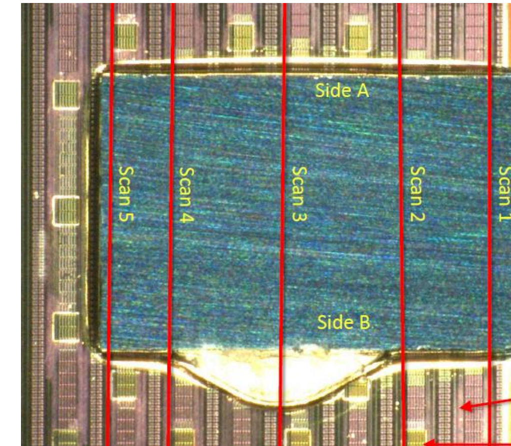
Glue deposition

R/O CHIP

Align & pressure

DETECTOR CHIP

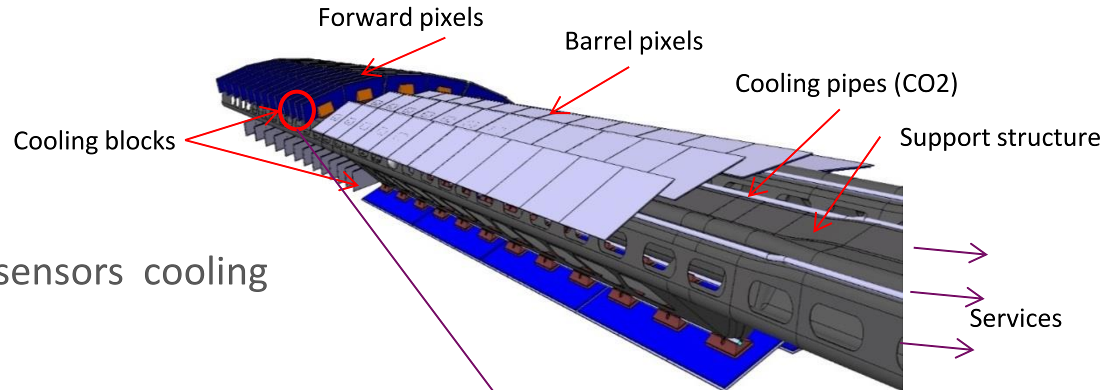
R/O CHIP



→ Participate right now to play a role for future participation in modules production

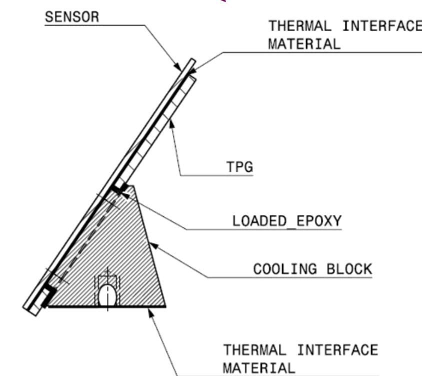
THERMOMECHANICAL STUDIES (PROPOSAL)

SIS perimeter



SLIM concept
(S. Michal's talk –UNI Geveve)

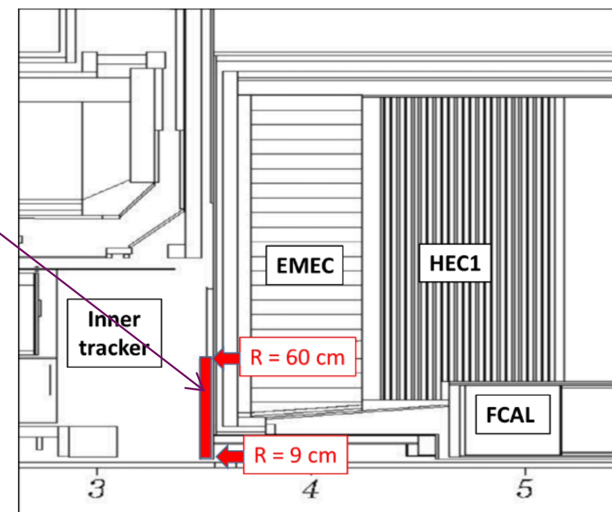
- Design studies of light material for sensors cooling blocks (thermal calculations)
- Thermal interfaces studies with prototypes realization
- New concept of cooling blocks deposit on support structure (test concept with 3D printer)
- Design study of outermost layers → interaction with physicists and follow ITK layout studies
- Routing and accurate assessment of services →regular interactions with collaboration



Tilted cell design

ATLAS HIGH GAIN TIMING DETECTOR

New detector to cope against pile-up effect in forward region



Main constraints:

- Time resolution of a few tens of ps
- Granularity better than 1 mm
- Important radiation levels comparable to first layers of ITK

2 options are considered at IRFU:

- Si pixels (HVCMOS) → new approach ≠ HVCMOS dev. for ITK
- Gaseous detector (Micromegas)

Technology options: intermediate milestones (F. Lanni)

- Oct 2015 - Sep 2016: R&D on sensors – prototypes
- Jul 2016 - Mar 2017: Test-beams and validation
- Mar 2017: Decision baseline technology [ATLAS]

SUMMARY

- MAPS technology is nowadays sufficiently valid and mature for large physics experiments and has demonstrated excellent performances for charged particles tracking

- Strong experience in standard monolithic CMOS pixels sensors design/validation at IRFU
  - Regular Partner in European projects: FP6 (EUDET), FP7 (AIDA), H2020 (AIDA2020)
  - Active participation in large collaboration: (ILC), ALICE upgrade (close work with CERN micro-elect design team)

- New challenge for IRFU group for ATLAS Phase 2 ITK project → HVCMOS/HVMAPS
  - R&D effort started beginning of 2015 for pixels sensor design
  - Good relationship with collaborators (BONN, CPPM, …)
  - Excellent perspectives in case of success for ATLAS ITK but not only (FCC, other)
  - Strong support of IRFU hierarchy to this activity is mandatory to suceed

DE LA RECHERCHE À L'INDUSTRIE

cea

Thank you for your attention

USE CASES FOR CMOS PIXELS IN ITK 2024

S. Rozanov – CPPM

- **Inner pixel** layers (R=3-6 cm) → Use of FE-RD53 in 65nm technology with 50x50 µm pixel size. Four CMOS 25x25 µm sub-pixels with thickness <50 µm. Strong radiation hardness demand up to 1 GRads
- **Intermediate pixel** layers R=6-25 cm → Use of FE-RD53 with 50x50 µm pixel size. Four CMOS 25x25 µm sub-pixels with thickness <50 µm interesting, but not mandatory.
- **Outer pixel layers** R> 25 cm → Use FE-Ix digital tier with pixel 50x250 µm. Low cost bonding (gluing or C4 bumps) mandatory for cost reasons.
- **Outer pixel layers** R>25 cm → Use Full monolithic CMOS chip with classical column readout