

ADVEOS

Custom ICs for Radiation Detection & Imaging

April 2016

Overview

- Company Introduction
- Supply Chain positioning
- Medical Imaging Market & Challenges
- ASIC Benefits
- ASIC Design Flow

About us

- Core business is IC design services for
 - Medical Imaging
 - RF/mmWave applications
- Founded in 2015
- 100% privately owned
- Located in Athens, GR

Team's Credentials

- Adveos people have decades of experience in the semiconductor industry in
 - successful startups
 - high-growth medium-sized companies
 - global internationals
- Strong academic background
- A total of 11 papers in IEEE Journals and conferences
- A good grasp of all areas in a project - system down to transistor level
- More than 40 successful tapeouts - first pass success rate >90% (before 2012)
- Numerous chips are already in the market

ASIC facts

ASIC – Application Specific Integrated Circuit

- + Customized to meet user requirements
- + Smaller size and simpler PCB
- + Improved performance

BUT

- Time to market
- NRE overheads for design, manufacturing and test

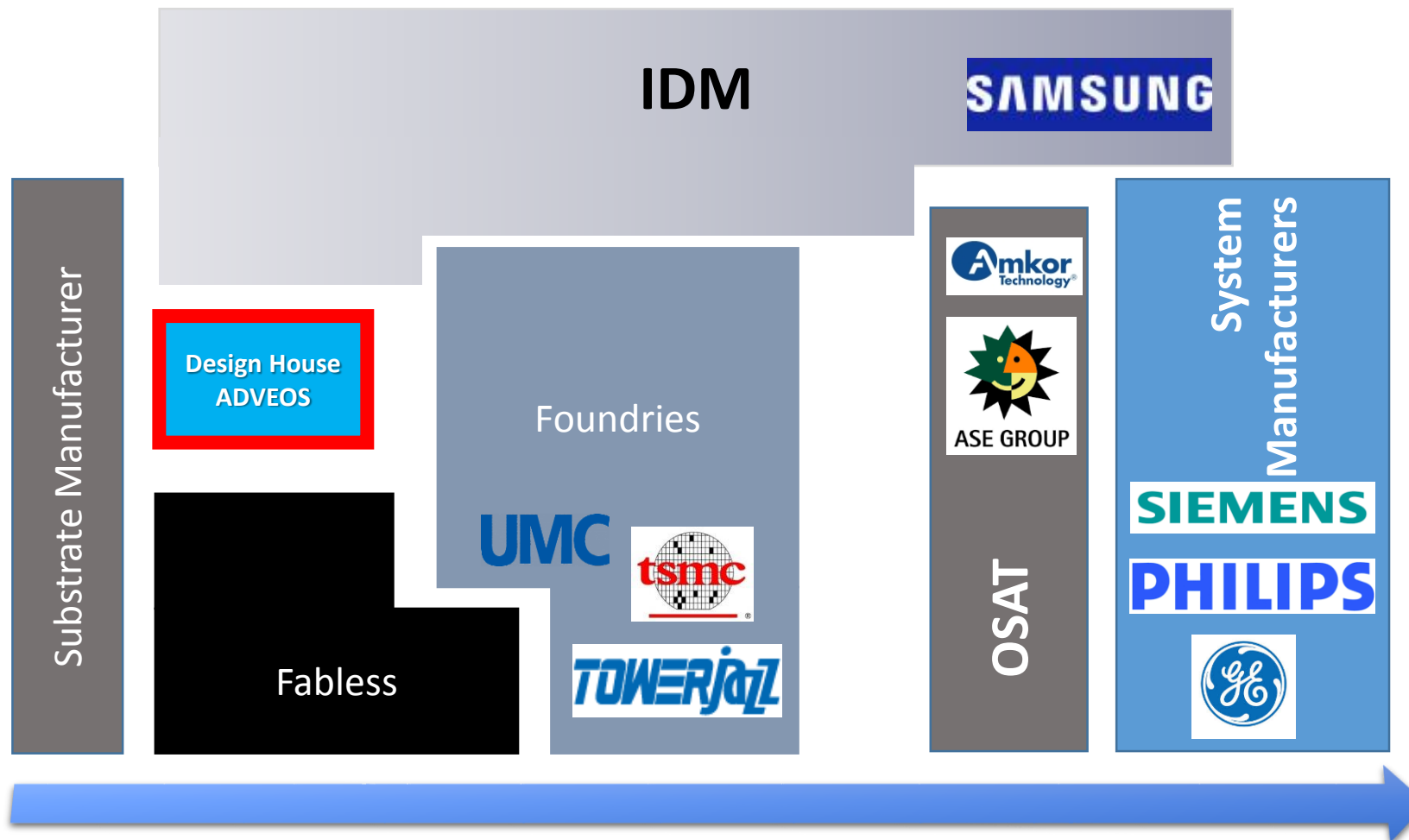


NRE – Non Recurring Engineering

Supply Chain mapping

IDM – Integrated Device Manufacturer
OSAT - Outsourced Semiconductor
 Assembly and Test

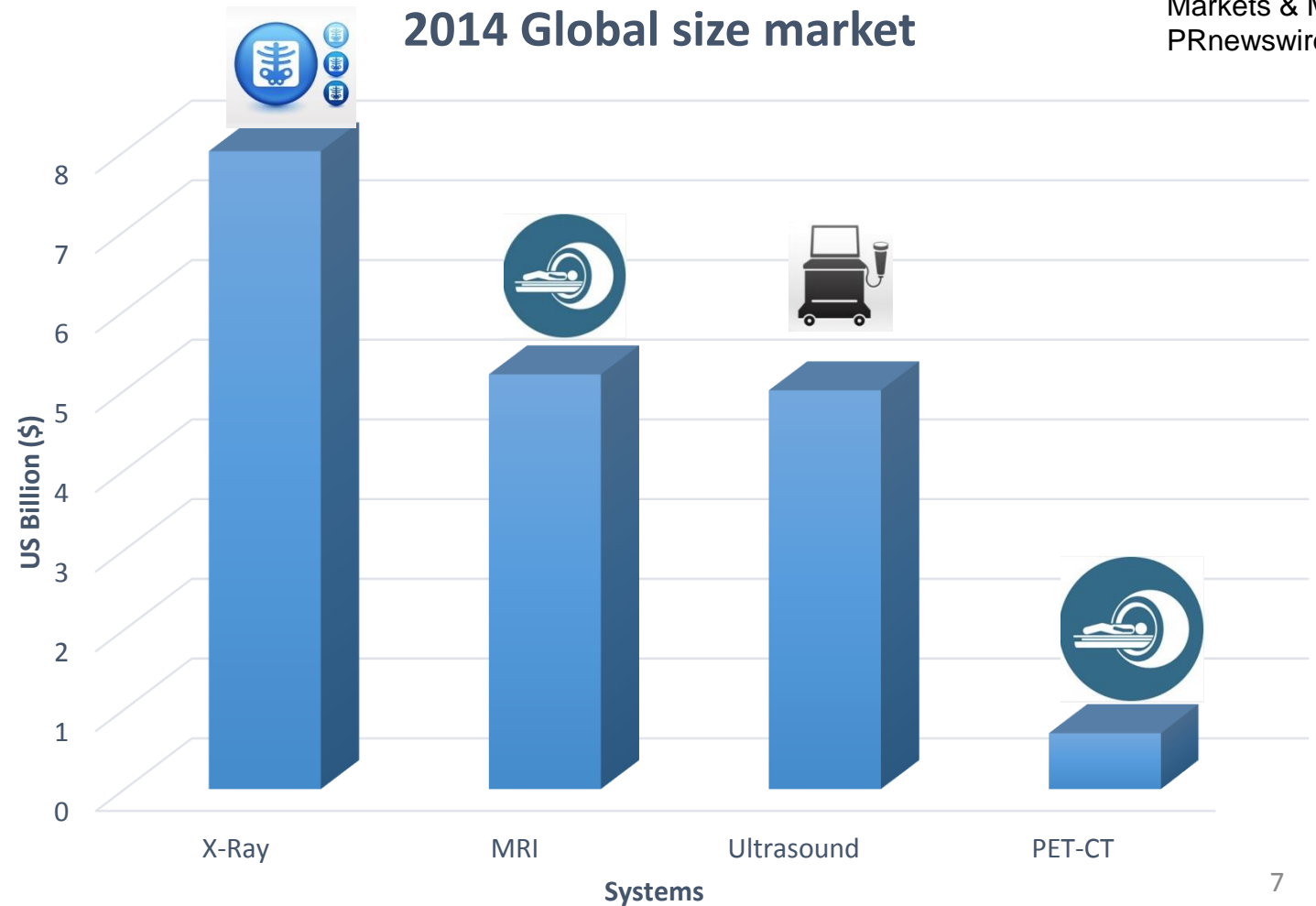
An example for the medical market - IC



Imaging & Radiation Detection market

Overall Market is huge
~20B€ and expected to
grow by 5-7% over the
next years

- Aging population
- More resilient to economic trends



Medical Device Market challenges

1. ASIC integration is a Must-Have for Medical products
 - Many medical devices require ASIC levels of integration even for entering trials
 - PCB full of discrete parts can only be used for bench level testing of early prototypes
2. MRI ASIC technology
 - Filtering and High speed and High Resolution ADCs to process pulse waveforms in the 60MHz to 130MHz range
3. Mixed Signal ASICs for PET, MRI and CT Scanners
 - Higher resolution systems – more acquisition channels to be placed in the same physical area

ASIC benefits for Medical Electronics

- Improved performance (power consumption, speed, reliability)
- Small form factor
- Reduce product's BOM
 - Although the NRE cost for design, manufacturing and test may be high for a low volume application
- **Real IP protection against competition**

Design Flow

Design Flow



Design Flow

- **Customer provides system specifications**
- **Adveos makes an initial feasibility study of the system**
 - Behavioral modelling of the system
 - Translate system specifications to specification for each individual sub-system/block
 - Identification of critical blocks for the performance of the system

Feasibility Study Review

- **Electrical design**
 - All blocks are electrically designed and simulated
 - Performance is evaluated under PVT corner conditions
 - The design is tuned so that all circuits pass the given specifications under every simulating condition requested by the customer (typical, corner, statistical variations)
 - Models for the packaging of the chip and the PCB of the final/testing platform are introduced in order to be taken into account in the system performance

Design review

Design Flow

- **Physical design**

- The layout of all the system blocks is produced
- The parasitics of the layout are extracted (for very critical blocks and depending on the application, an electromagnetic simulator is used at this step)
- Simulations with all the extracted parasitics are performed and the results are compared with those of the electrical design
- If necessary, layout of blocks is improved until their performance meets the given specifications

Design review

- **Post layout verification**

Tape-out

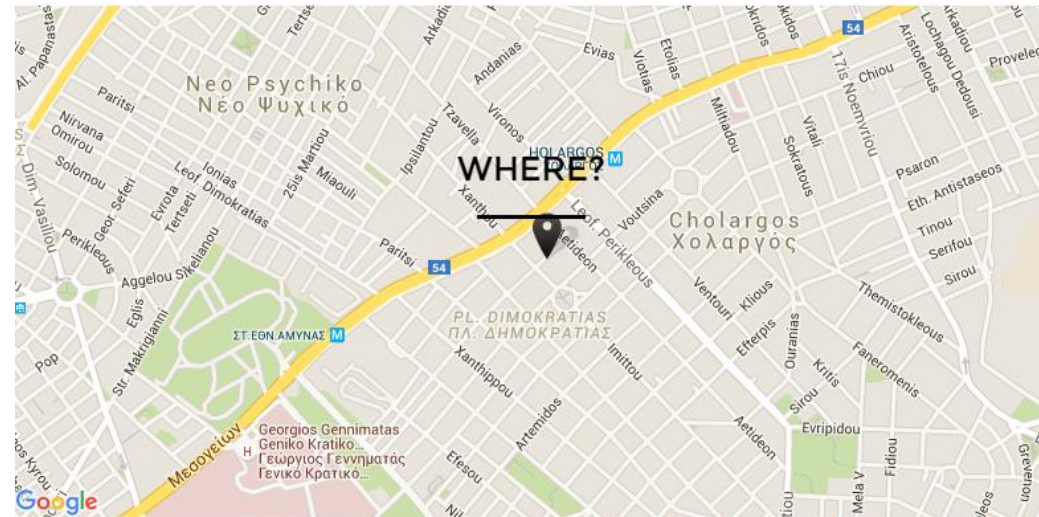
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Thank you!

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