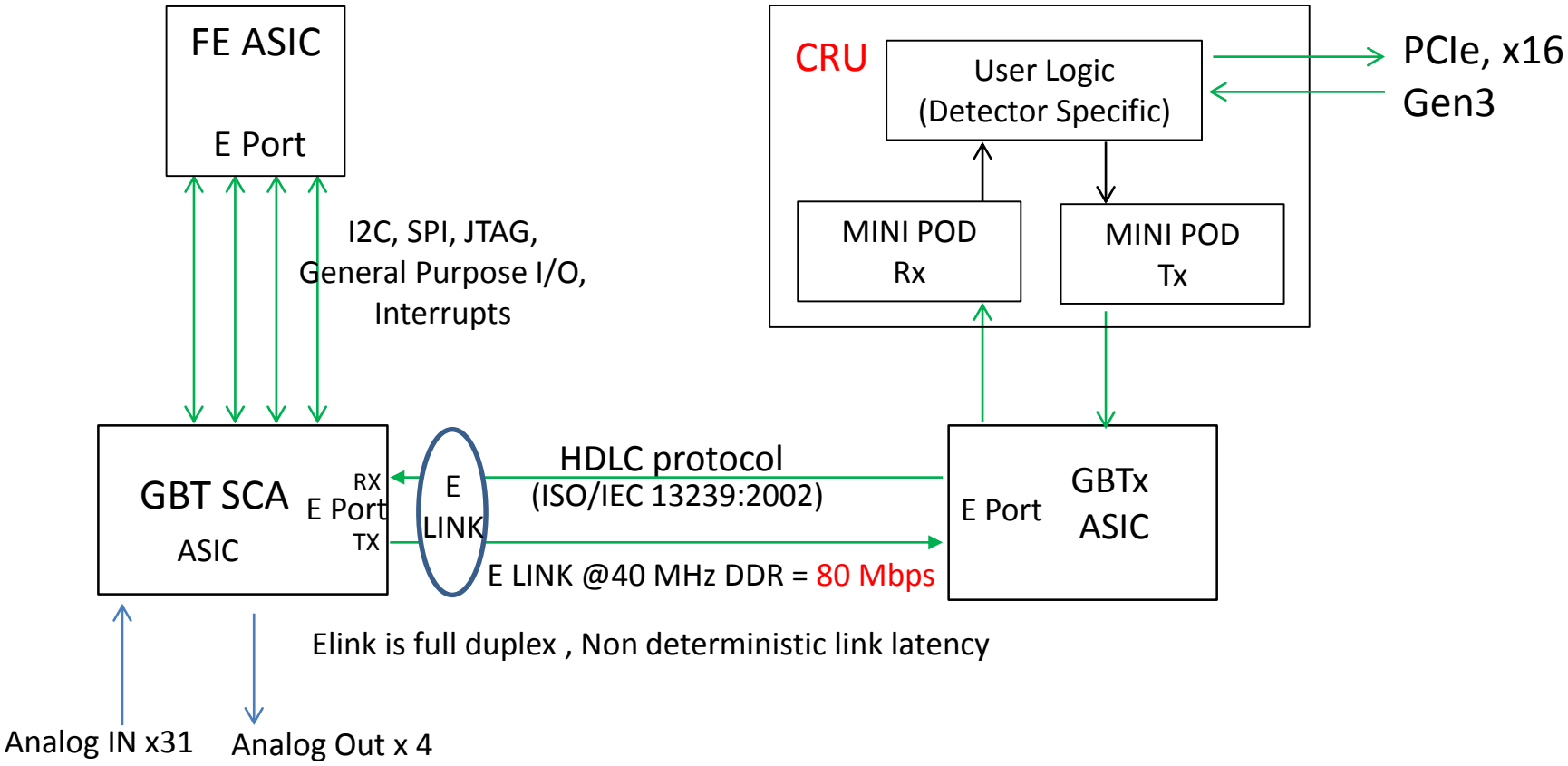
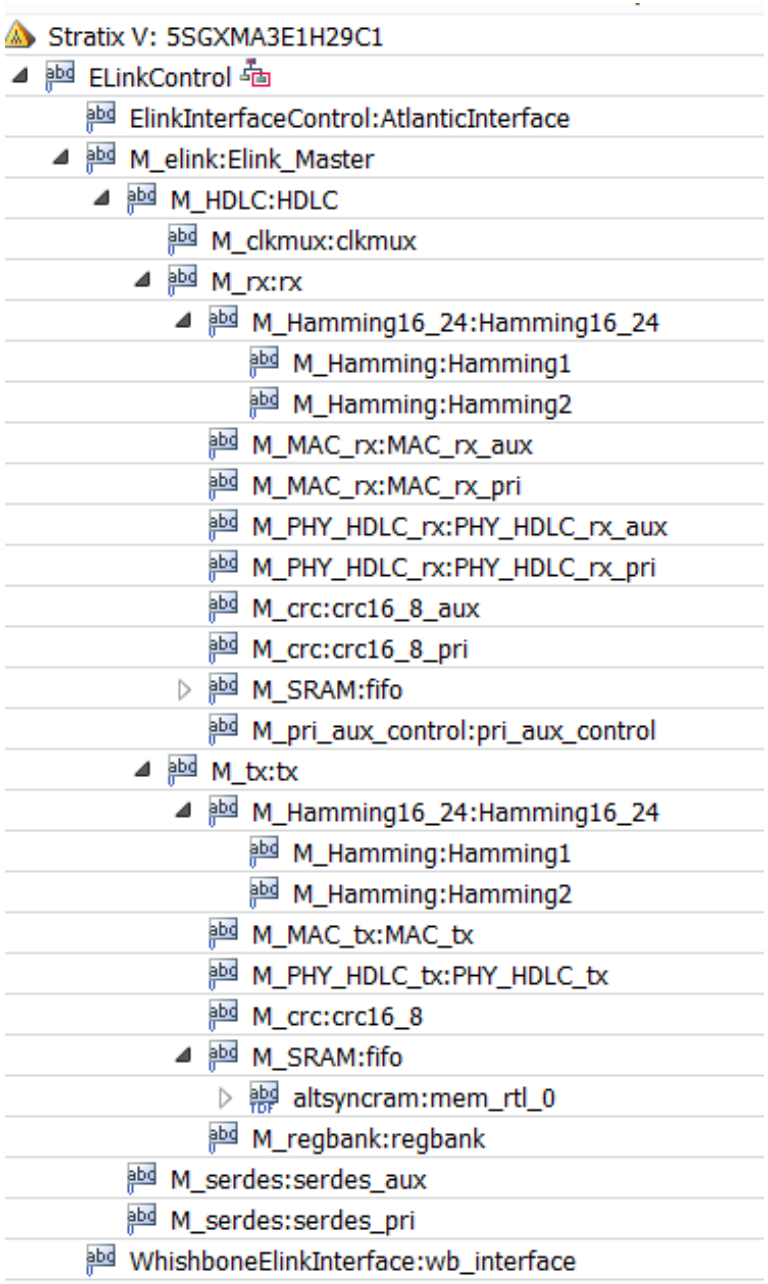
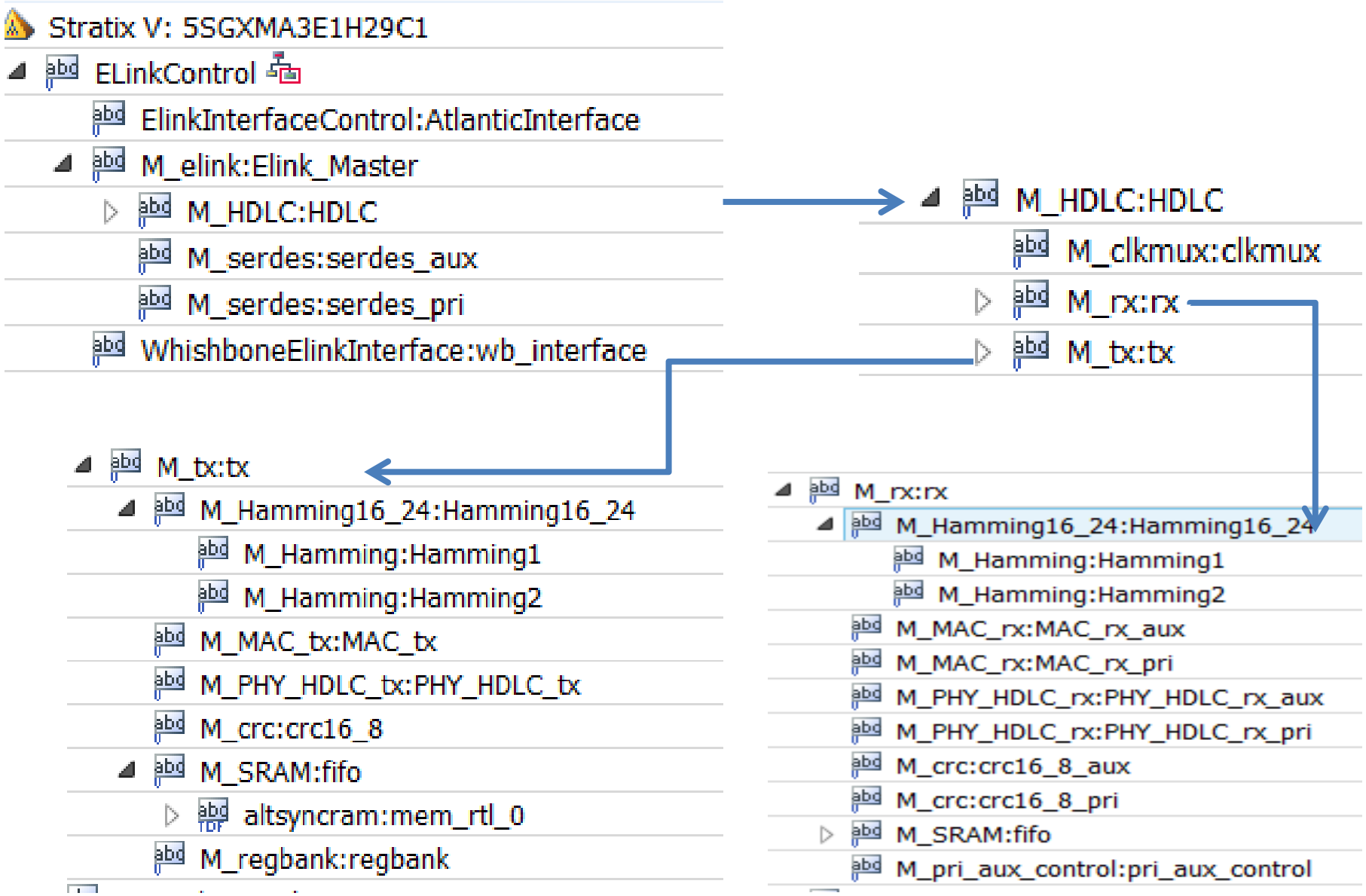
CRU DCS Interface Discussion

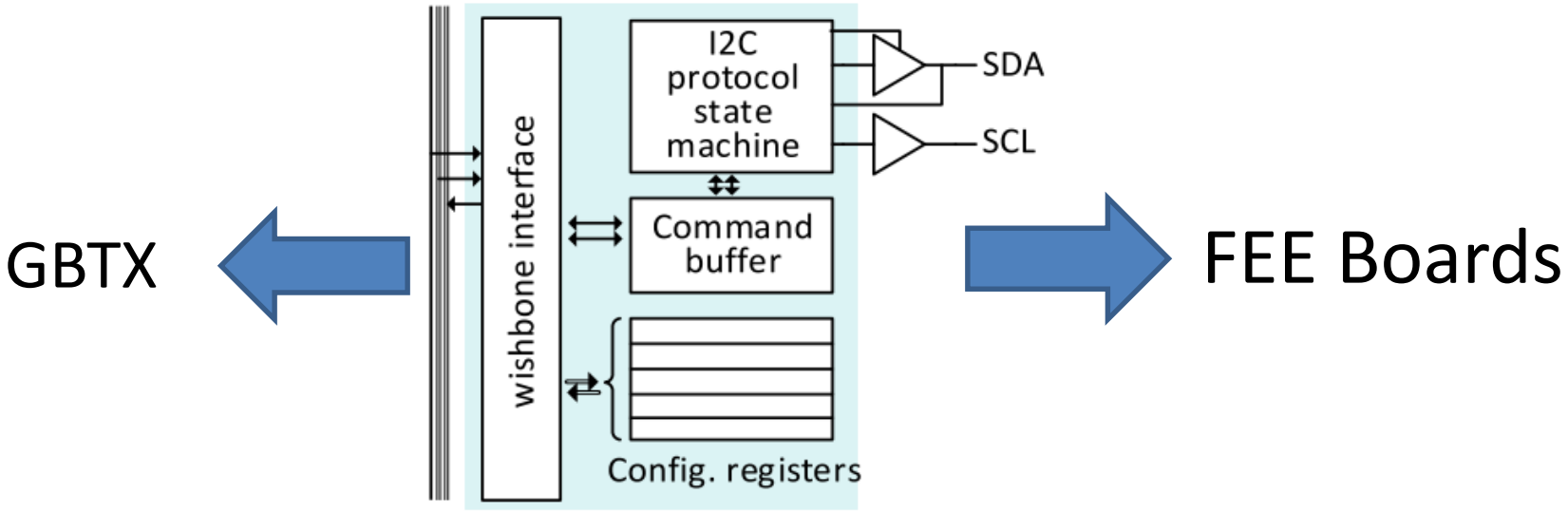
Communication Flow between DCS and CRU



E Link Hierarchy




Stratix V: 5SGXMA3E1H29C1
ELinkControl
ElinkInterfaceControl:AtlanticInterface
M_elink:Elink_Master
M_HDLC:HDLC
M_serdes:serdes_aux
M_serdes:serdes_pri
WhishboneElinkInterface:wb_interface
M_HDLC:HDLC
M_clkmux:clkmux
M_rx:rx
M_tx:tx
M_tx:tx
M_Hamming16_24:Hamming16_24
M_Hamming:Hamming1
M_Hamming:Hamming2
M_MAC_tx:MAC_tx
M_PHY_HDLC_tx:PHY_HDLC_tx
M_crc:crc16_8
M_SRAM:fifo
altsyncram:mem_rtl_0
M_regbank:regbank
M_rx:rx
M_Hamming16_24:Hamming16_24
M_Hamming:Hamming1
M_Hamming:Hamming2
M_MAC_rx:MAC_rx_aux
M_MAC_rx:MAC_rx_pri
M_PHY_HDLC_rx:PHY_HDLC_rx_aux
M_PHY_HDLC_rx:PHY_HDLC_rx_pri
M_crc:crc16_8_aux
M_crc:crc16_8_pri
M_SRAM:fifo
M_pri_aux_control:pri_aux_control



The GBTSCA include 16 independent I2C master serial bus with the following features:

1. Concurrent operation of all 16 channels
2. Individually programmable data transfer rates: 100 KHz, 200 KHz, 400 KHz, 1 MHz Supports both 7---bit and 10---bit addressing standards
3. Supports single--byte and multibyte I2C read/write bus transactions Support read---modify---write atomic operations with 'AND', 'OR' or 'XOR' masks.

The I2C channels implements a set of registers

- to configure the interface and the operating modes,
- to read the received data and write the bytes to transmit.

Specific commands are defined to access those registers. It defines a set of commands to start the I2C operations on the bus.

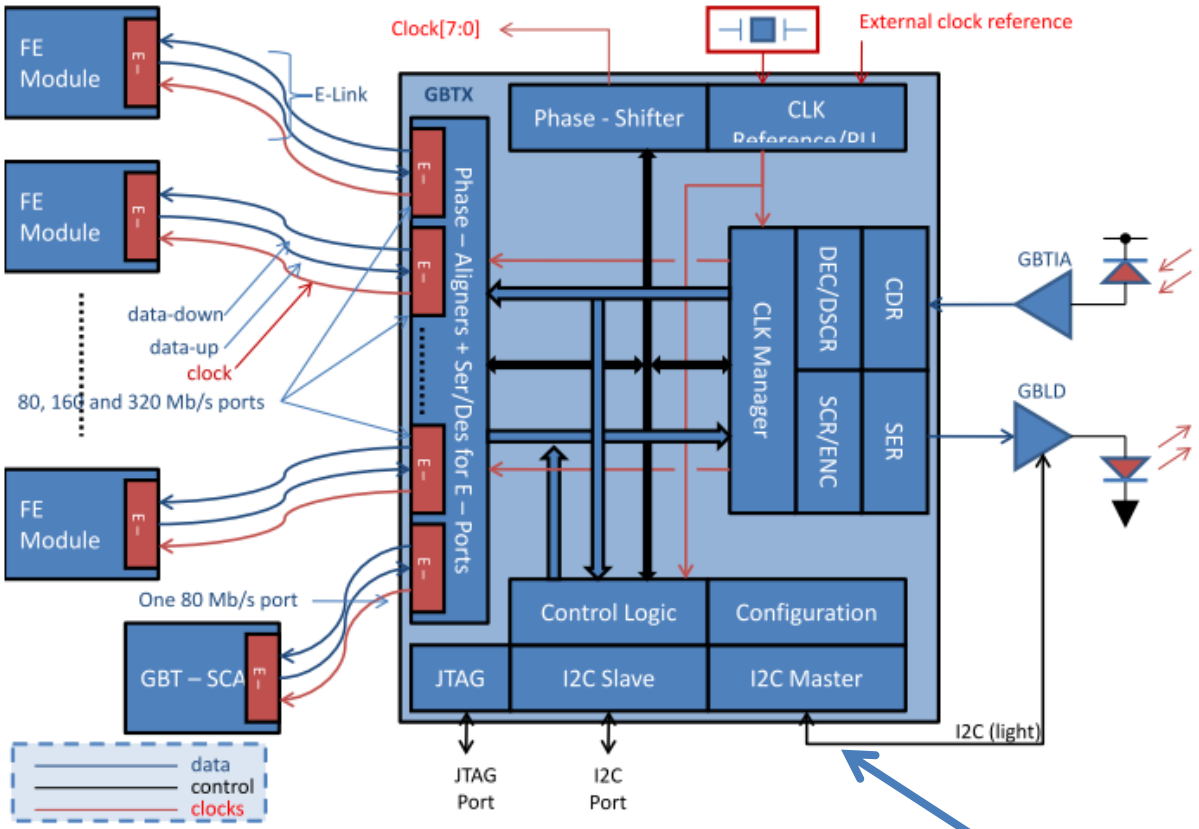
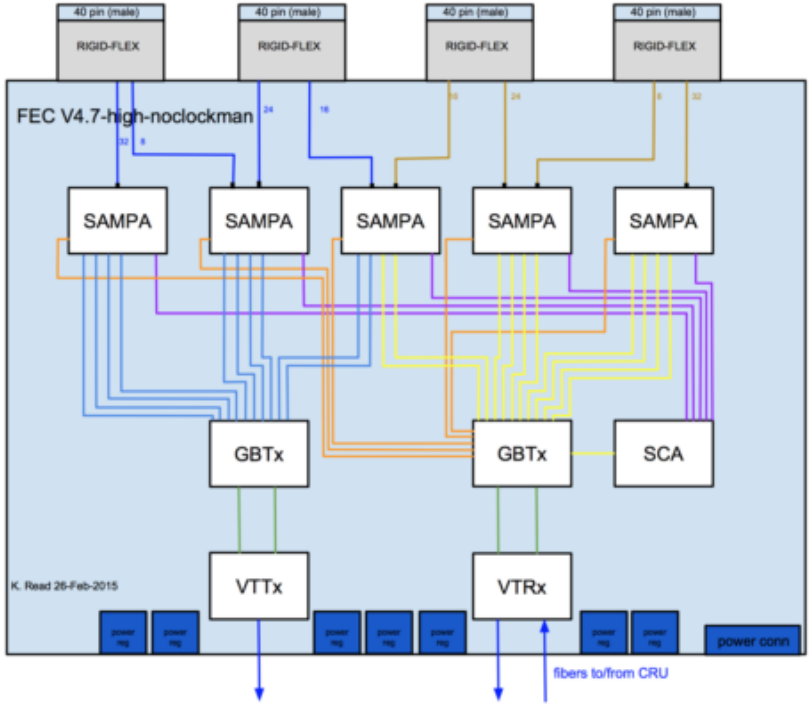


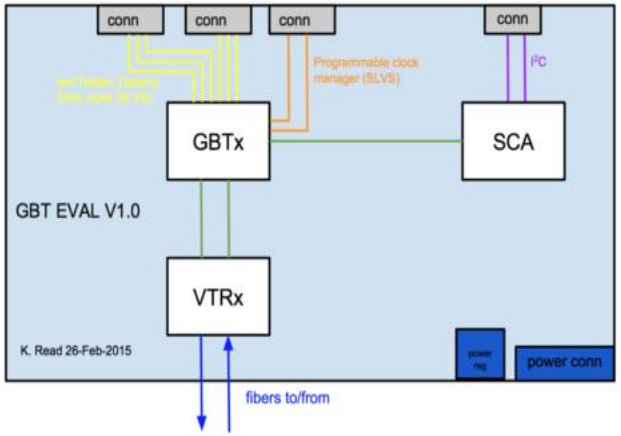
Figure 2 GBTX architecture and interfaces.

Assumption by ERNO: that VTRx and VTTx and the second GBTx ASIC (the one connected to the uni-dir VTTX) will be connected to SCA I2C master

FEC Conceptual Drawing



Discussing GBT Evaluation Board with MCH



How to start with GIT ?

How to submit the projects in GIT ?