Status of LHCb Upgrade Electronics

Thanks to colleagues from whom I stole pictures
http://lhcb-elec.web.cern.ch/lhcb-elec

2015….. Lots of reviews

VeloPix EDR
PLL for VeloPIX EDR
Velo Hybrid & OPB EDR

UT SALT EDR
UT Electronics General Review

SciFi PACIFIC EDR

CALO ICECAL EDR

Muon nSYNC, nODE, nSB, nPDM EDR

Signs of very good progress

All new ASICs have been reviewed

All ASICs have been proto-typed to some level

Review reports on EMDS:
LHCb Experiment Upgrade/Common Electronics/Reviews

ASIC technology

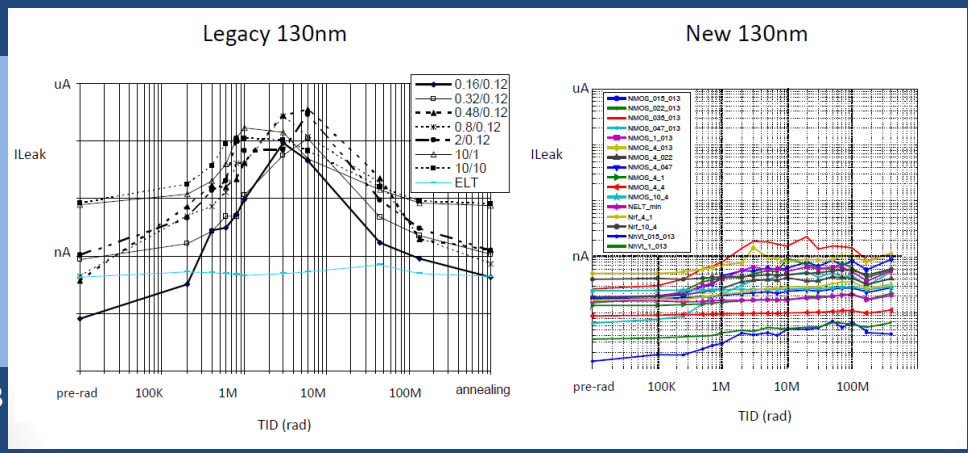
Reminder: after risk-assessment,
Velo, UT, SciFi changed ASIC technology to new vendor

Some pain during transition process (mostly with design kit)

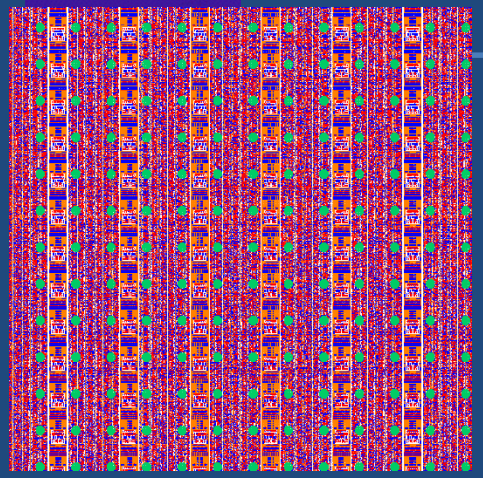
But we are now benefitting from

- Fast delivery time
- Sharing of design blocks
- Attractive pricing
- Improved performance
- Design kit that is now stable

NB: We have to keep an eye on the radiation effects (Velo & UT)
Constantly monitor the technology (eg leakage current evolution)

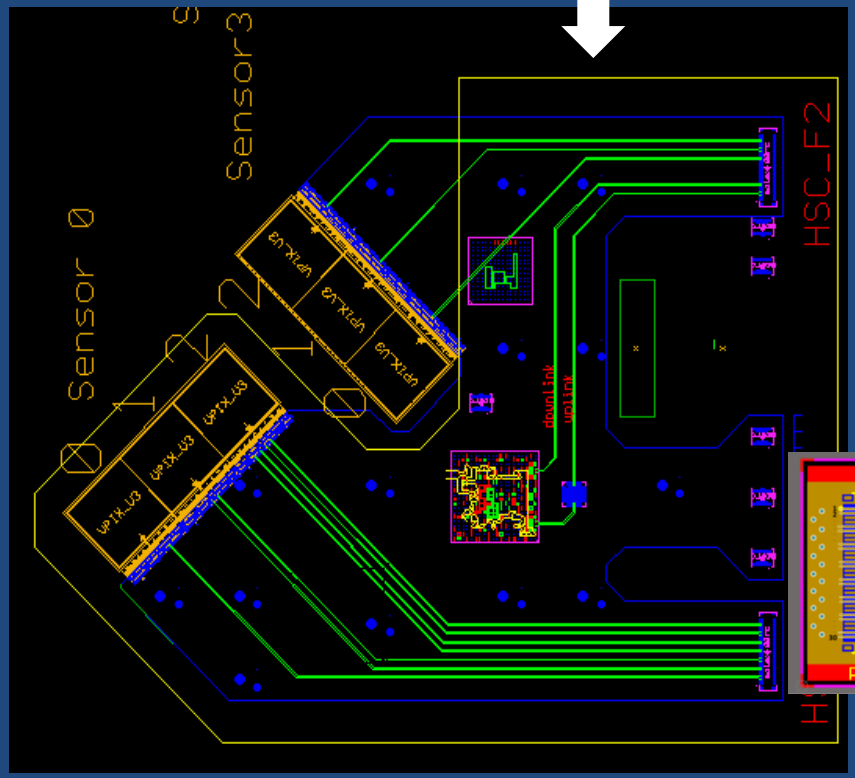


Velo

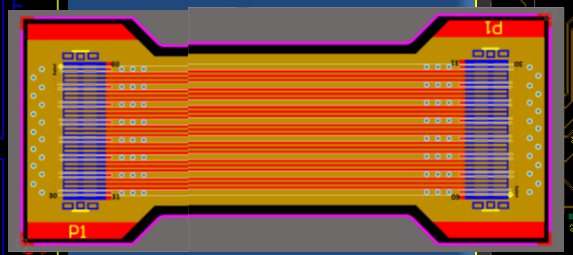


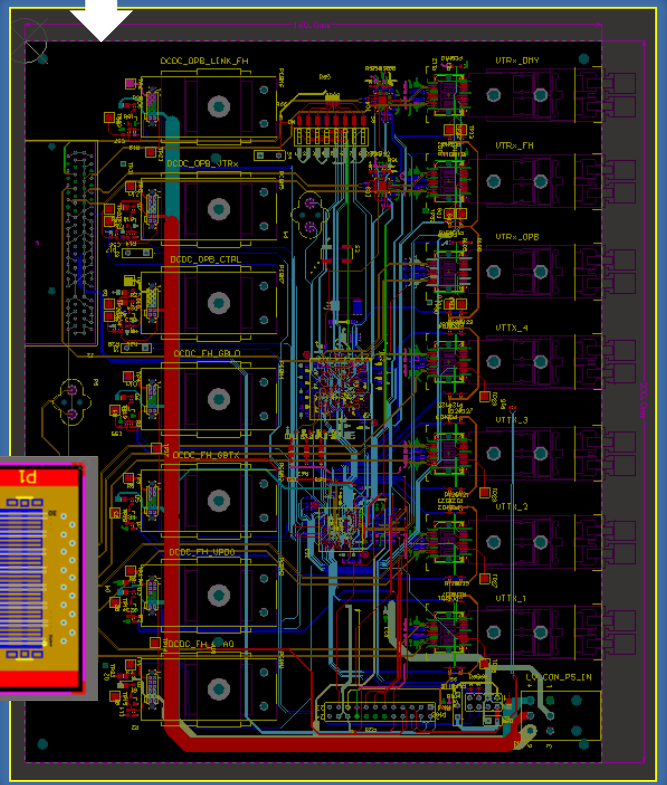
VeloPIX is nearly ready
Blocks being assembled, simulated, analysed
NB this is the ‘final’ chip, all features included

Hybrid & Opto-Power Board design

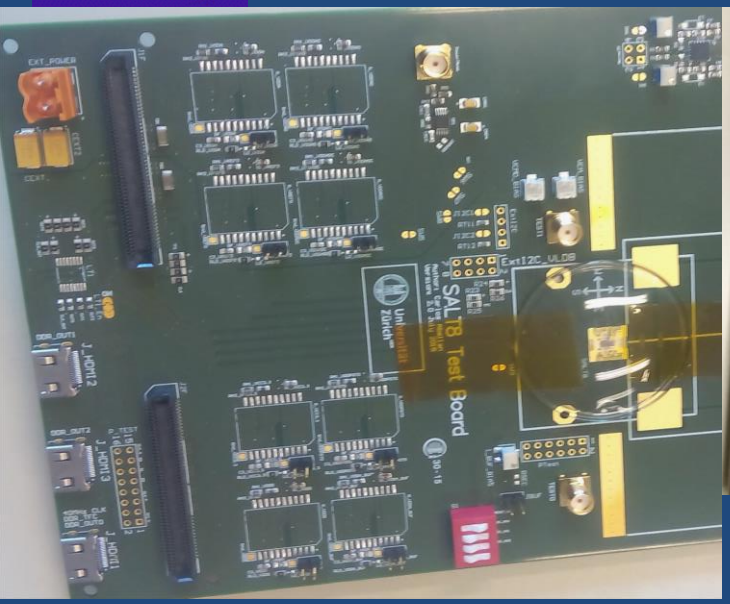


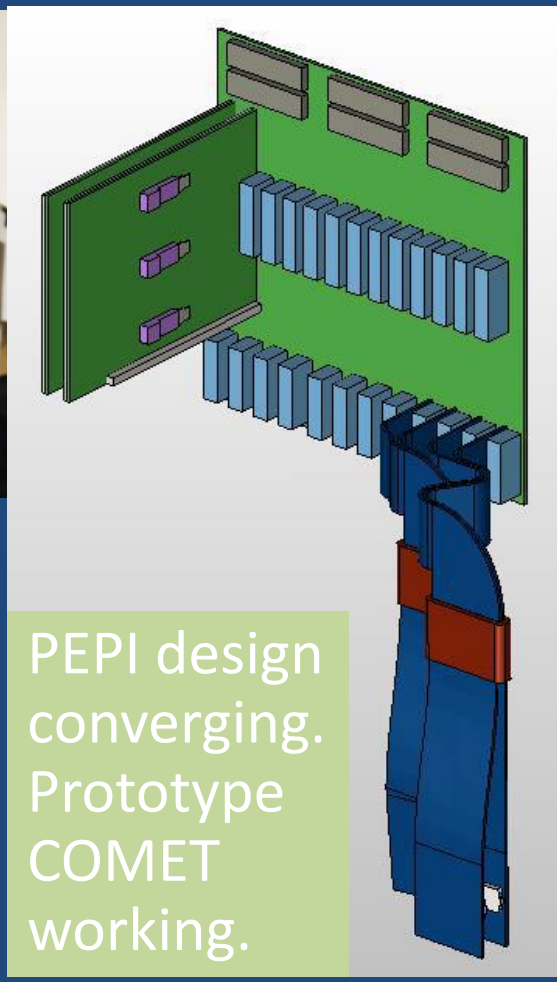
Data link out of vacuum is challenging





UT





SALT8 v1 tested.
Some bugs but useful for learning & building system.
v2 submitted 2 weeks ago

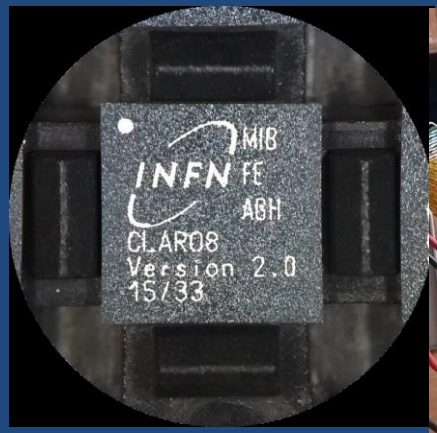
Long flex prototyped with CERN.
Discussions with industrial supplier.

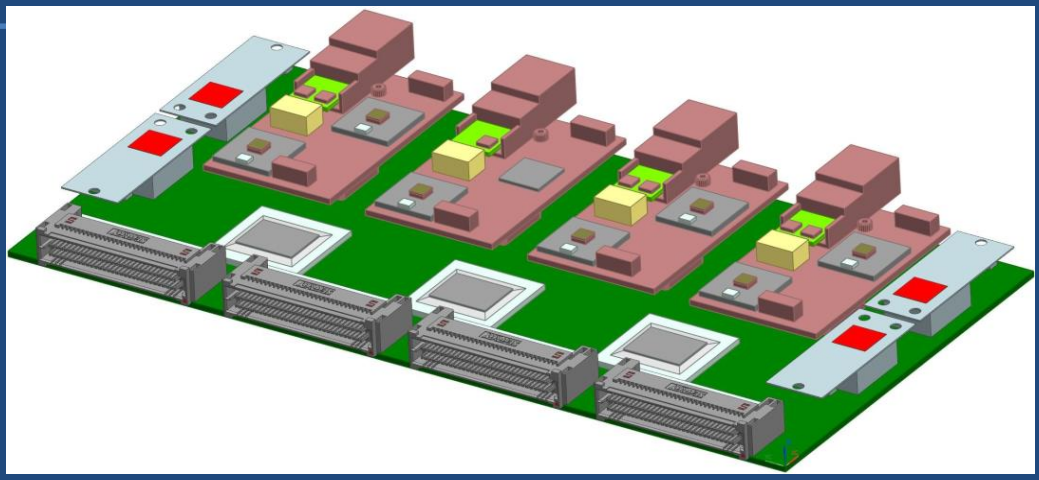
PEPI design converging.
Prototype COMET working.

Slice test now close – important test of many aspects

Early user of TFC/ECS/DAQ interface through miniDAQ

RICH





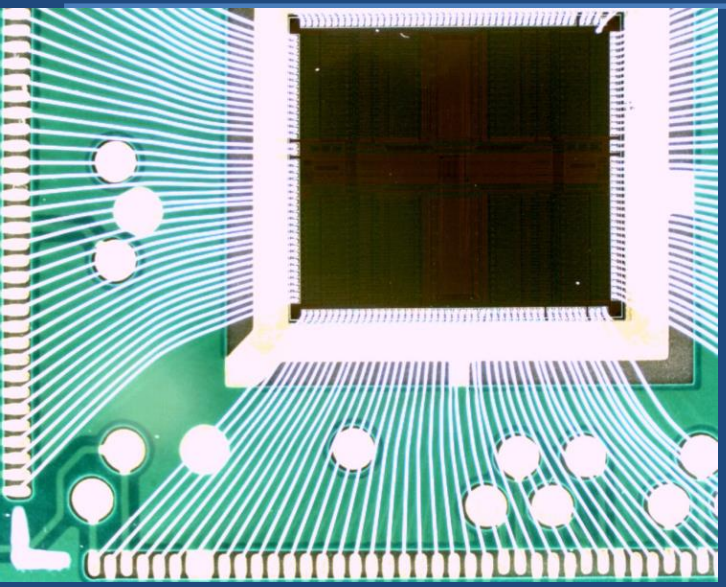
Digital board under design, with constraints from mechanics & cooling

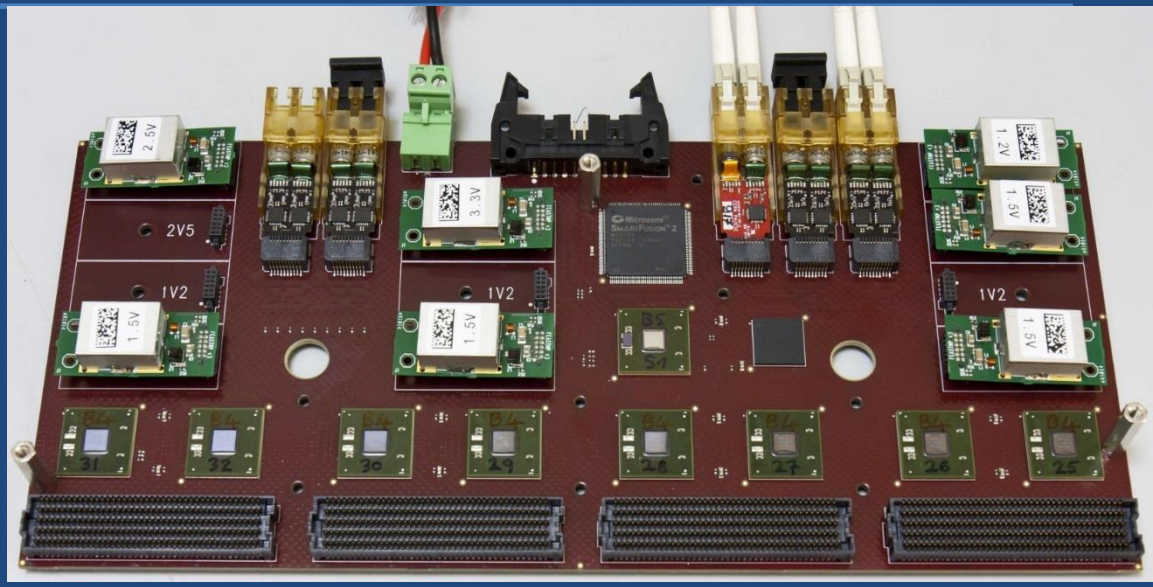
CLARO8 v2 tested.
Big improvement on v1.
Used extensively in testbeam.

A few issues observed, to be rationalized by RICH group.

Irradiation tests of FPGA started (TID & SEUs).
Configuration is sensitive to SEUs => rate is crucial for performance of RICH.

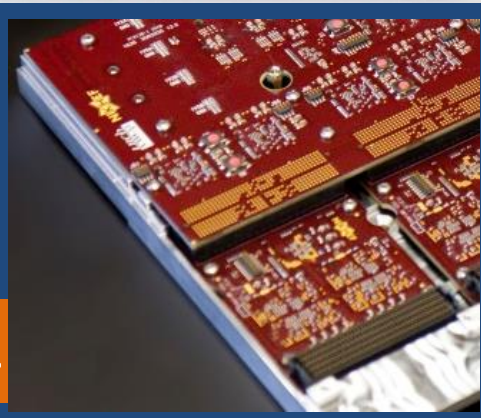
SciFi





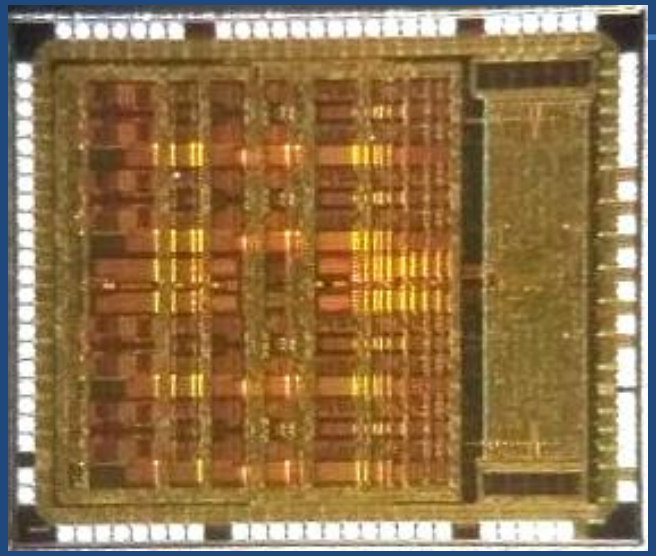
PACIFIC3 tested.
Working well.
Few small issues to improve.

FEB prototype tested.
Working well, other boards coming.

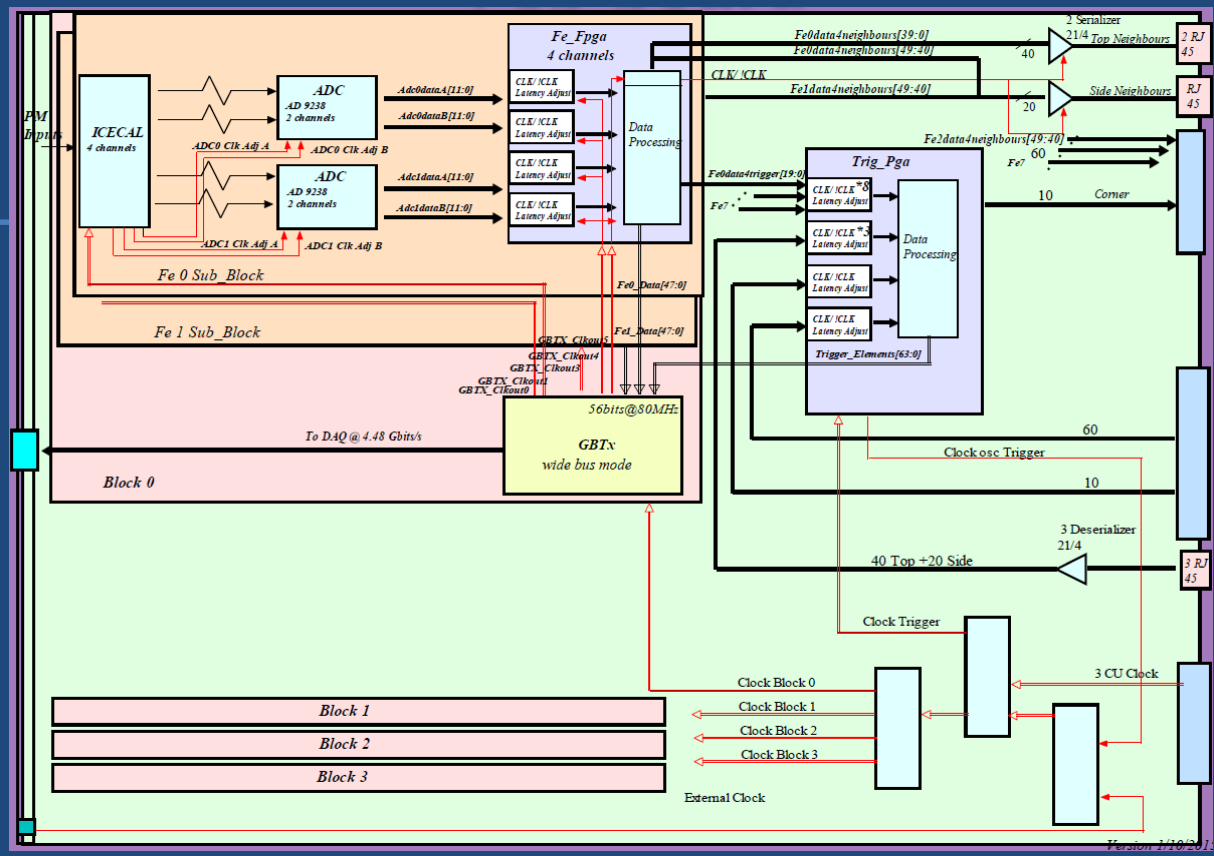


Early user of TFC/ECS/DAQ interface through miniDAQ

Calo



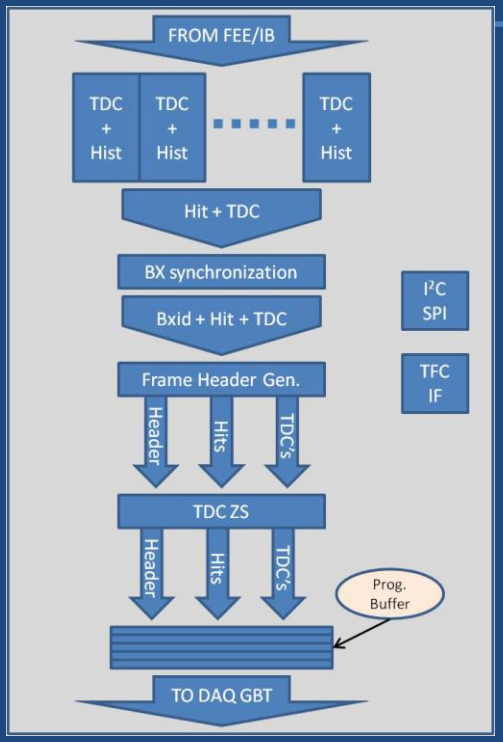
ICECAL v3 tested.
Working well.
Used extensively for testbeam.
Neutron radiation damage assessed (OK).

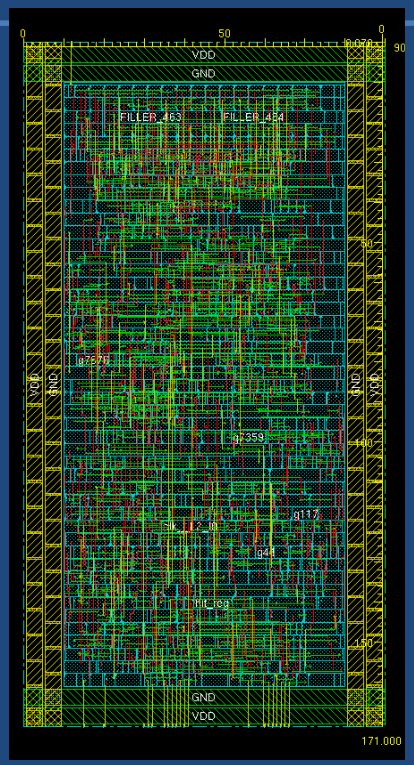


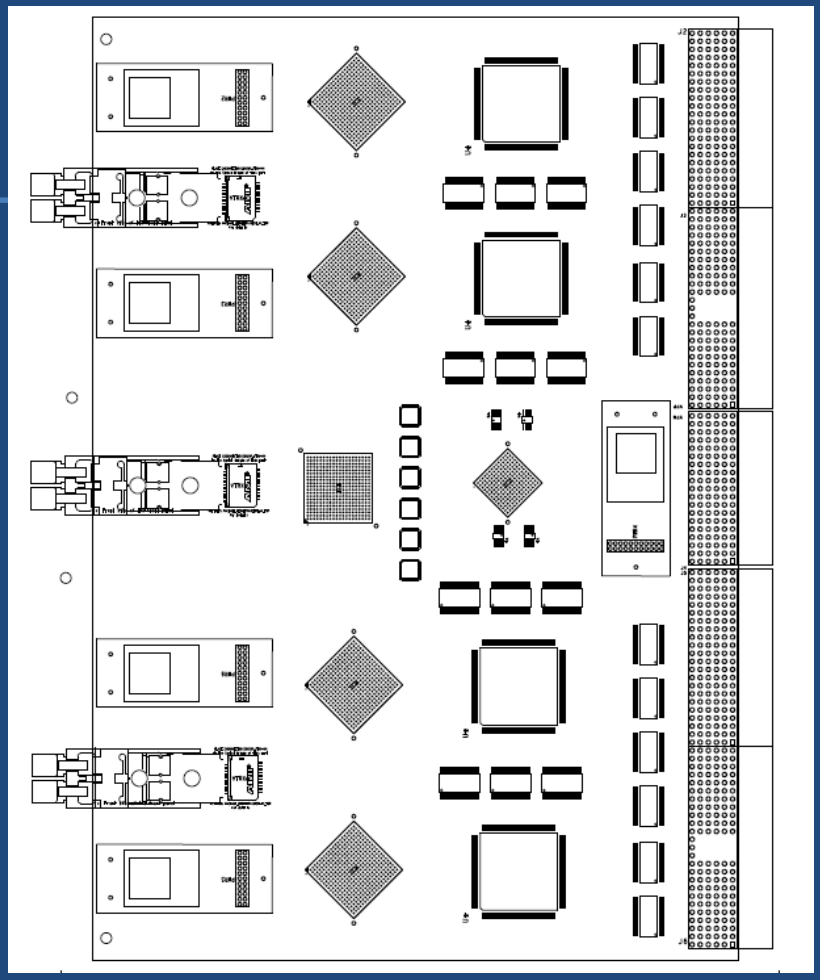
FEB design well advanced.
Optimization: Removal of individual LLT link
LLT data combined with DAQ data.

On-going discussion on dynamic range…….

Muons







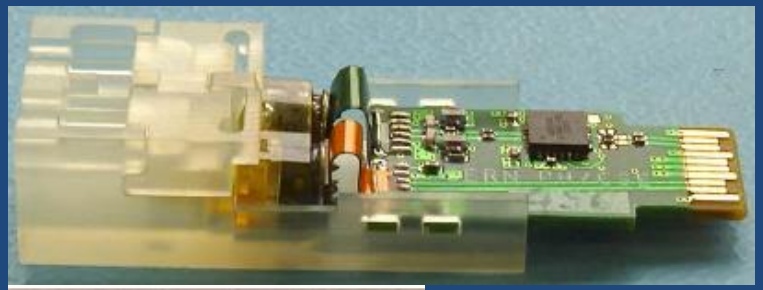
nSYNC under design.
TDC block using digitally-controlled-oscillator.
Already tested OK.

nODE, nPDM, nSB under design.
Compatible with existing infrastructure.
Optimization: Hit map & TDC data transmitted on same links

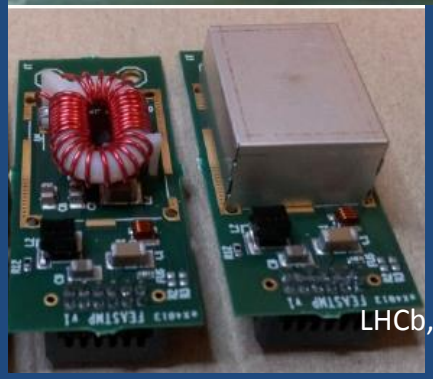
Common components

GBTX production started
50,000 chips in total
wafers, packaging,
automated testing by company
GBTXs for Velo hybrids already delivered
GBT-SCA version 2 submitted
(improved ADC, 3.3V compatible)

Versatile Link optical components
Starting in December, monthly batches



Rad-tol DC-DC convertor
5000 parts under test, delivery soon



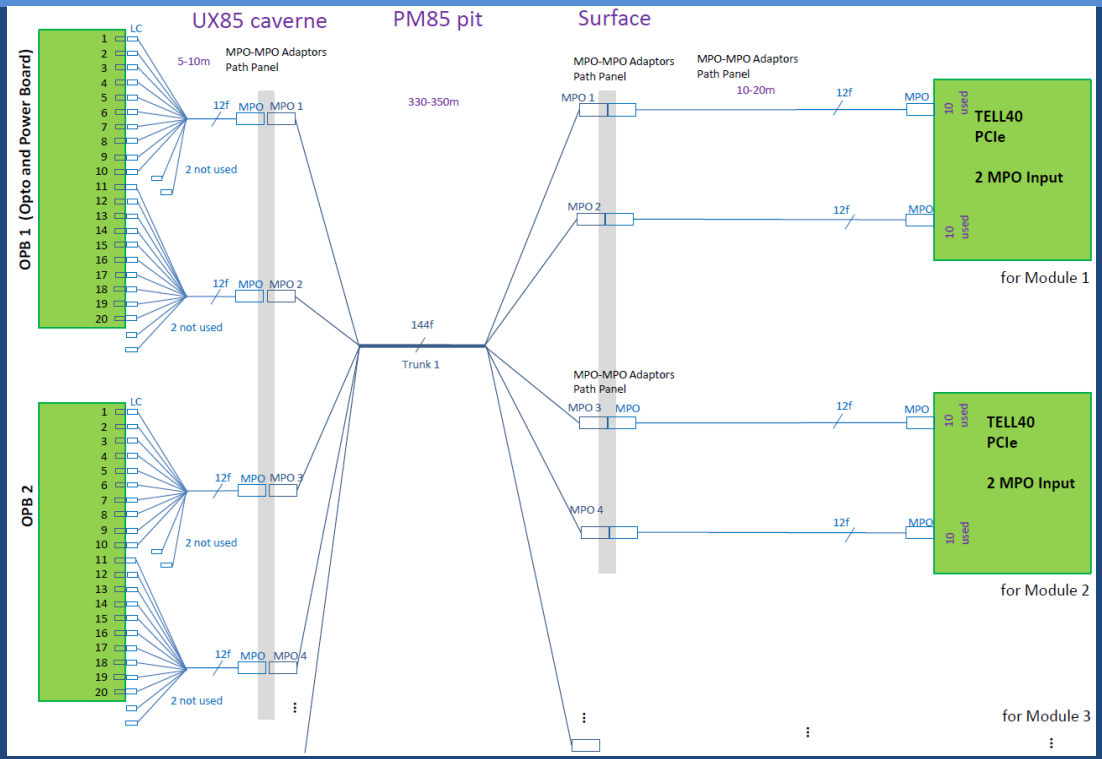
Optical fibres

Sub-detectors are converging on their numbers:

- long distance fibres
- patching to front-end
- patching to PCIe40

Tests at Point 8 are very encouraging (double-length)

Online group preparing more links with VTRx/VTTx



PCIe40 => TELL40 + SOL40

Prototypes tested OK

Small changes
=> ready for miniDAQ2
But delay in FPGA delivery
=> miniDAQ2 in spring 2016

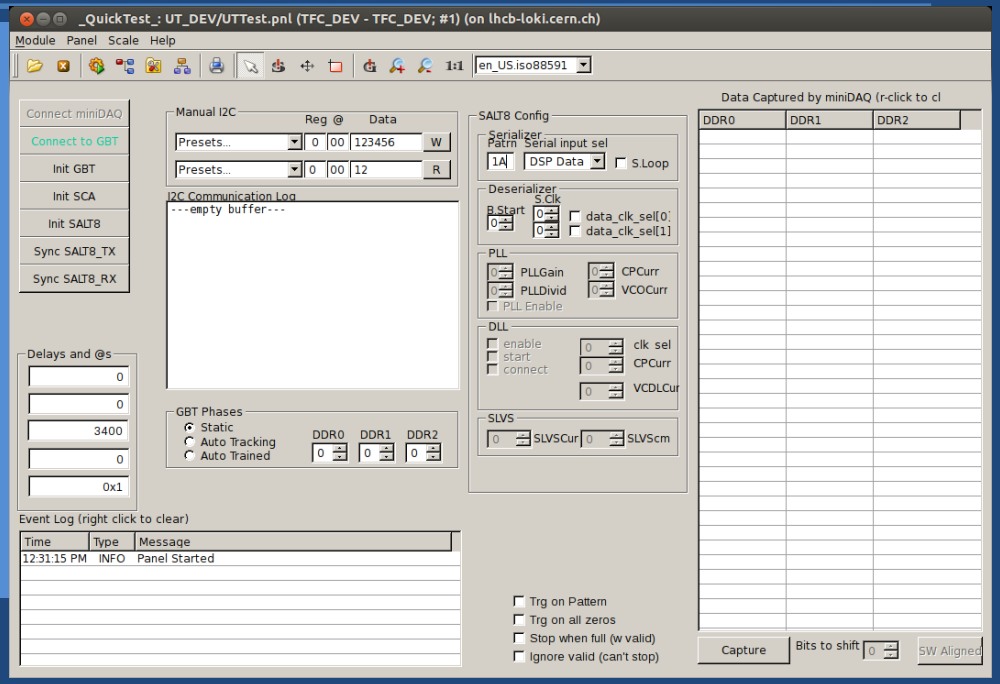
Commercial procedure started for full production

Firmware framework & management in place
active community, constantly evolving
all (almost) sub-detectors actively using the mini-DAQ
good communication is essential !!!!

TFC/ECS (SOL40 platform)

ECS:
FPGA firmware seems to be stable (some features still to be tested)

Focus is moving to the software (WinCC etc)
Example of custom panel for UT SALT8 testing



TFC:
Passive-Optical-Network under test now with PH-ESE

Focus now on sub-detectors needs for testing Front-Ends with miniDAQ (eg triggering, test patterns etc etc)

Look ahead to 2016…..

Lots of reviews!

Completion of ASICs in all sub-detectors

Prototyping of Front-End-Boards……. some thoughts:

We will create a lot of data !!! (one SciFi FEB = ~ 40 Gbit/s)

Sub-detectors will need:

- hardware to check all data => miniDAQ
- interfaces to configure/control => miniDAQ
- software to configure/control => ECS framework

Steep learning curve – start now!

Strong support required from miniDAQ team
ECS/TFC team