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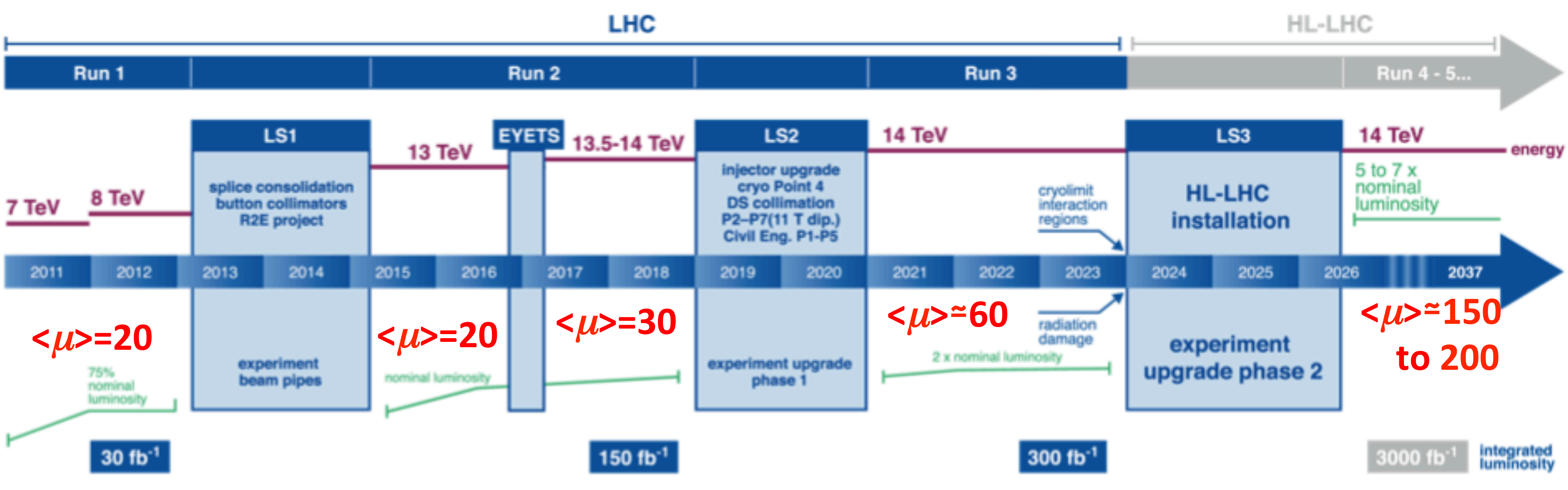
ATLAS Calorimeters: Run-2 performance and Phase-II upgrade

Djamel Boumediene
On behalf of the ATLAS Collaboration

cnrs dépasser les frontières
LPC Particules pLasmas Univers applicationS
Laboratoire de Physique de Clermont
ATLAS

LHC timeline

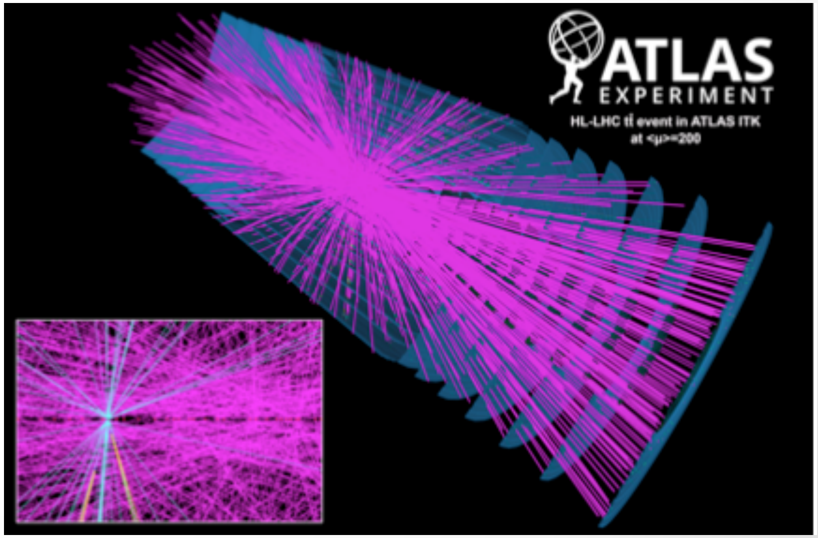


Phase-II conditions:

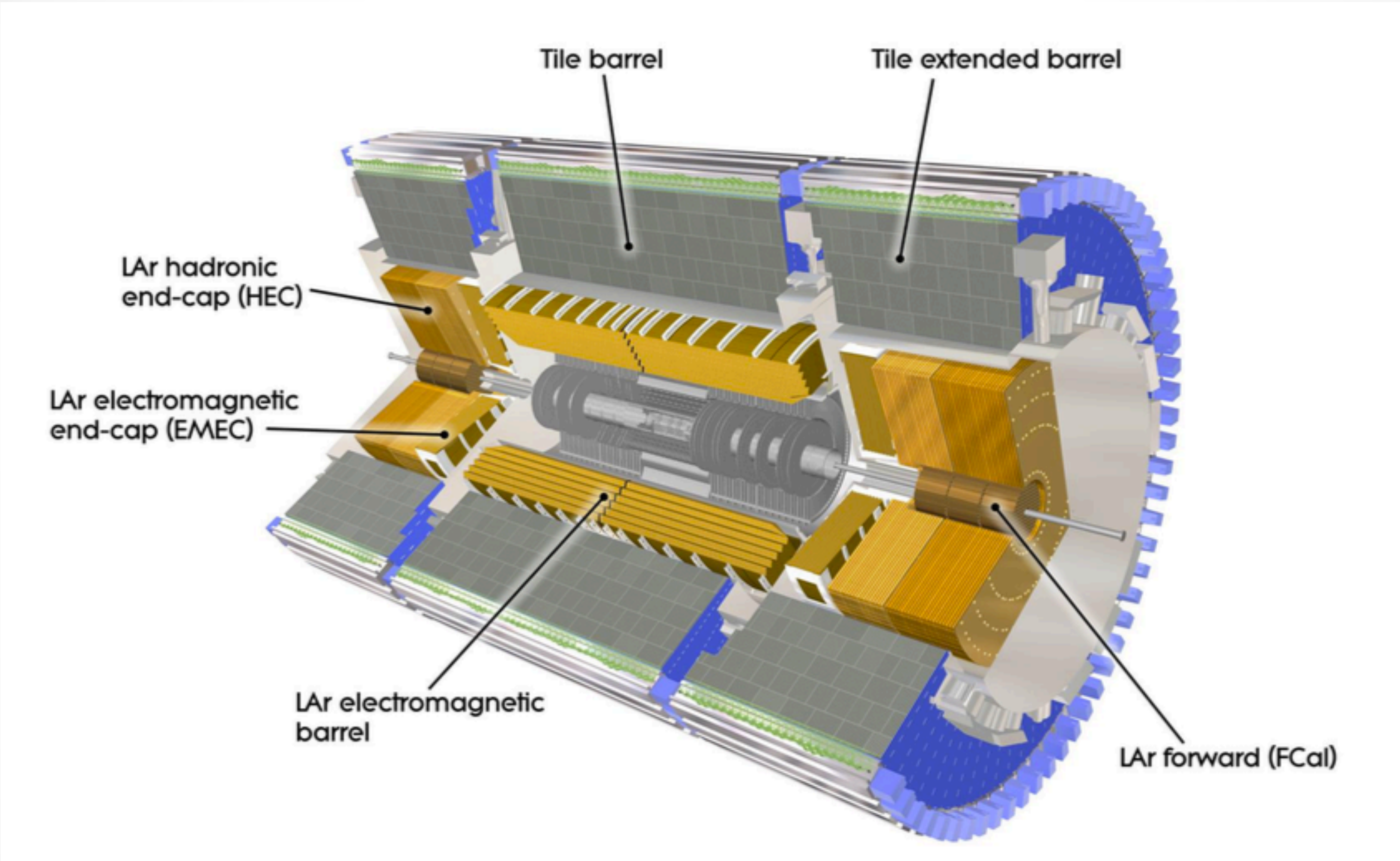
- Starting at the end of 2026
- L=5-7 x 10^{34} $cm^{-2}s^{-1}$ and 3000 fb^{-1}
- Challenging pile-up:

Up to 200 collisions per bunch crossing (σ_t = 150 ps, Δz = 50 mm)

Overlapping vertices, high pile-up noise in calorimeter endcaps and forward region

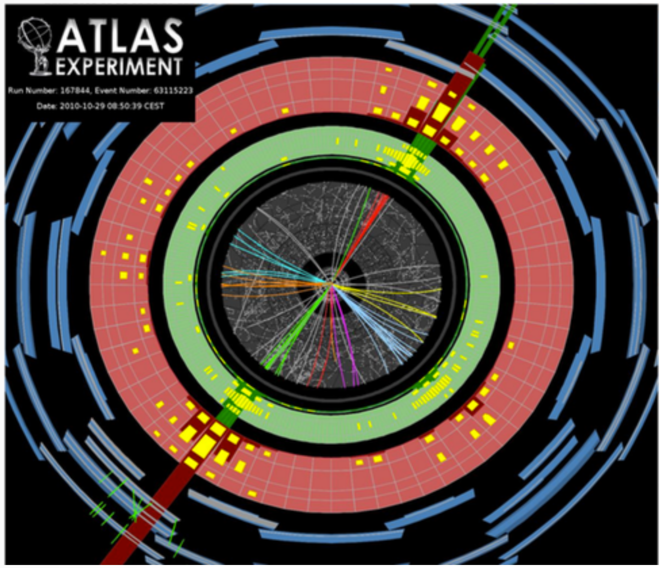


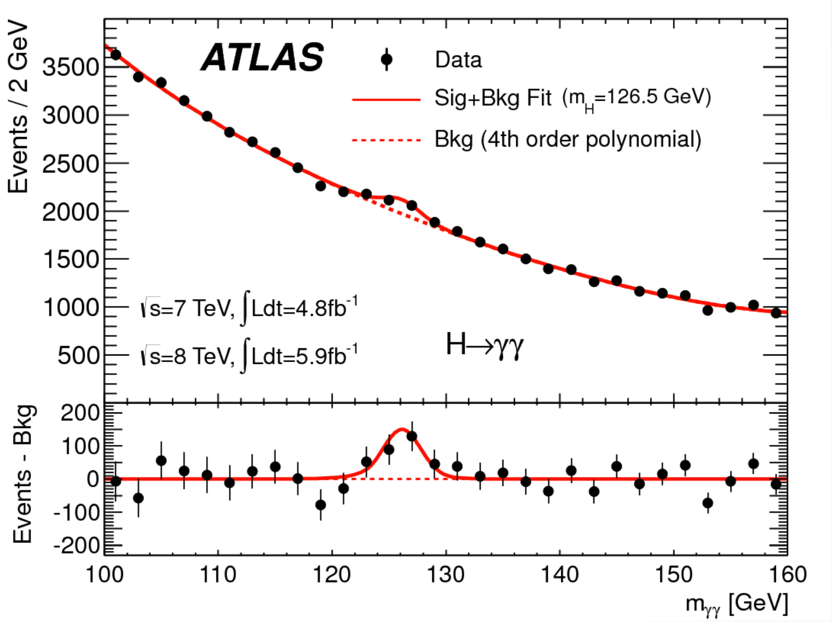
ATLAS Calorimeters



ATLAS Calorimeter upgrades for Phase II

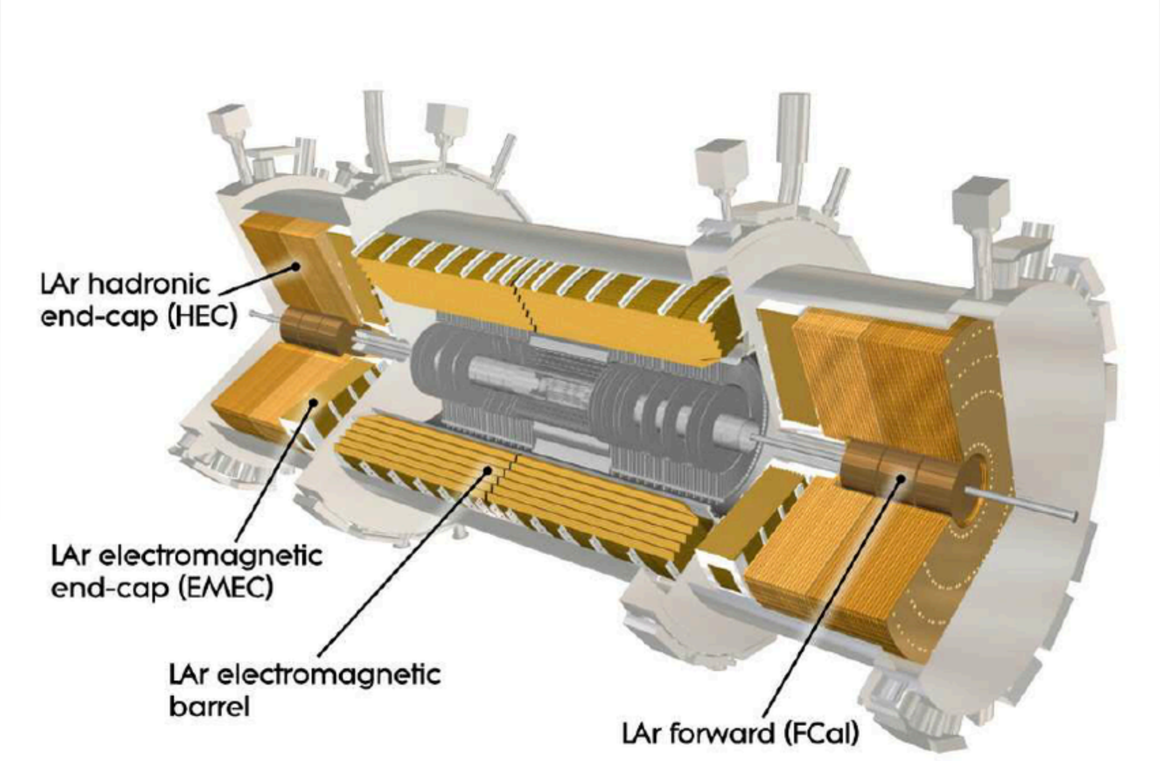
- ATLAS calorimeters operated successfully during Run I and Run II of LHC





- Calorimeters to be adapted to Phase-II requirements:
  - Latency and Trigger rate of 1MHz at Level 1
  - Radiation Hardness above nominal design
  - Send full Front End granularity digital data at 40 MHz to back-ends
- Extended tracker at high η:

  Complete with high granularity and timing calorimeters



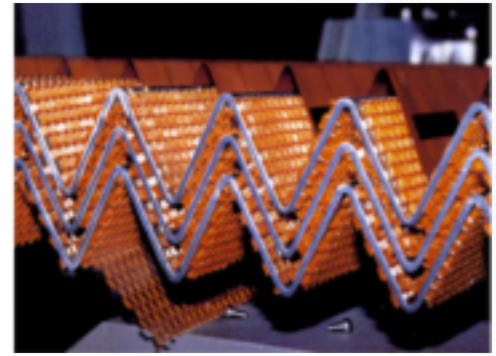
The Liquid Argon Calorimeters (LAr)

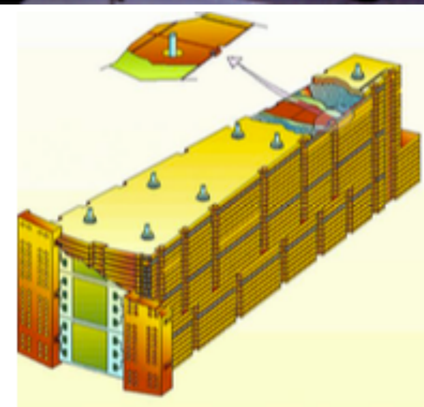
The Liquid Argon Calorimeters

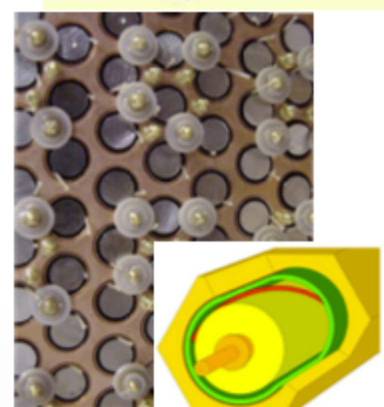
- EM Barrel and Endcap:
  - Accordion shape
  - Pb absorber and Cu electrode

- Hadronic Endcap (HEC)
  - Plates
  - Cu absorber and electrode

- Forward calorimeter
  - Rod matrix
  - EM Layer Fcal1: Cu
  - Hadronic Layers FCal2,3: W





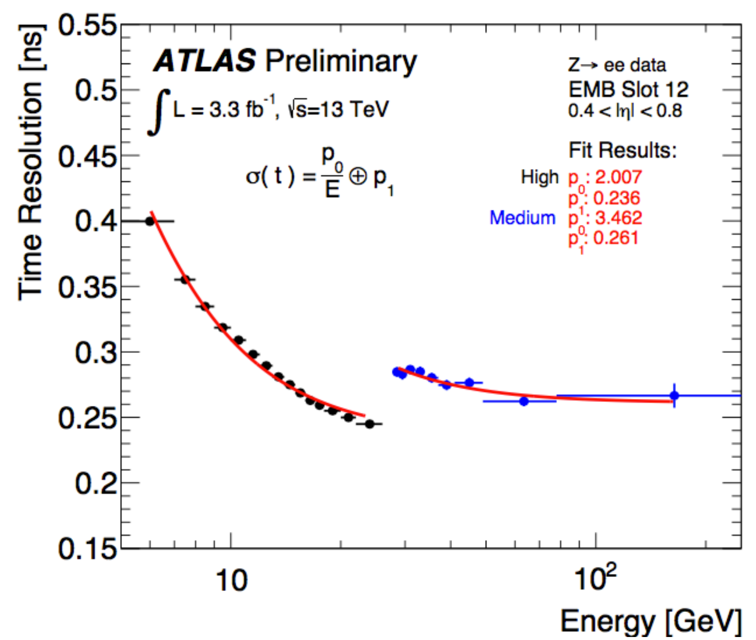


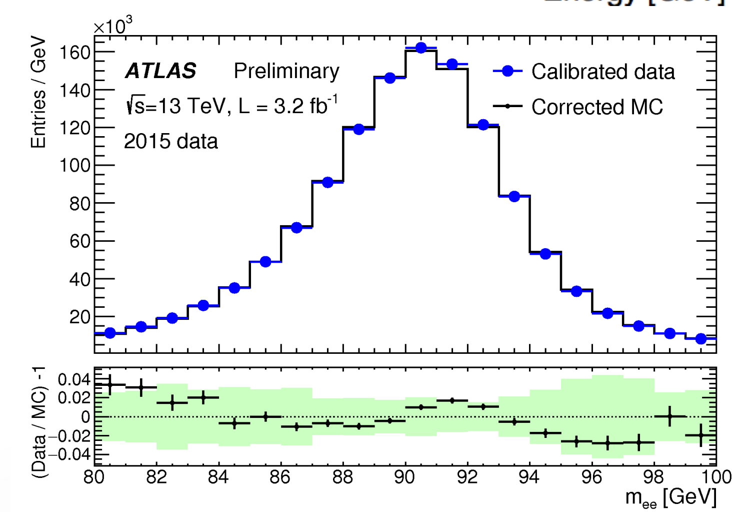
LAr performances in Run II

- Operational performances:

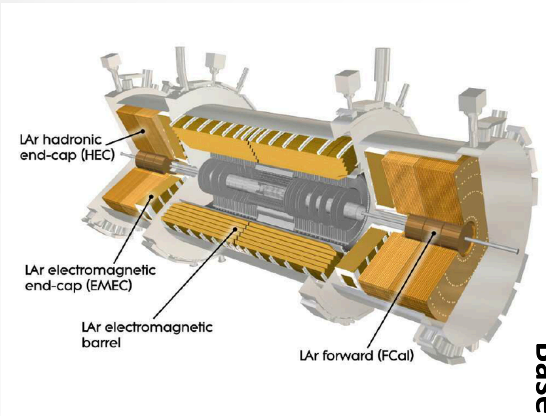
  More than 99.6% of operational channels, >99% of data with good quality in 2016

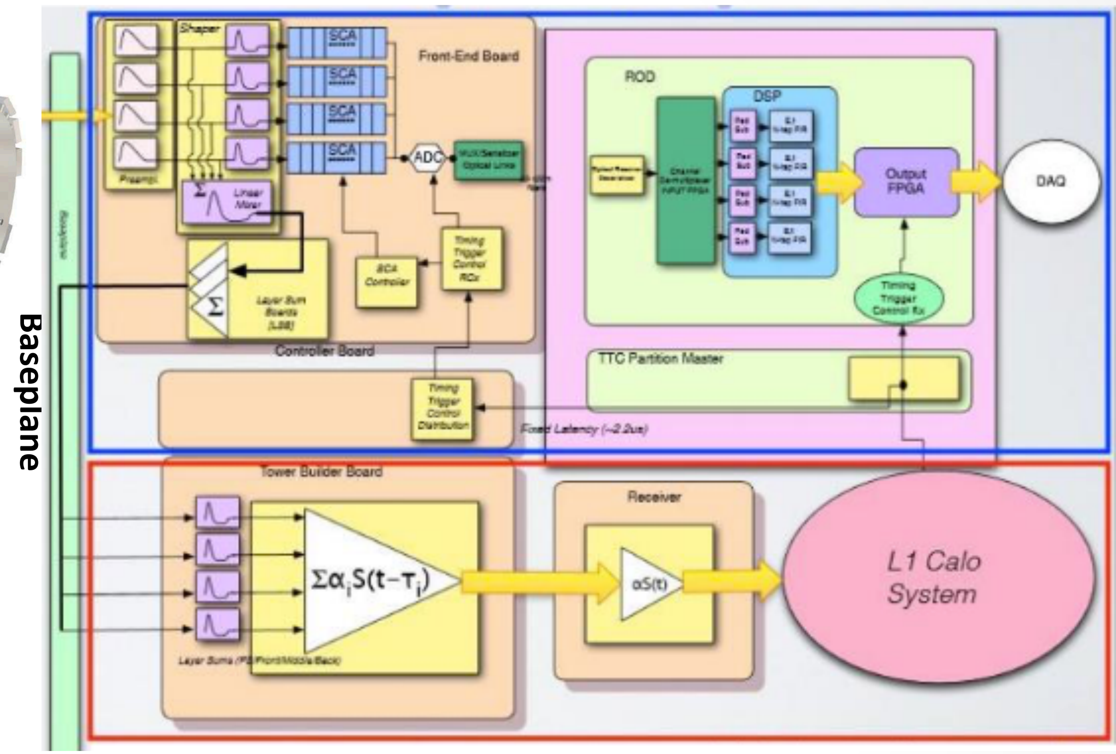
- EM scale and particle reconstruction:
  - Data corrected from non-uniformities and Data/Simulation corrections
  - Energy scale and electron/photon identifications controlled with J/ψ and Z events





LAr current readout



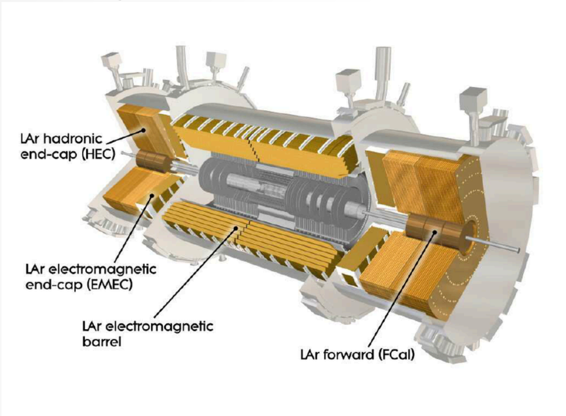


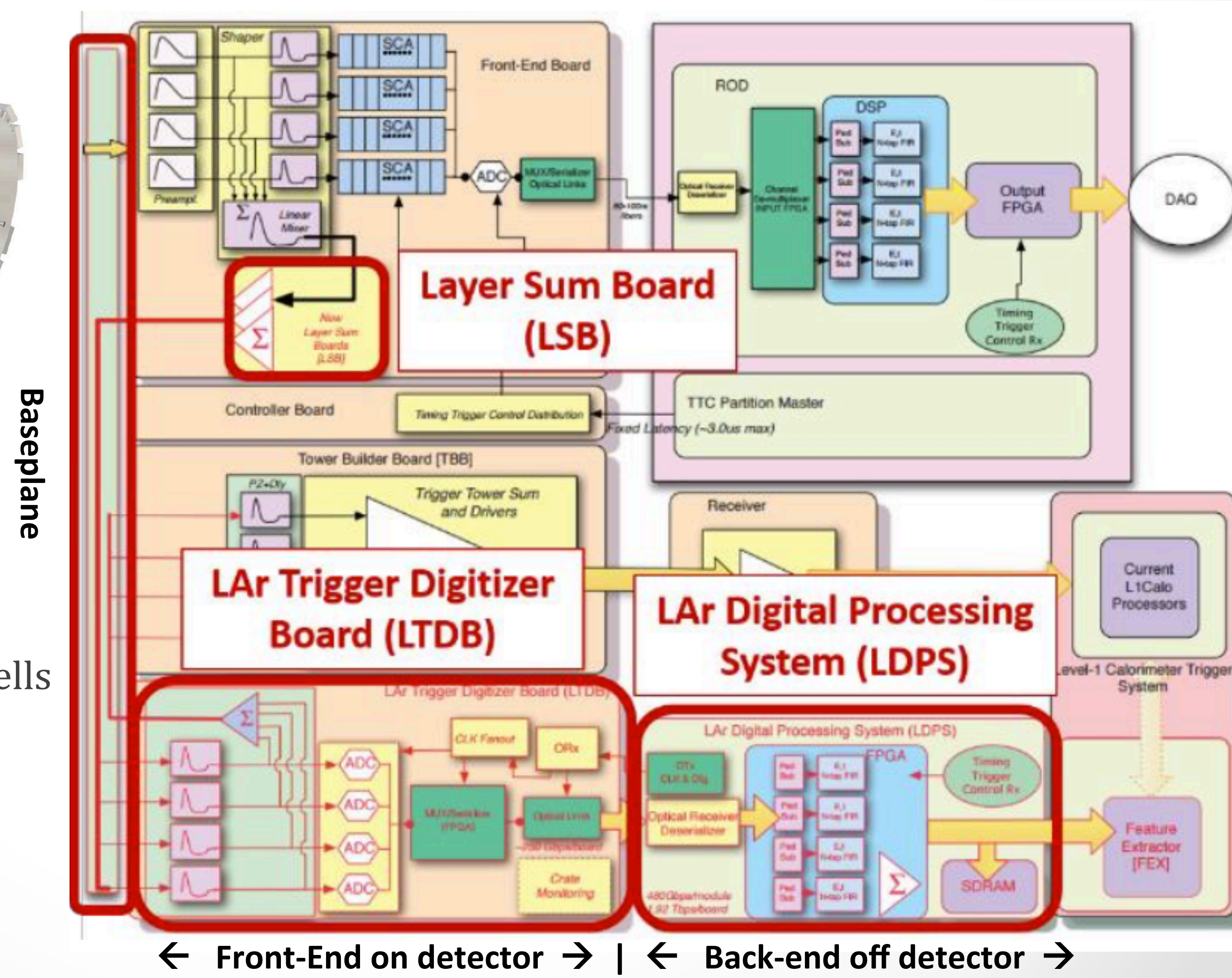
← Front-End on detector → | ← Back-end off detector →

- Cells signals are amplified, shaped, sampled, digitized at 40MHz
- Data are transmitted at 100 kHz upon level-1 trigger
- Layer Sum Board (LSB) perform signal summing
- Tower Builder Board (TBB) form Trigger Towers

LAr readout upgrade

Readout architecture: signal from all LAr channels will be digitized at 40MHz and fully processed in the back-end





New LSB: Phase-I

Analog Sum of Super Cells

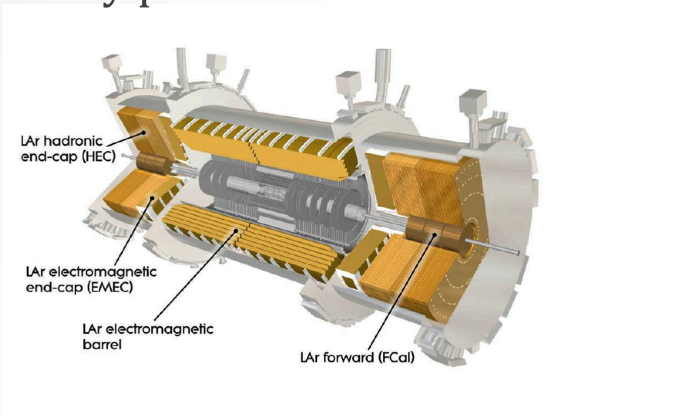
New LTDB: Phase-I

124 LTDB process 34k supercells

TBB: backup in Phase-I

LAr readout upgrade

Readout architecture: signal from all LAr channels will be digitized at 40MHz and fully processed in the back-end



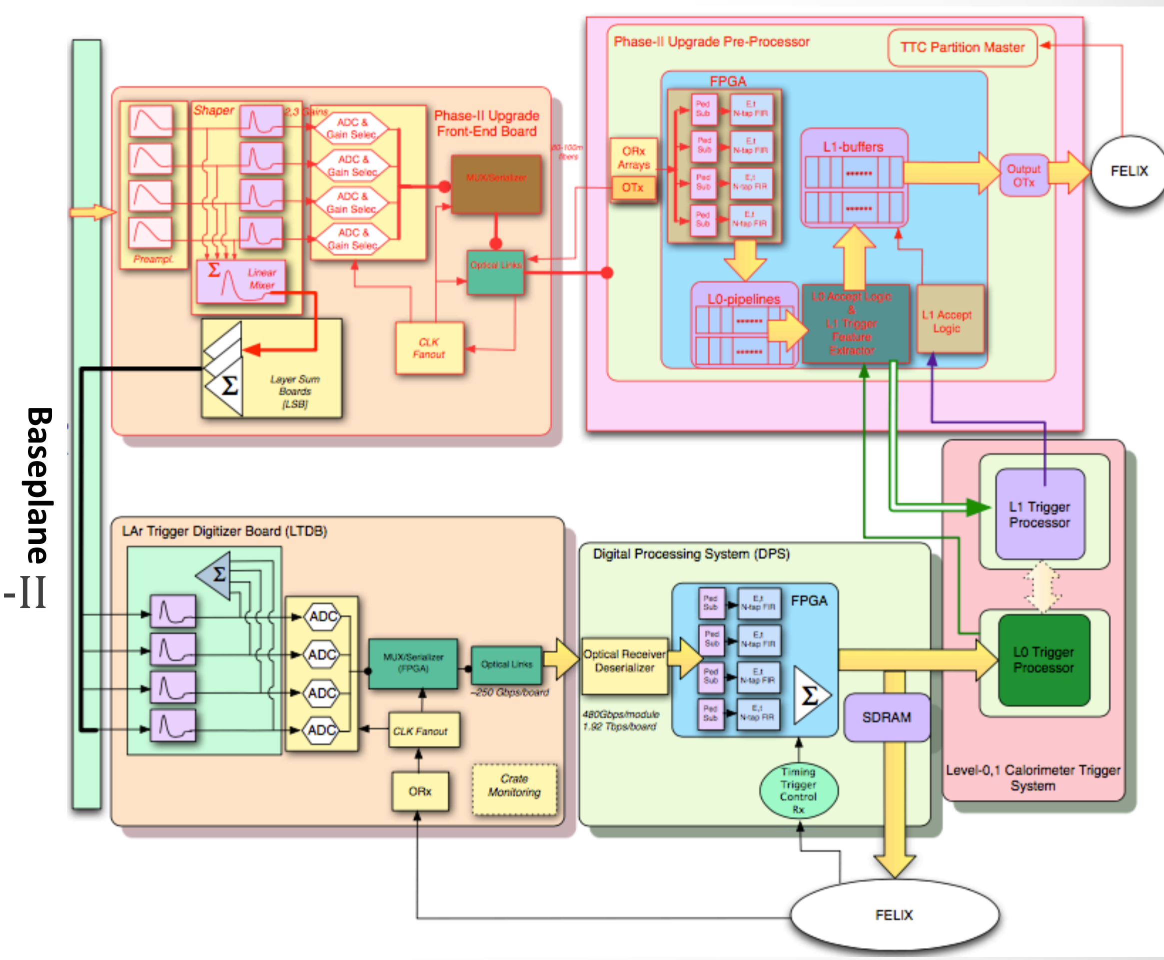
New LSB: Phase-I kept in Phase-II

New LTDB: Phase-I kept in Phase-II

TBB: removed in Phase-II

Controller Board: removed in Phase-II

Front-End Boards upgraded for Phase-II



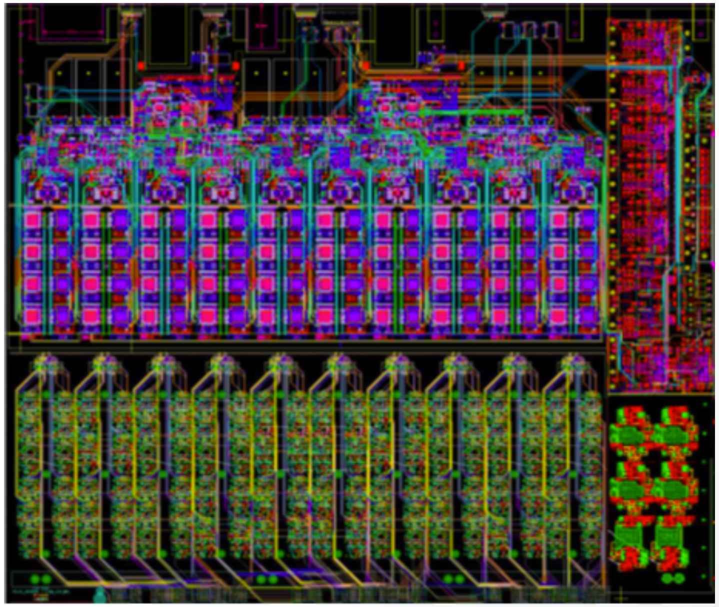
← **Front-End on detector** → | ← **Back-end off detector** →

LAr readout upgrade

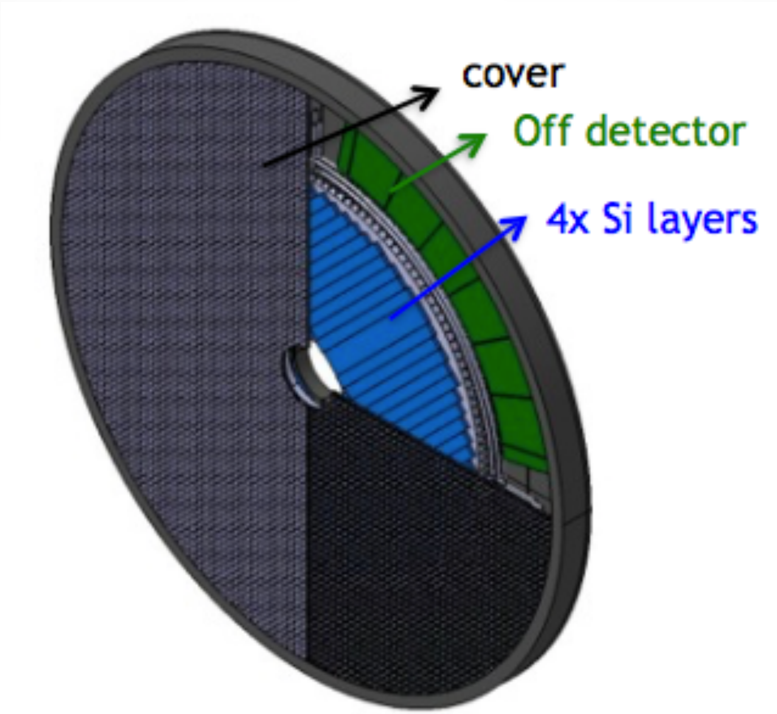
- **Front-end:** FEB pipeline restricts L1 rate to 100 kHz, latency 3μs → new readout adapted to Phase-II TDAQ requirements:
  - L0 rate 1MHz – latency 10μs
  - L1 rate 400kHz – latency 60μs

- Digitize at 40 MHz and read out full granularity, to maximize info provided to trigger → **new ASICs**
  - Preamp & Shaper ADC
  - 10 Gbps Serializer
  - Tolerant to high radiation doses

- **Back-end:** high performance FPGAs with large bandwidth



Phase-I LTDB prototype



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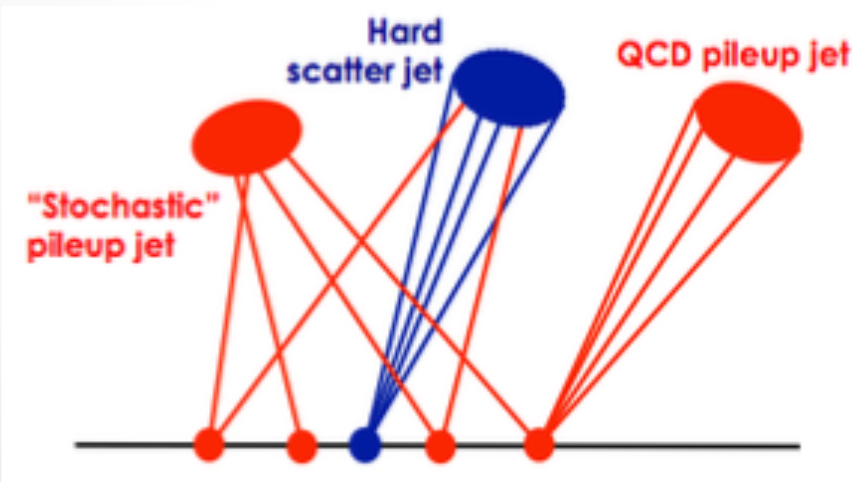
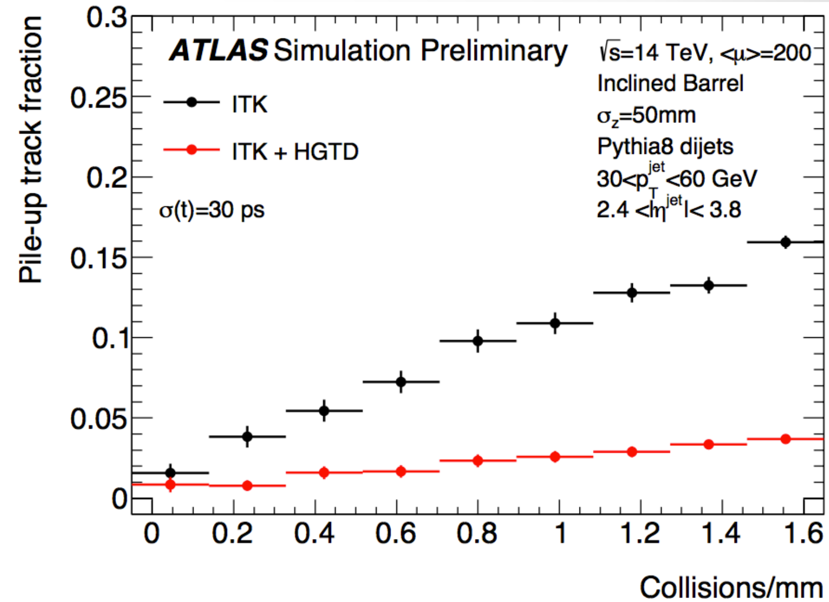
High Granularity Timing Detector (HGTD)

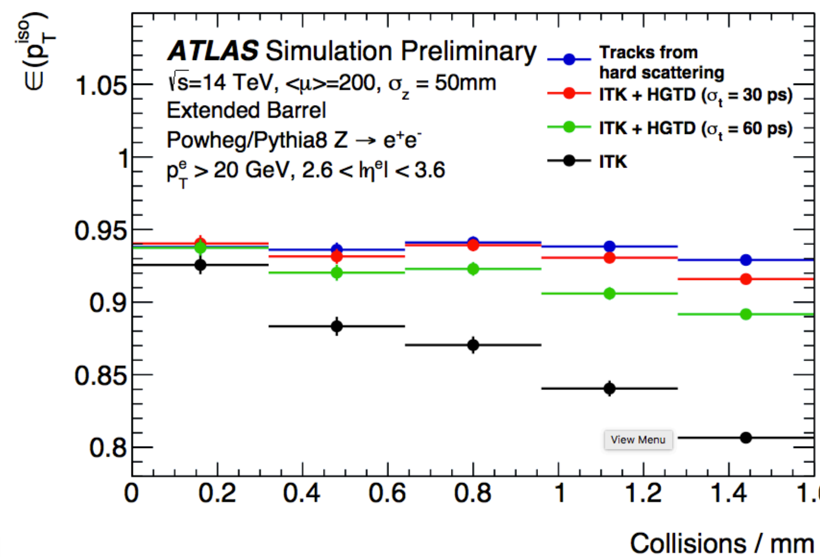
A potentially new sub-detector for phase 2 upgrades

High Granularity Timing Detector (HGTD)

- Extended tracking coverage in ATLAS up to $|\eta|=4.0$
- Adds to each track a time information
- Time information allows track to vertex assignements:
  - Improve lepton and photon isolation
  - Suppress PileUp jets
- Targets of 30 ps time resolution

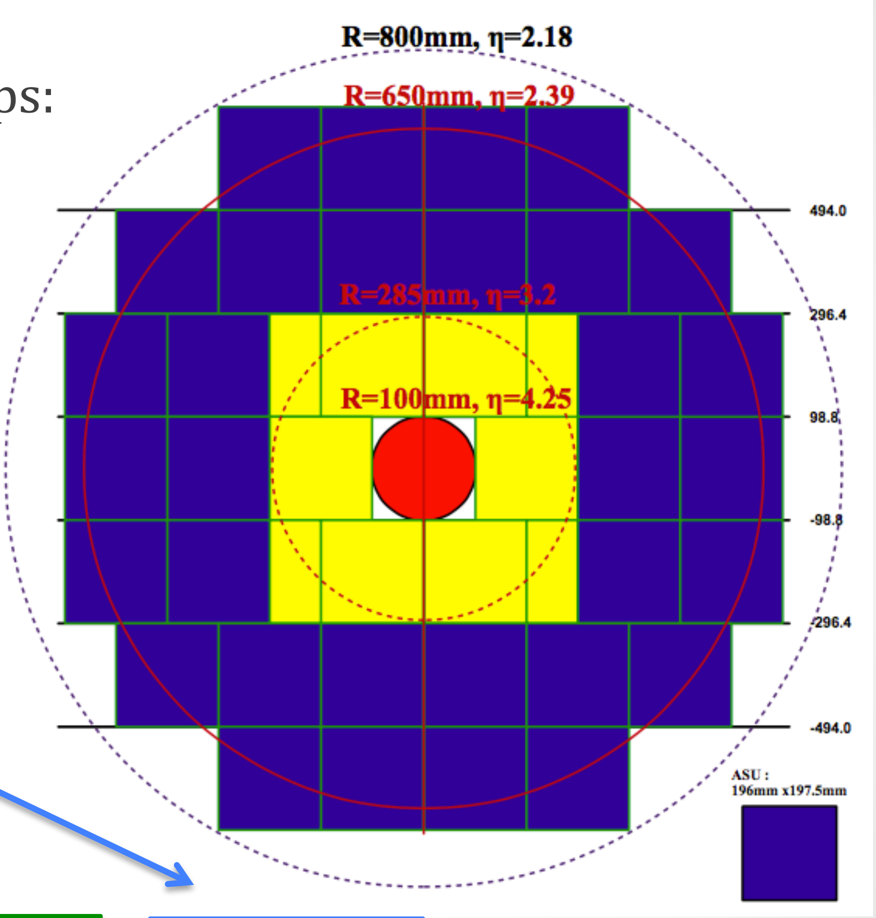






HGTD Design

- To be installed in front of the LAr end-caps:
  - 65 mm thick, $2.4 < |\eta| < 4.2$
  - Envelope 110 mm – 1045 mm radius
  - Sensitive region: 120 mm – 650 mm radius
  - 4 layers

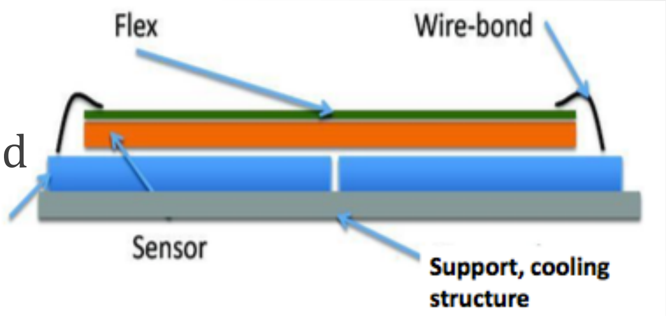


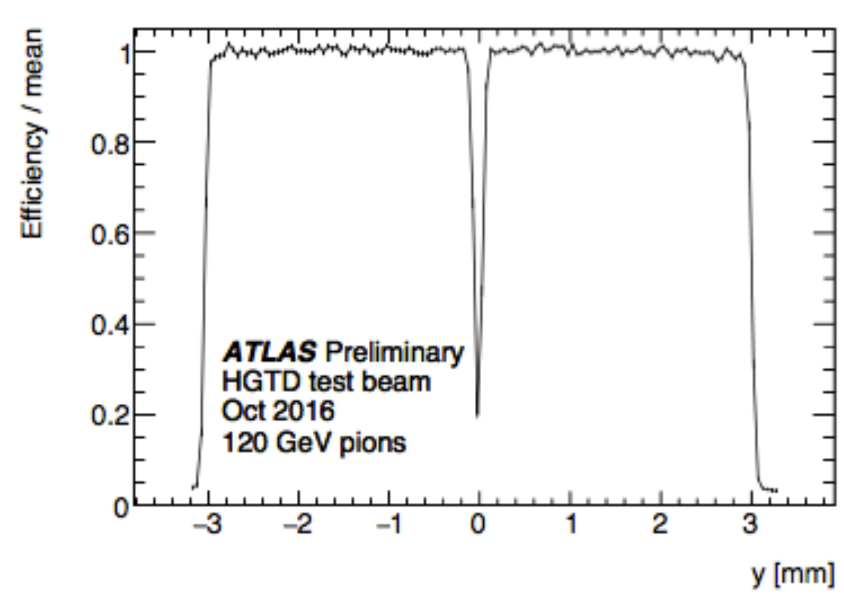
- Active elements:
  - Use of Low gain avalanche diodes
  - Time resolution of 30-50 ps achieved by optimising thickness, signal shape, electronics

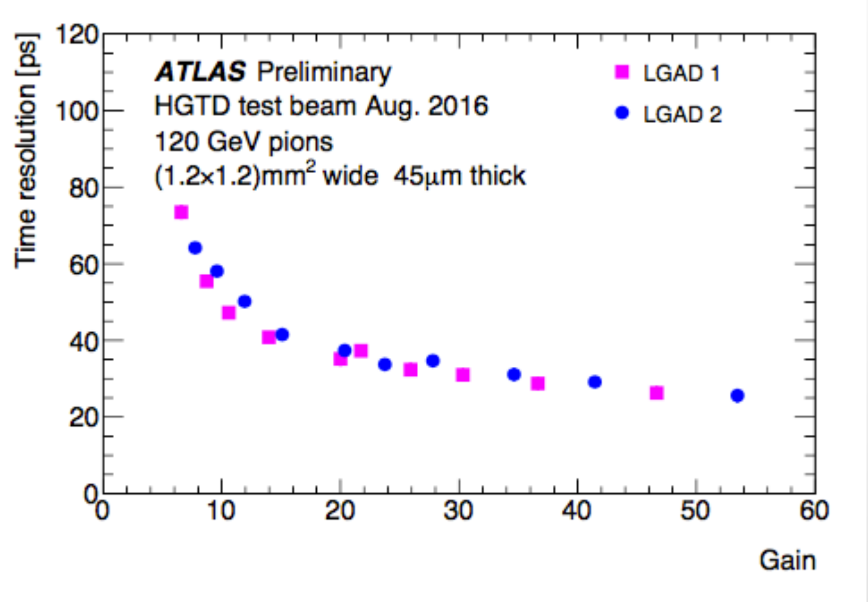
$$\sigma_{tot}^2 = \sigma_{Landau}^2 + \left(\frac{t_{rise}}{S/N}\right)^2 + \left(\left[\frac{V_{thr}}{S/t_{rise}}\right]_{RMS}\right)^2 + \left(\frac{\mathrm{TDC}_{bin}}{\sqrt{12}}\right)^2$$

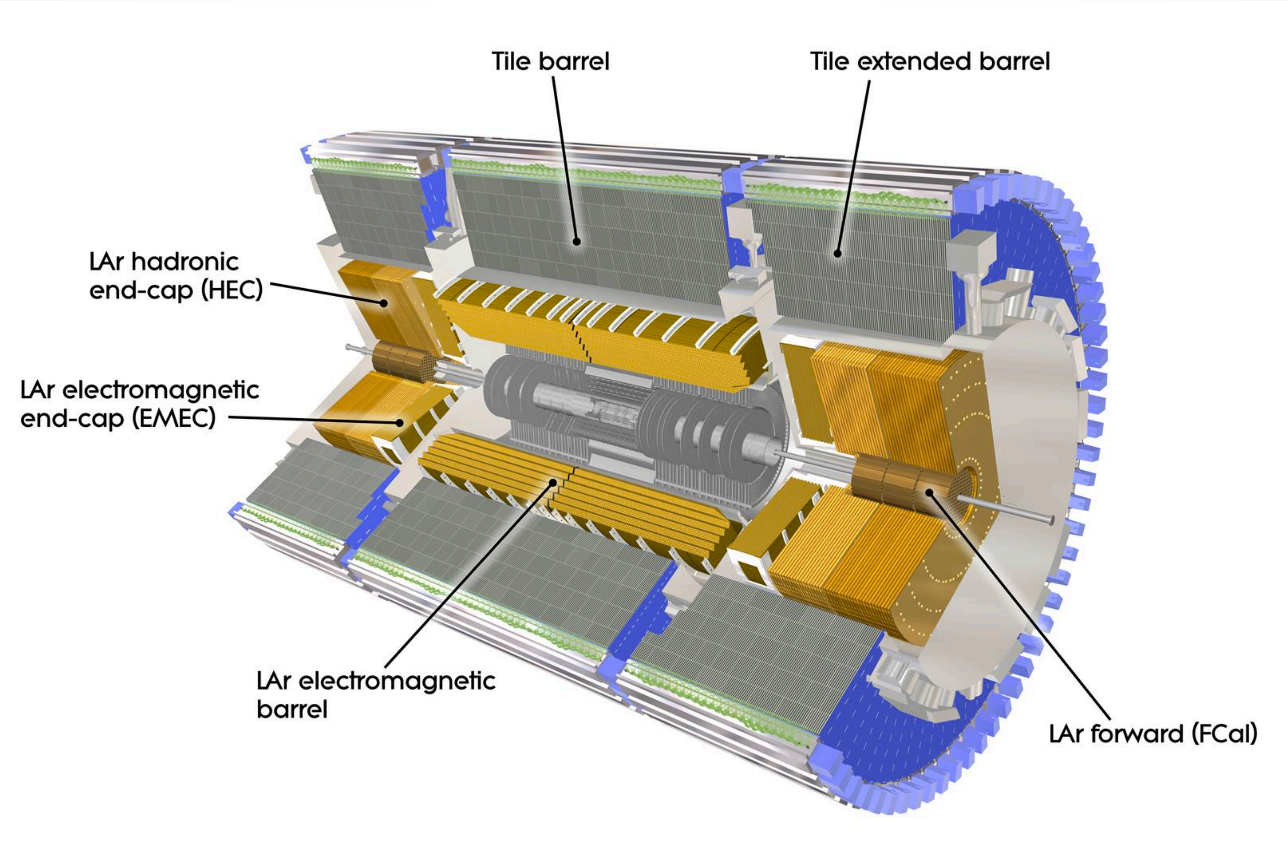
HGTD performances

- Performances validated in Test beam campaigns in August and September 2016
- Use of 2x4 cm sensors array of sensors bump-bonded to ASICs prototype
- Good Efficiency and uniformity
- Occupancy < 10% → pads of 1.3x1.3 mm^2









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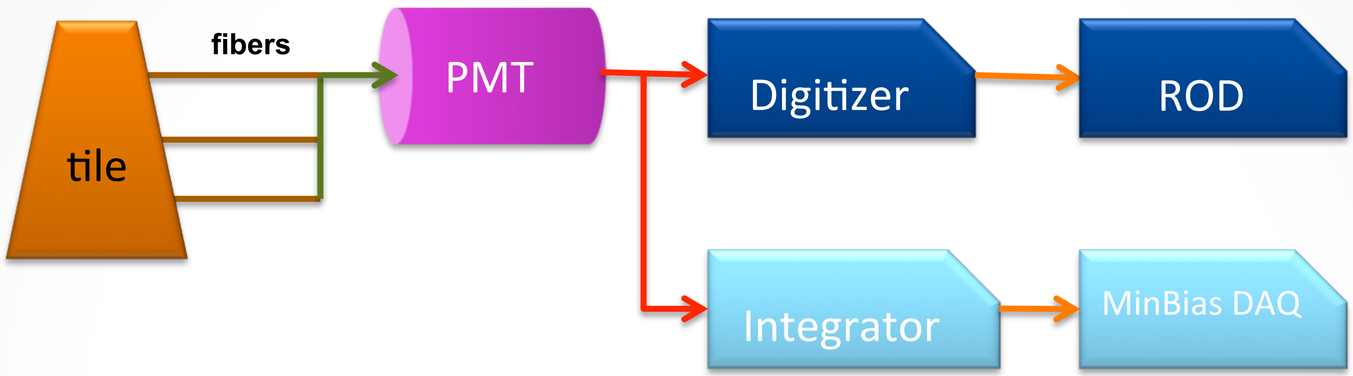
The Tile Calorimeter

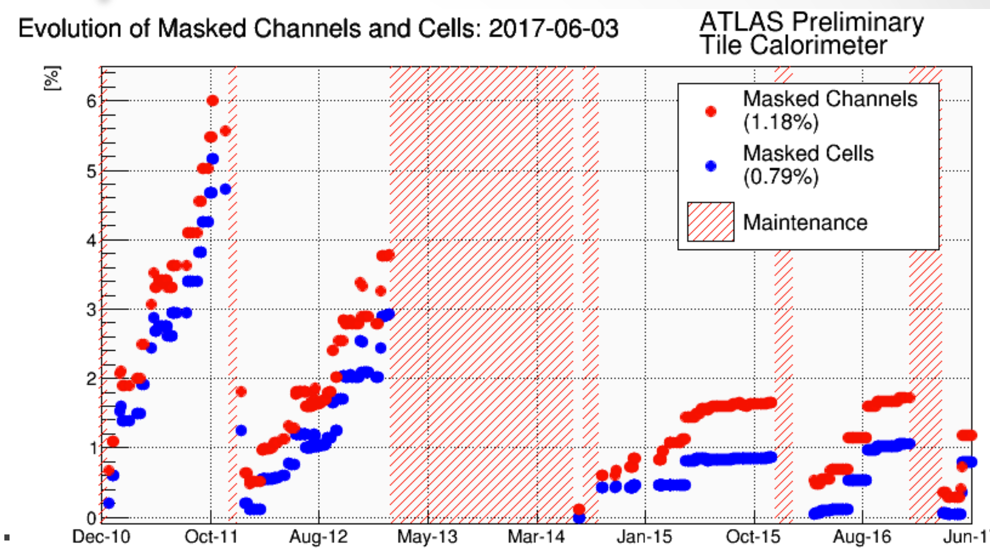
Signal readout in TileCal



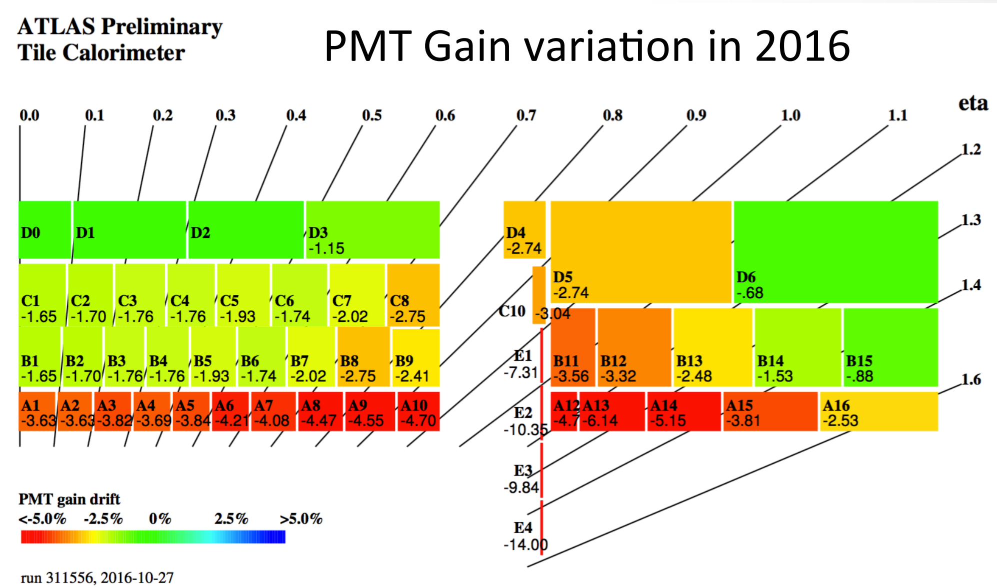
- Light produced in scintillating **tiles** is converted into electric currents by the **PMTs**
- Phase 0:
  - The signal from the PMTs is shaped and amplified using two gains (with a ratio of 1:64) with a 10-bit **ADC**
  - Signals are sampled and digitized at 40MHz
  - For L1 events only (40 kHz) → Digitized signals are collected and processed by the RODs (Read-Out Drivers)
  - On-detector electronics designed to output digital data at the maximum rate of **100 kHz**. The digital data is stored on detector in a 2.5 μs-long pipeline

TileCal Run 2 performances

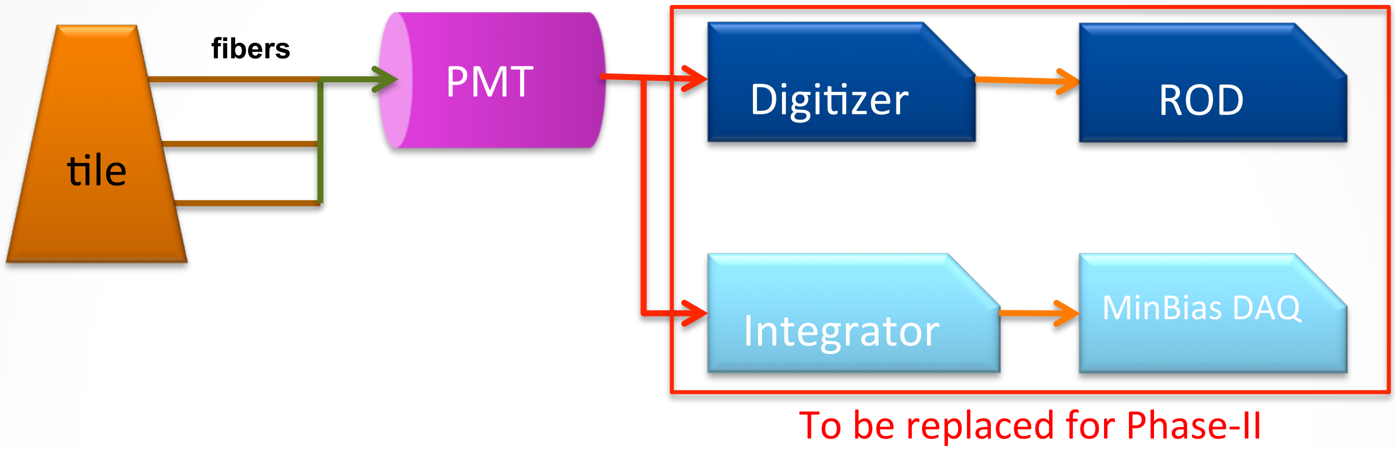
- TileCal was monitored during LHC Run 2: less than 1% of masked cells at end of 2016



- TileCal elements were calibrated:
  - Electronics with Charge Injection System
  - PMTs with Laser system
  - Optics with Minimum Bias event
  - Energy scale maintained with Cesium calibration



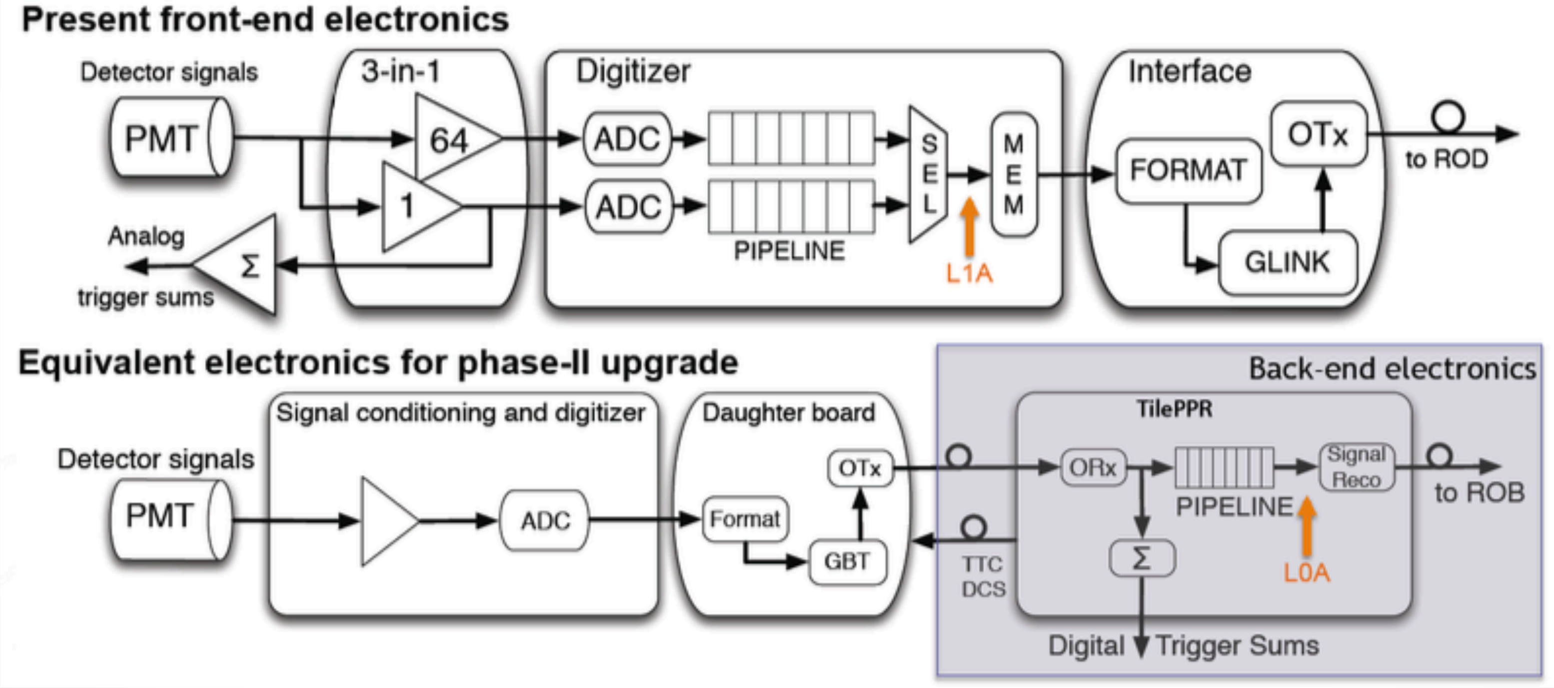
Components to be upgraded in TileCal



- Robust elements: scintillators, PMTs and fibres to be kept in LHC Phase-II
- The readout electronics has to be replaced for LHC Phase-II:
  - Present digital readout is not compatible with the HL-LHC architecture
  - Ageing of some elements due to time or radiations
  - To provide full-granularity digital data to the Level-0/1 triggers at 40 MHz
- Update HV distribution over PMT dynodes
- Remote HV supply
- Update the mechanics of drawer

TileCal readout upgrade

- **Readout architecture:** data will be pipelined and processed in the off-detector pre-processor boards.



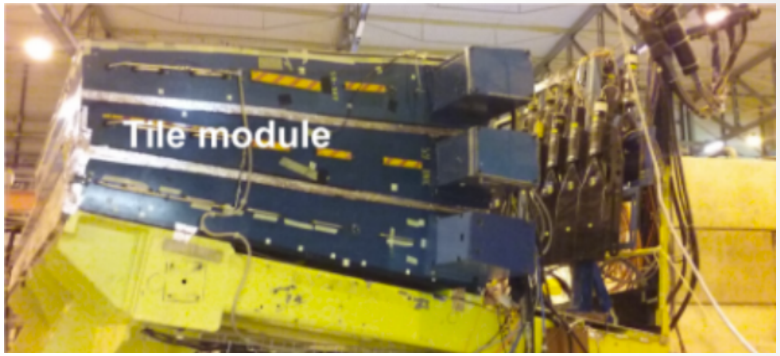
- **Front-end:** for each pulse, digitization provides a time and a total charge (energy). Two upgraded front-end technologies proposed:
  - **"3 in 1"** → optimized version of the current digitization based on discrete components. Compatible with current analog trigger.
  - **FATALIC** → New technology, implemented in an ASIC performing shaping & digitization

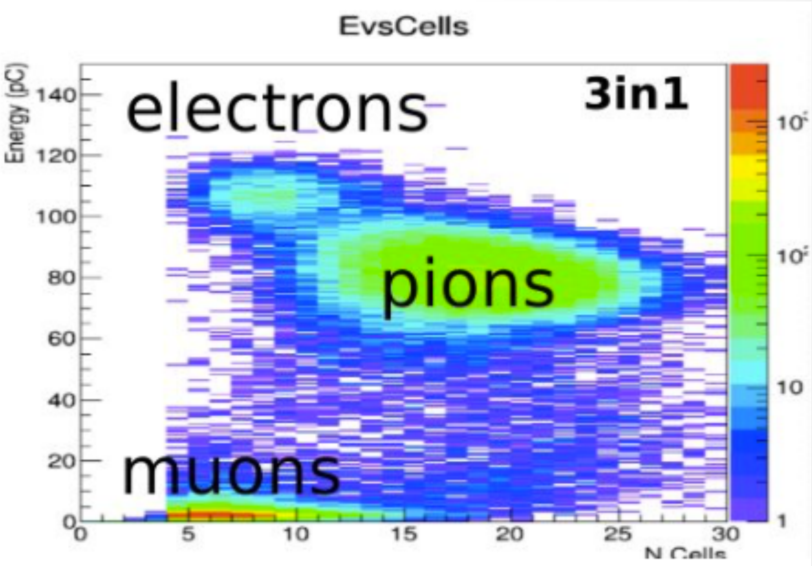
Testbeam validation of TileCal upgrade

- **Testbeam campaigns** in 2016 and 2017

- 3 TileCal modules equipped with Phase-II upgrade electronics together with modules equipped with the current system were exposed to different particles and energies.

- Options being validated in terms of:
  - Linearity, noise
  - Signal shaping





Conclusion

- The Liquid Argon and Tile calorimeters in ATLAS showed excellent performances during the LHC Runs I and II

- Calorimeters will be adapted to HL-LHC environment :
  - New TDAQ architecture
  - High PU

- Liquid Argon Calorimeters and TileCal will use an upgraded readout

- A High Granularity Timing Detector has been proposed to complete tracking information and reduce the impact of PU on e/γ reconstructions and forward jets

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Additional Material

FCAL in LHC Phase-II

- At high luminosity, high η, degradations expected due to:
  - Ar^+ build-up
  - high currents
  - temperature increase

- Keeping same FCAL configuration for LHC Phase-II:
  - Compensate signal degradation due to Ar^+
  - studies done at software and calibration level