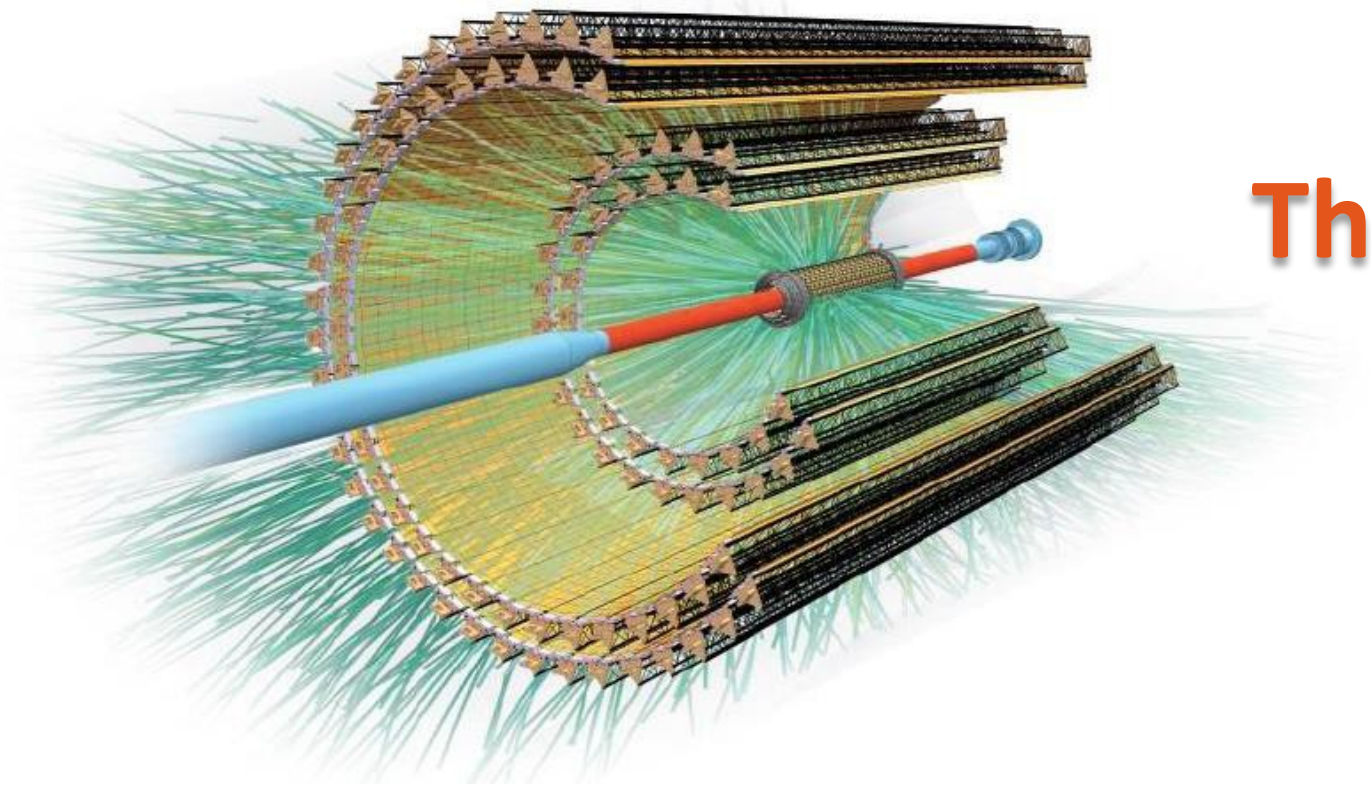


The ALICE ITS UPGRADE

Paolo Camerini

Università degli Studi di Trieste & INFN

on behalf of the ALICE collaboration

UNIVERSITÀ DEGLI STUDI DI TRIESTE

INFN

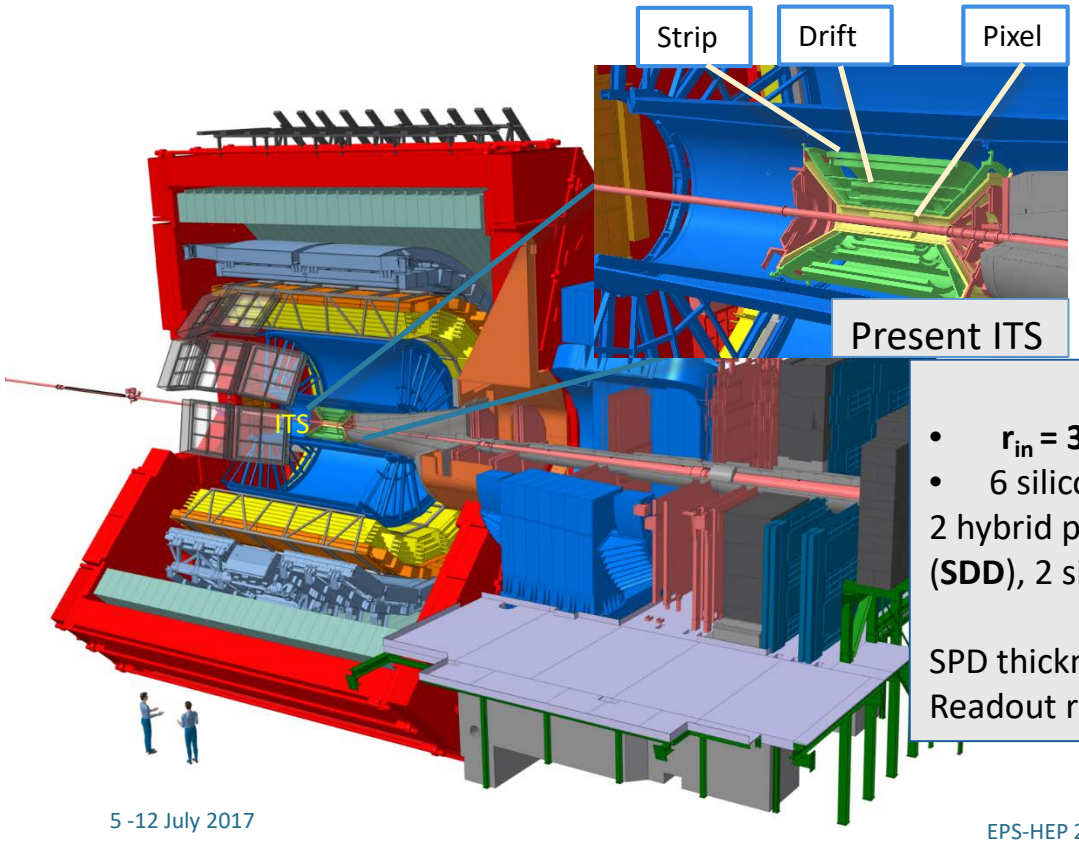
ALICE

ALICE UPGRADE

Major upgrade of ALICE forseen during Long Shutdown 2 (2019/20)
Expected Run3&4 Pb-Pb luminosity 6×10^{27} cm^{-2}s^{-1} (10nb^{-1} integrated, factor 100 gain in statistics wrt Run1-2)

Physics Goal: Study of Quark Gluon Plasma properties via high-precision measurements of rare probes

- identification of secondary vertex of short lived particles @ low p_T
- large minimum bias data sample needed (no hardware trigger possible)



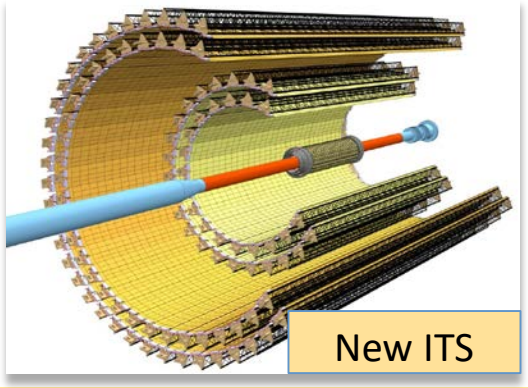
Present ITS

- r_{in} = **3.9 cm** r_{out} = **43 cm**
- 6 silicon detector layers:

2 hybrid pixel (**SPD**), 2 silicon drift (**SDD**), 2 silicon strip (**SSD**)

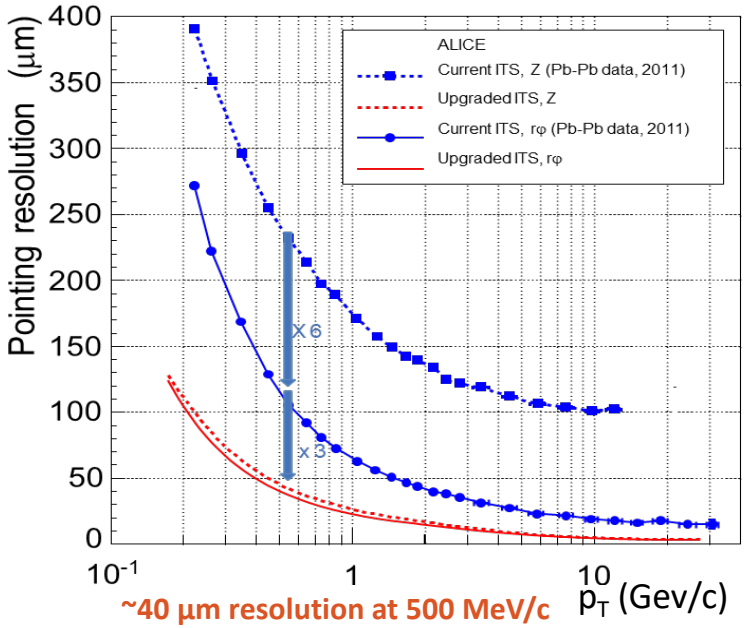
SPD thickness (X/X_0): **1.14**%/layer
Readout rate: ~**1kHz**

To cope with the increased luminosity and improve the tracking performances, several upgrades planned: new Inner Tracking System, new Muon Forward Tracker, TPC, Readout electronics, Trigger, Online/Offline

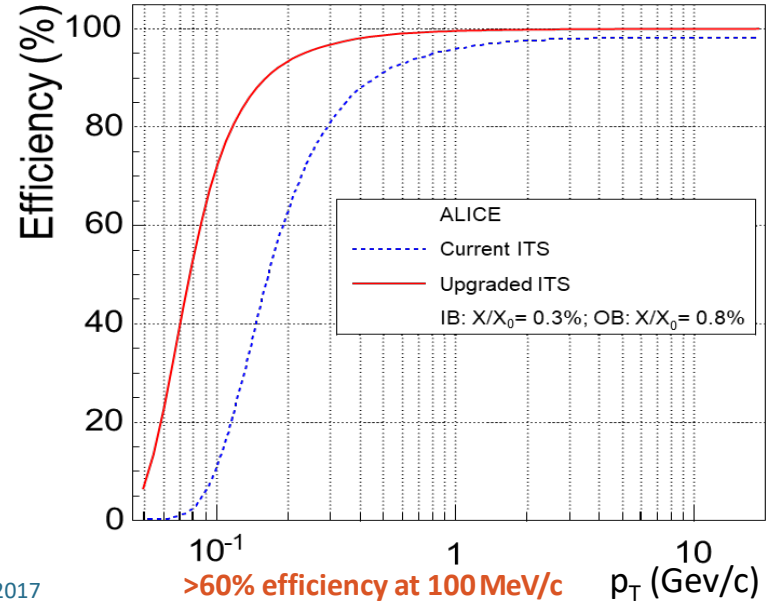


Major Upgrade of the
Inner Tracking System to improve low p_T tracking and data rate performances

ITS UPGRADE KEY REQUIREMENTS



~40 μm resolution at 500 MeV/c



>60% efficiency at 100 MeV/c

Improve impact parameter resolution

- Get closer to IP: 1st layer 39 mm → 23 mm (new beam pipe)
- Reduce material budget: 1.14% X_0 → 0.3% X_0 (Inner Barrel stave)
  Constraints on chip thickness, power density, support structures
- Reduce pixel size: 50 μm x 425 μm → O(30 μm x 30 μm)

Improve low pT resolution and tracking efficiency

- Pixel, drift, strip detectors → pixel detector
- 6 layers → 7 pixel layers

Improve readout to exploit increased luminosity

- Interactions readout rate (2x LHC expected interaction rate):
  Pb-Pb ~100kHz, minimum bias

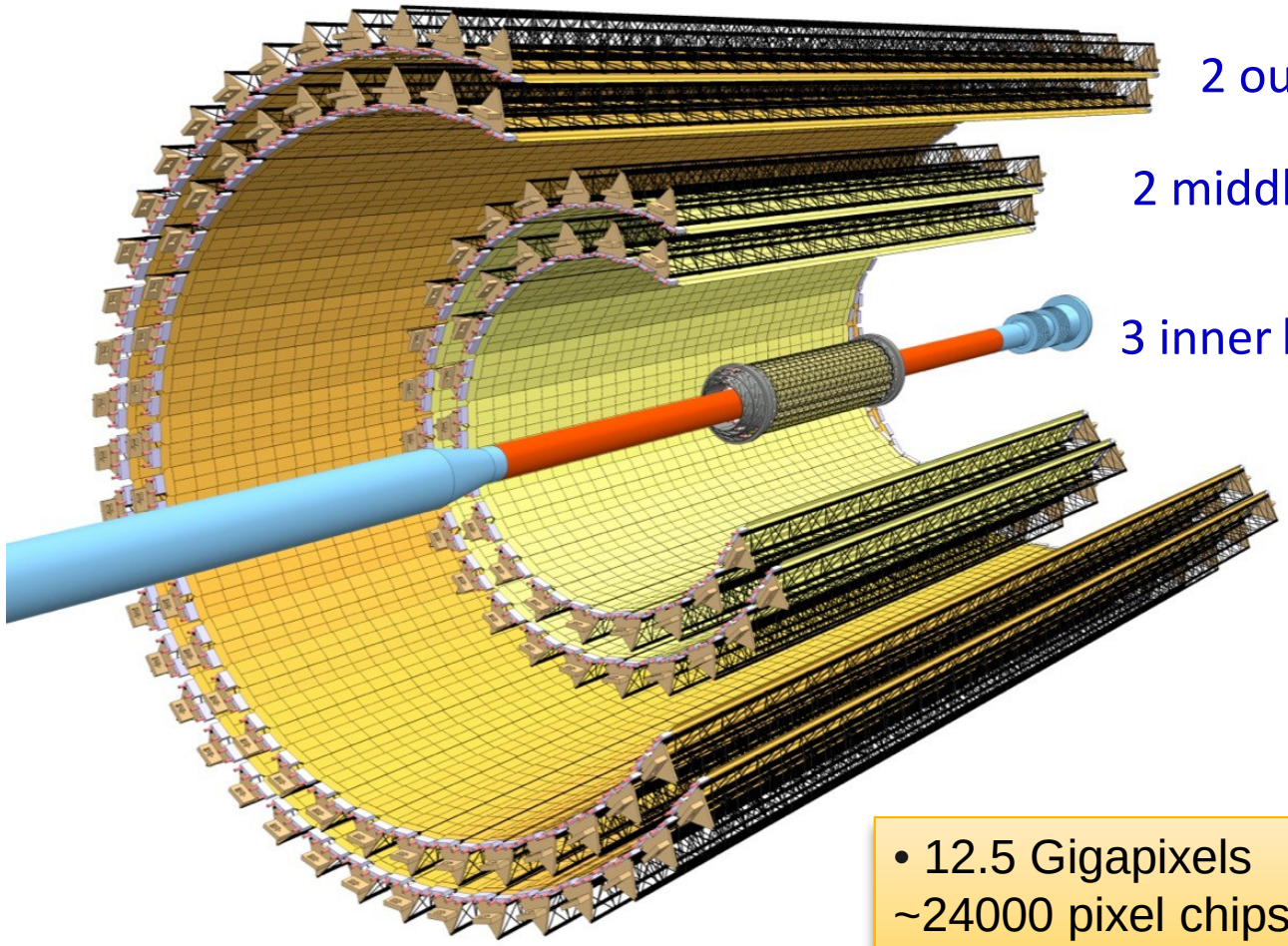
Capability of fast insertion and removal during end of year shutdown

- possibility to replace non-functioning detector modules

Expected radiation load (10 yrs + safety factor, innermost layer):

- TID: ~ 2.7 Mrad; NIEL: ~1.7×10^{13} 1MeV n_{eq} / cm^2

INNER TRACKING SYSTEM UPGRADE LAYOUT



2 outer layers (90 staves)
2 middle layers (54 staves)
} Outer Barrel (OB)

3 inner layers (48 staves) Inner Barrel (IB)

7-layer barrel geometry equipped with Monolithic Active Pixel Sensors

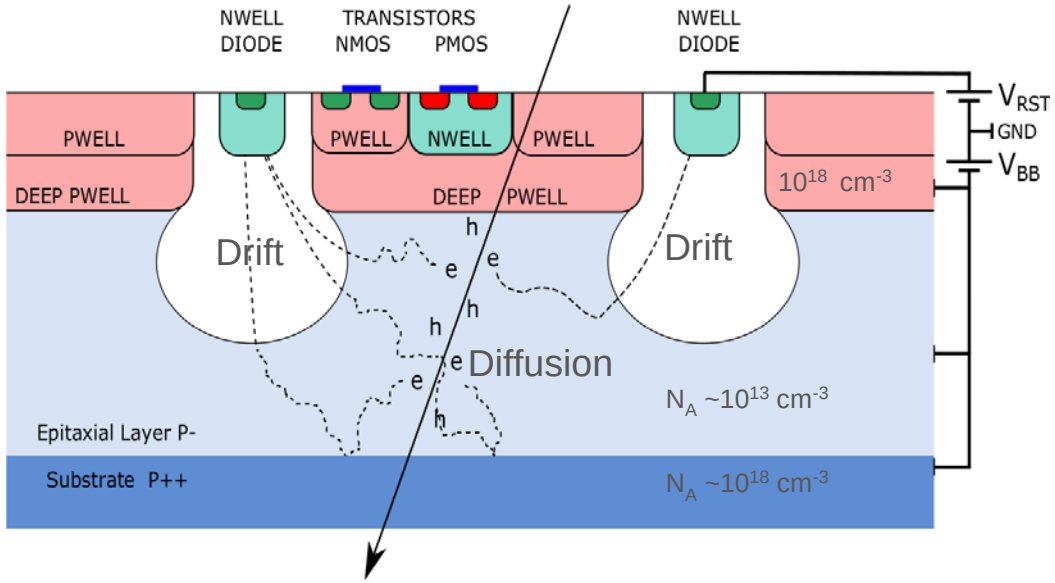
- 12.5 Gigapixels
~24000 pixel chips
- binary readout
- ~ 10 m^2 active area
η coverage: $|\eta| \leq 1.22$

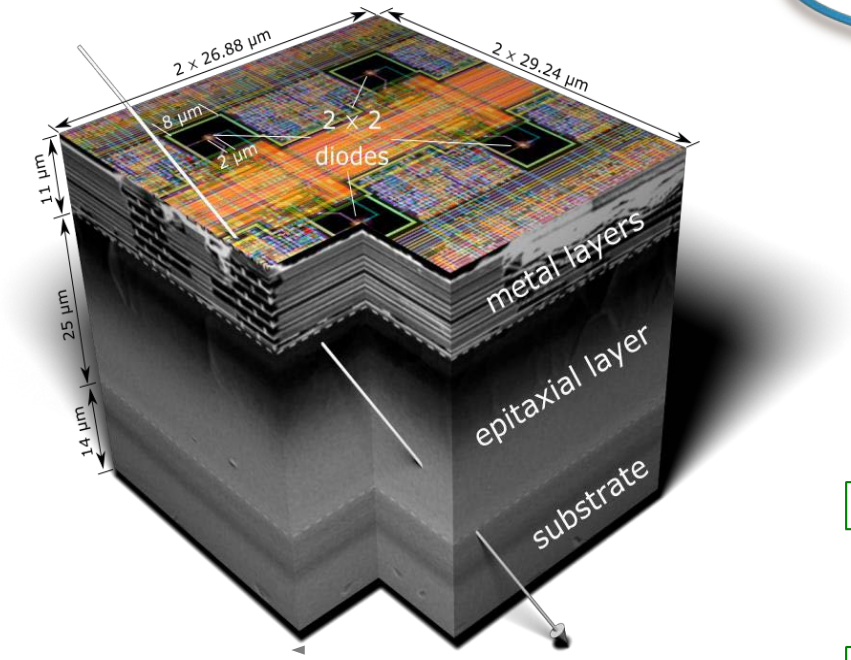
IB **Radius** (mm) ~ **23**, 31, 39
IB stave **length** (mm): ~290

OB **Radius** (mm): ~196, 245, 344**, 393**
Middle layers stave **length** (mm): ~900
Outer layers, stave **length** (mm): ~1500

ALPIDE: THE MONOLITHIC ACTIVE PIXEL SENSOR

Pixel Sensor produced using TowerJazz 0.18µm CMOS Imaging Process



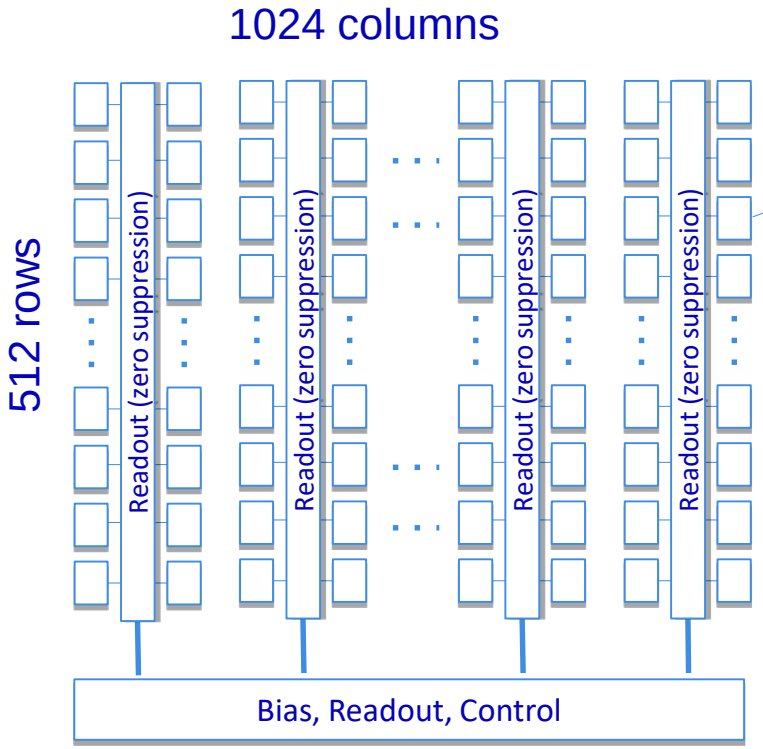


Pixel sensor R&D

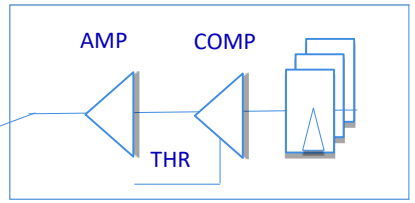
- 2012 — Explorer analogue
- 2013 — pALPIDEss-0 digital
- May-2014 — pALPIDE-1 Full scale
- May-2015 — pALPIDE-2 Full scale
- Oct-2015 — pALPIDE-3 Full scale
- Aug-2016 — **ALPIDE final**

- Deep Pwell allows in-pixel full CMOS (complex in-pixel circuitry without charge loss).
  - Key to enable low-power read-out.
  - High granularity, low material budget (~1/7 w.r.t. present ITS pixel chip)
- Resistivity (>1 kΩ·cm) p-type epitaxial layer (25 µm);
- Possibility of reverse biasing

ALPIDE: THE MONOLITHIC ACTIVE PIXEL SENSOR



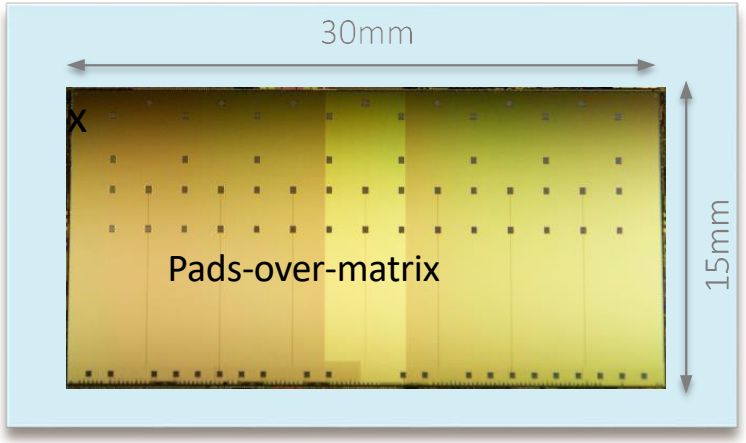
In pixel:



- Amplification
- Discrimination
- multi-event buffer

Chip size:
30 mm x 15 mm

Pixel size:
27 μm x 29 μm



10

- In matrix zero suppression.
- Triggered or continuous readout
- Connects directly to 5-m away off-detector electronics via high speed link

Parameter	Inner Barrel	Outer Barrel	ALPIDE
Silicon thickness	50μm	100μm	OK
Spatial resolution	5μm	10μm	~ 5μm
Chip dimension	15mm x 30mm		OK
Power density	< 300mW/cm^2	< 100mW/cm^2	< 40mW/cm^2
Event-time resolution	< 30μs		~ 2μs
Detection efficiency	> 99%		OK
Fake-hit rate *	< 10^{-6}/event/pixel		< 10^{-10}/event/pixel
NIEL radiation tolerance **	1.7x10^{13} 1MeV n_{eq}/cm^2	10^{12} 1MeV n_{eq}/cm^2	OK
TID radiation tolerance **	2.7Mrad	100krad	tested at 500krad

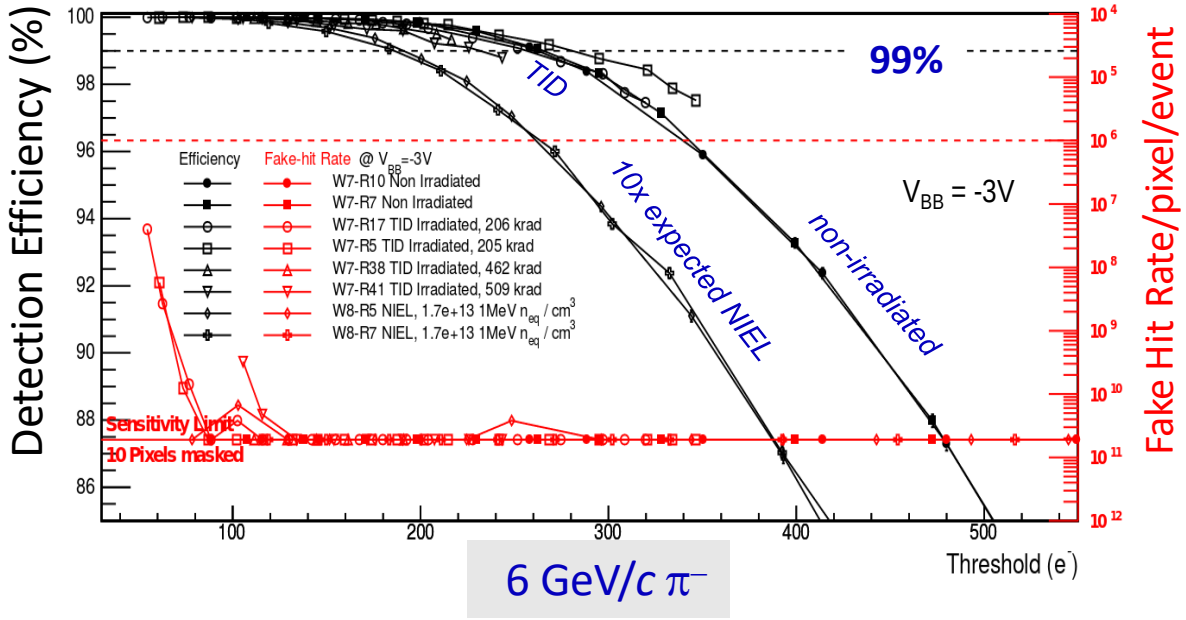
* revised numbers w.r.t. TDR

** including a safety factor of 10, revised numbers w.r.t. TDR

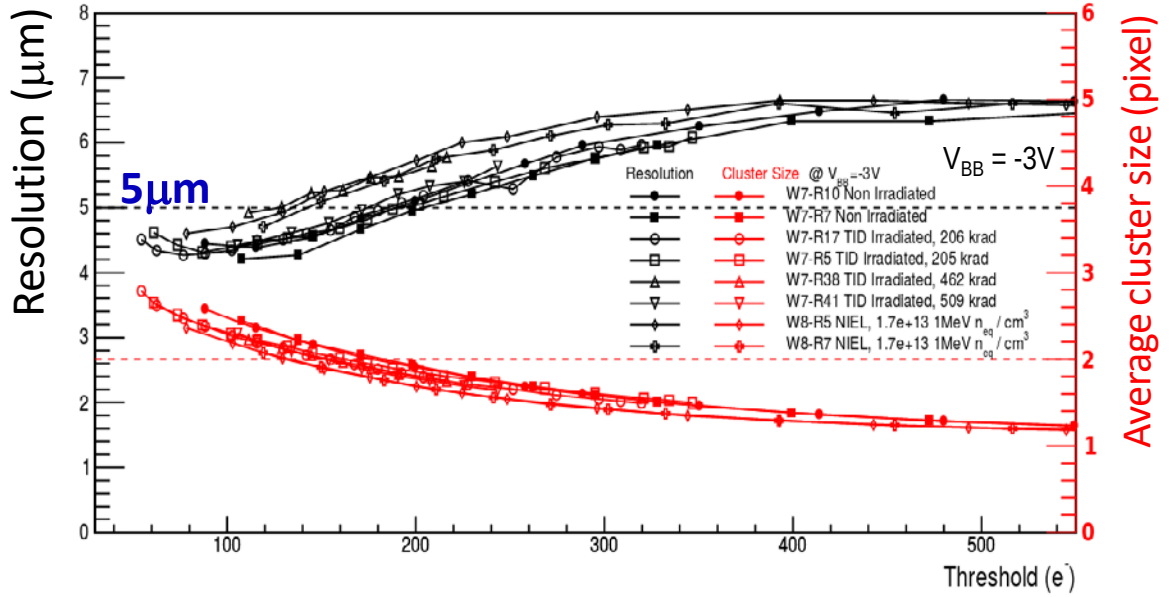
ALPIDE PROTOTYPES: TESTS AND QUALIFICATION

Extensive chip qualification campaign of laboratory and test beam measurements on irradiated and non irradiated sensors:

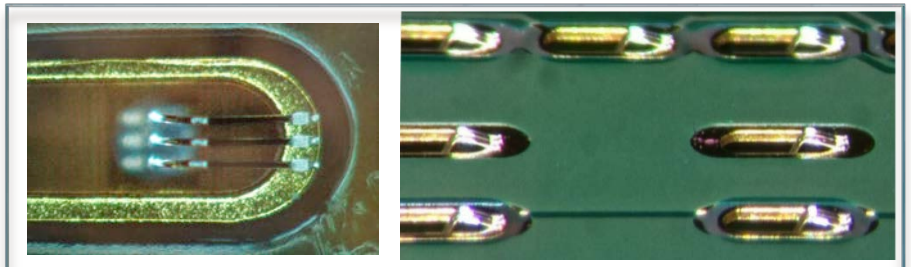
- fake-hit rate < 10^{-10} /pixel/event (10^{-6}required)
  → Big operational margin (only 10 masked pixels)
- Negligible chip-to-chip fluctuations
- Sufficient operational margin after 10x lifetime NIEL dose
- efficiency >99% up to ~200 electrons threshold
- Resolution of about 5µm @ threshold of 200 electrons
- **NIEL irradiated chips show no significant degradation of operation margins**



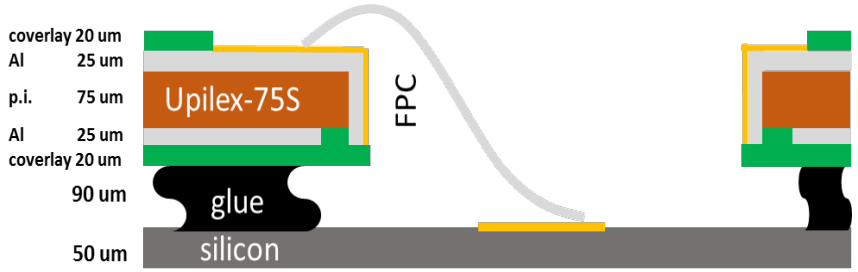
6 GeV/c π^-



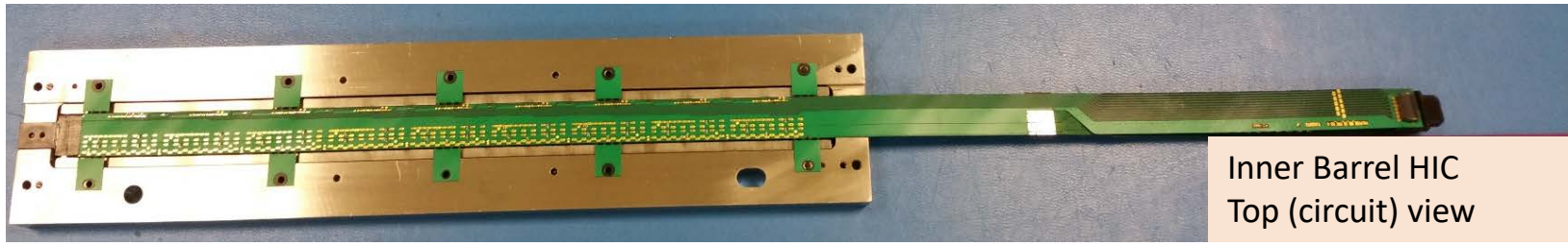
ITS-UPGRADE HIBRID INTEGRATED CIRCUIT



FPC to Chip interconnection



IB HIC cross section scheme

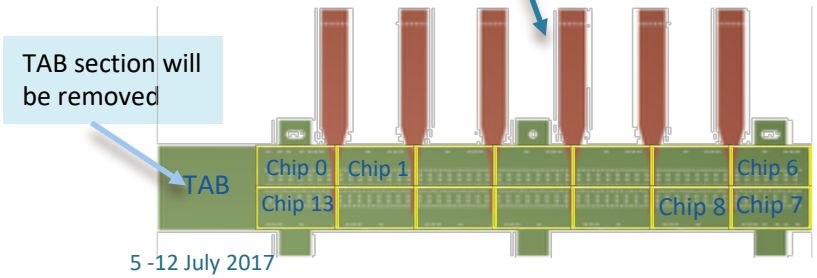


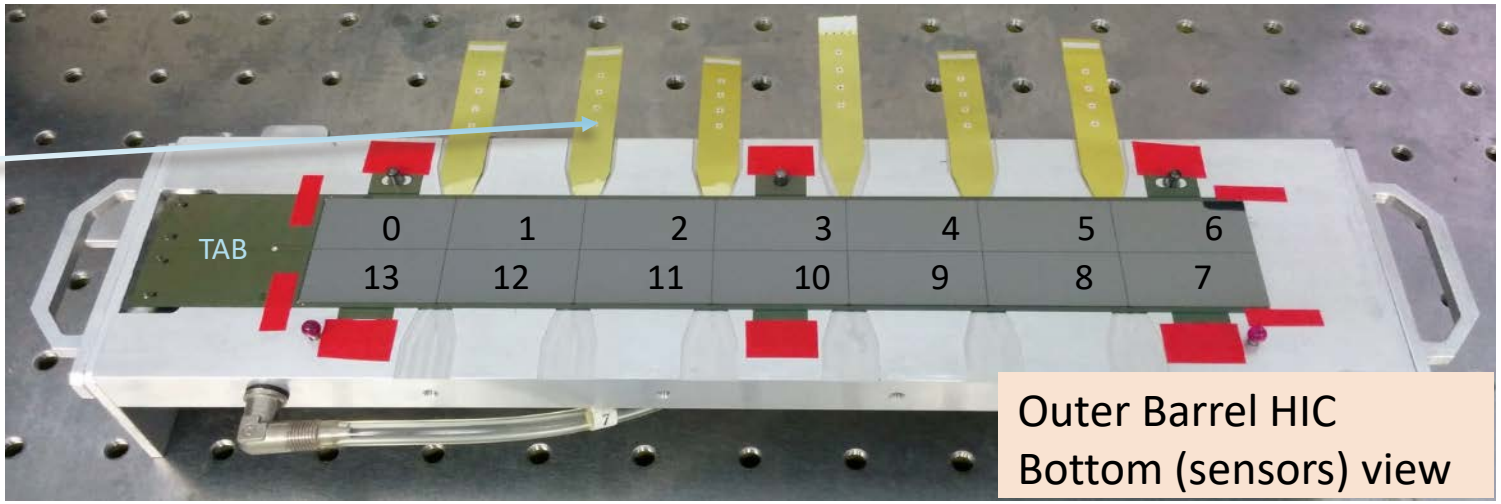
Inner Barrel HIC
Top (circuit) view

Low mass Hybrid Integrated Circuits (HIC)

- IB-HIC: 9 master chips (50 um);
- OB-HIC: 2x7 (1 master, 6 slaves) chips (100um)
- IB (OB): double sided Al(Cu)/polyamide Flexible Printed Circuits (FPC)
- Interconnection based on flip chip and wire bonding technology

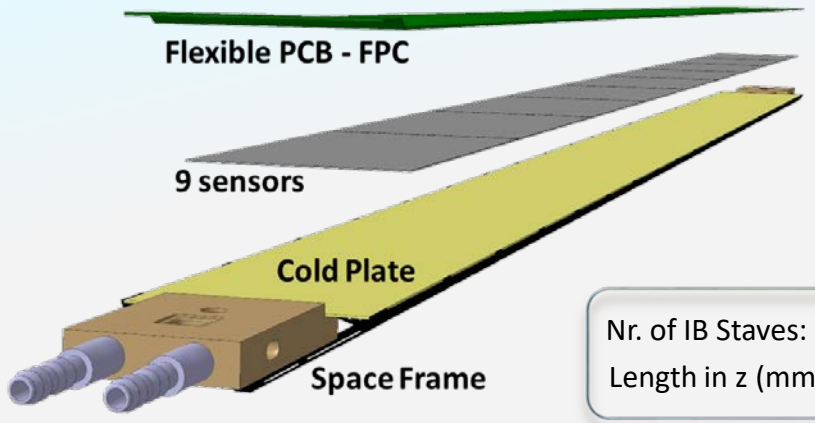
Thin cross cables for later connection to power bus



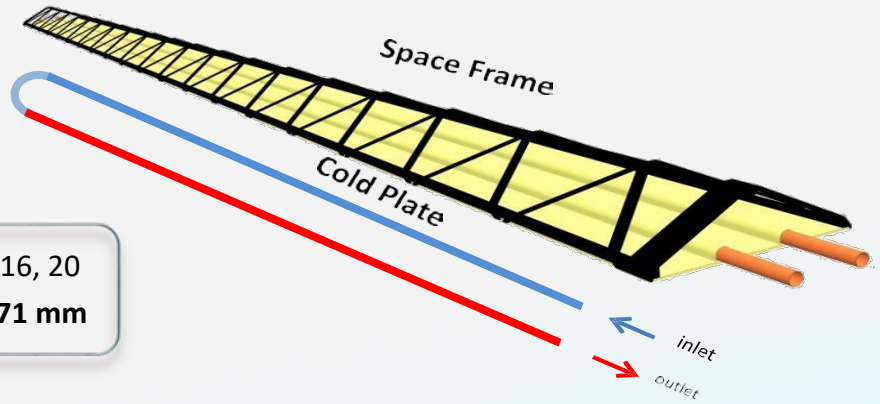


Outer Barrel HIC
Bottom (sensors) view

ITS-UPGRADE STAVES LAYOUT

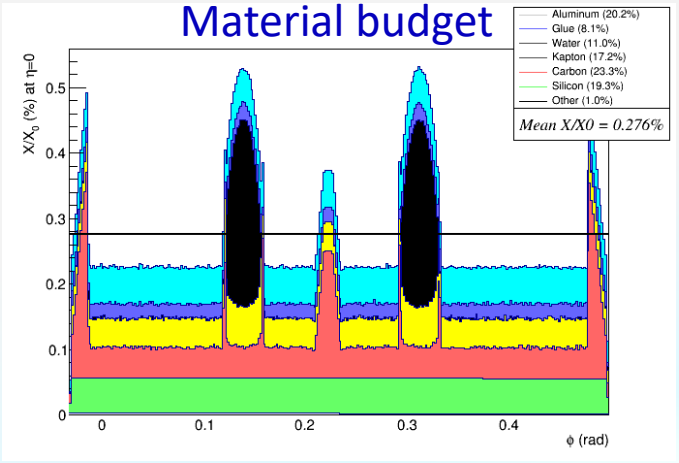


IB stave



Nr. of IB Staves: 12, 16, 20
Length in z (mm): **271 mm**

Material budget



OB stave

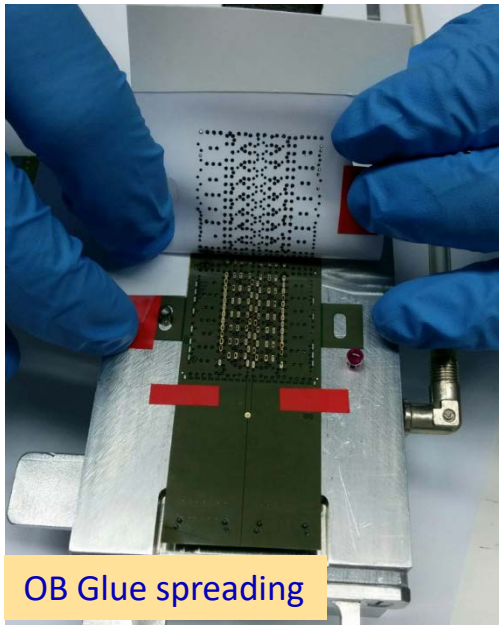
Nr. of OB Staves: 24,30,42,48
Length in z (mm): 844.2 (ML), **1477.5 mm (OL)**
Nr. modules/Half Stave: 4 (ML), 7(OL)

Staves Material budget

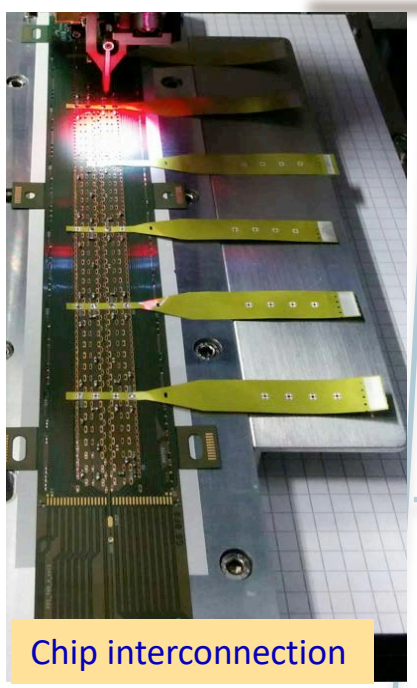
IB: ~0.3% X_0 OB: ~1% X_0

- Ultra-light stiff space frame C structure
- Ultra-light C laminate Cold Plate (with integrated polyimide cooling ducts; single-phase H_2O coolant
- Low mass Hybrid Integrated Circuit

HIC, STAVE, MECHANICS ASSEMBLY AND PRODUCTION

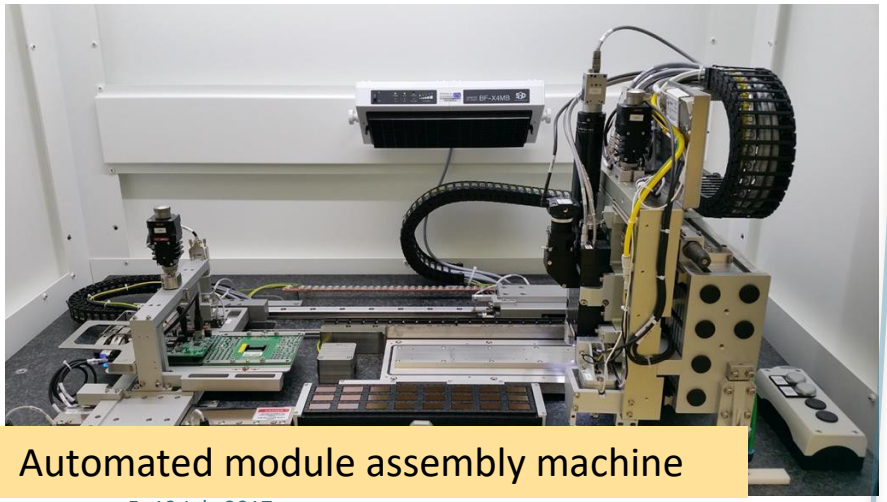


OB Glue spreading



Chip interconnection

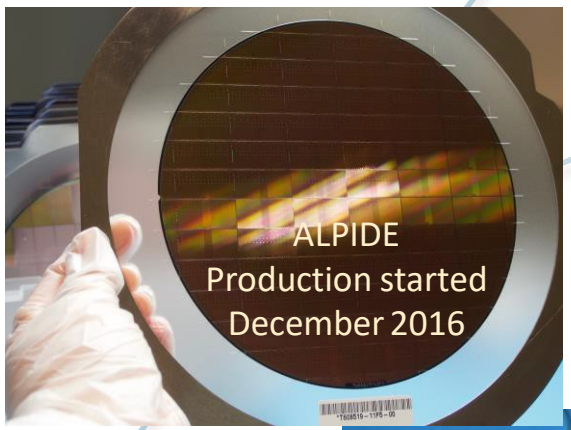
HIC assembly



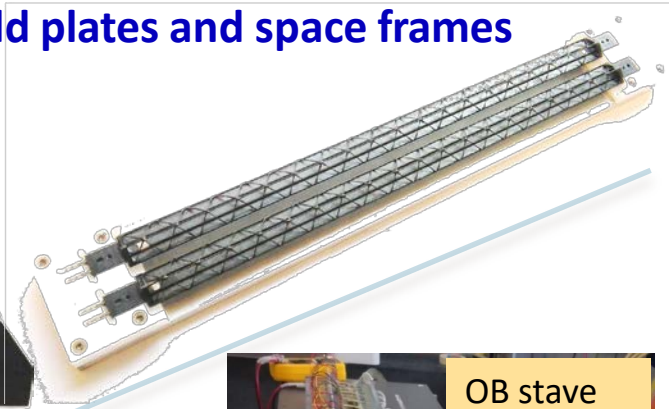
Automated module assembly machine

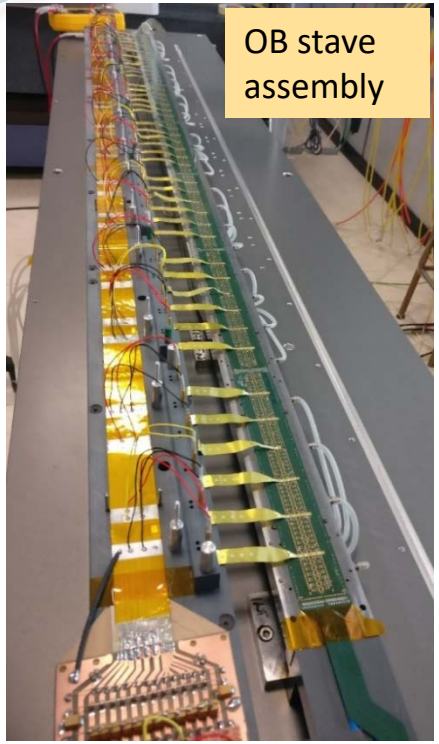
TAB removal

HIC Preparation for assembly



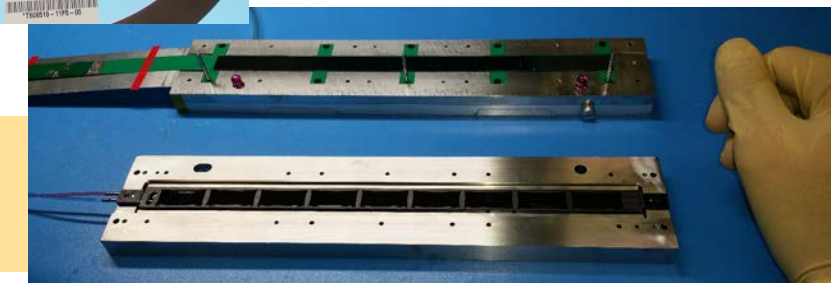
Staves production:
Cold plates and space frames





OB stave assembly

IB and OB staves assembly



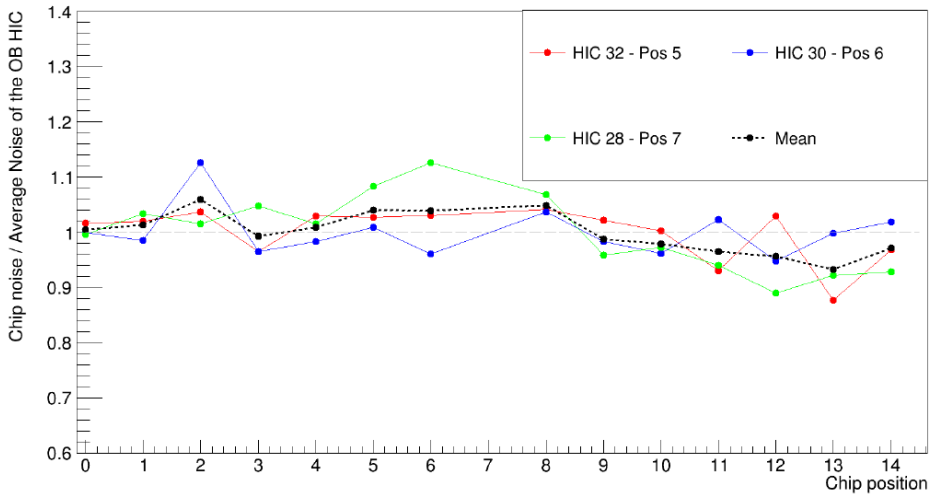
IB Space Frame + HIC gluing

HICS AND STAVES PROTOTYPES CHARACTERIZATION

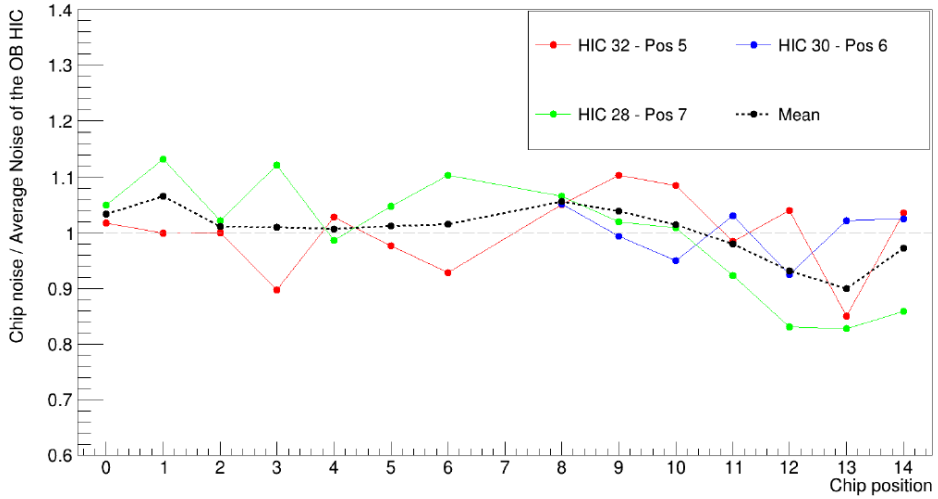
HICs and Staves prototypes

- HICs were characterized in different conditions, operation modes and readout rates
- No significant difference in performance found between standalone chip and chip mounted on HIC
- No significant difference in performance found between HICs and HICs mounted on staves.
- **All performances comparable to standalone ALPIDE chip**

Noise/Average noise-- before mounting



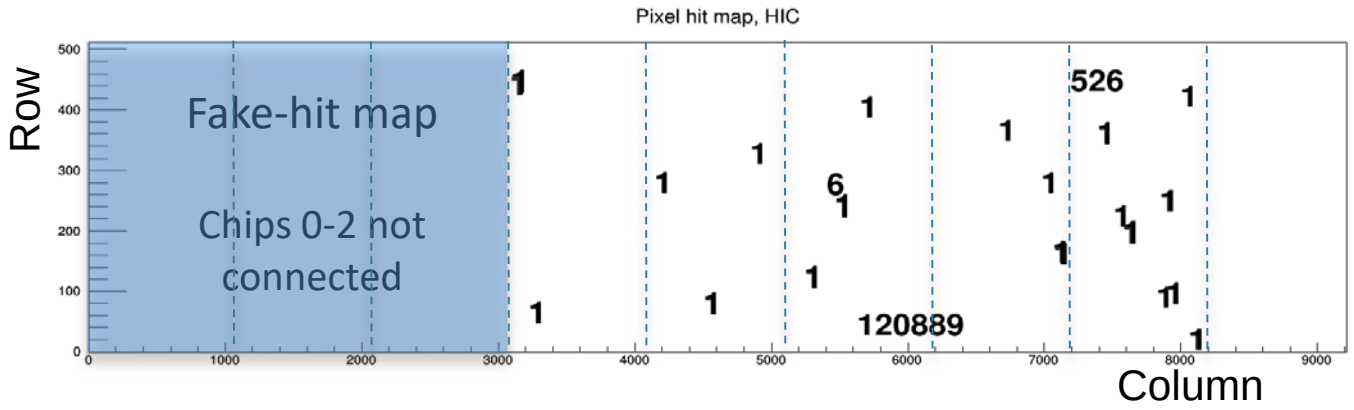
Noise/Average noise-- after mounting



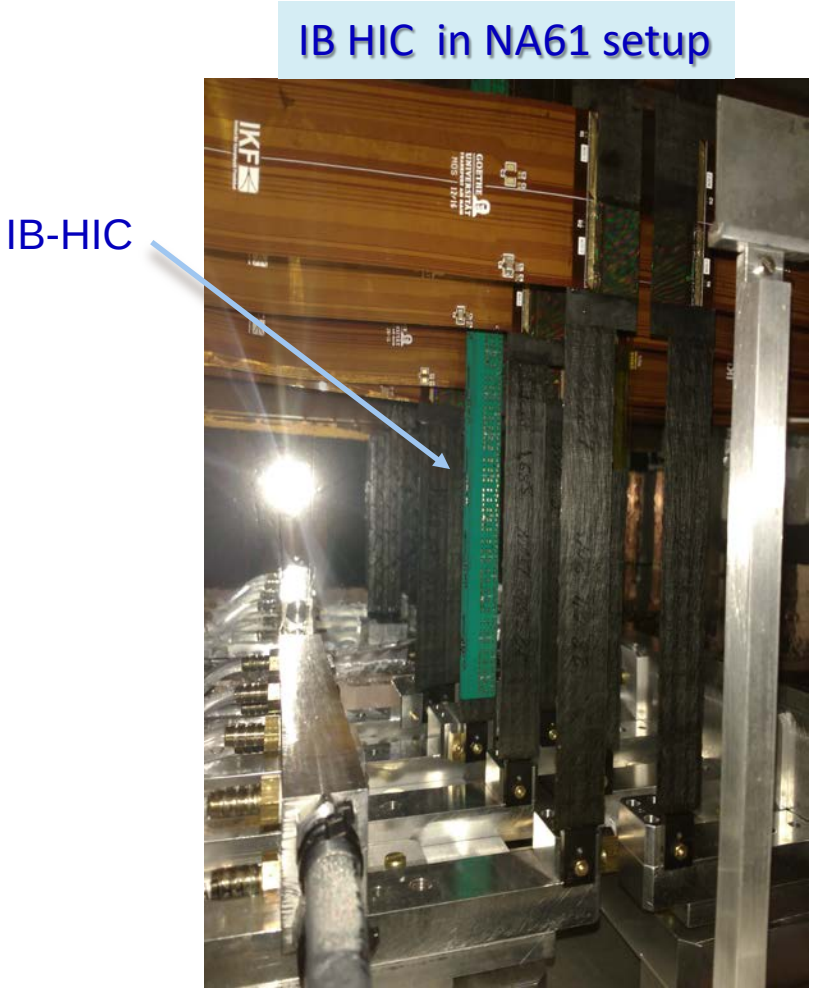
HICS AND STAVES PROTOTYPES CHARACTERIZATION

IB stave tested in Pb-Pb run in NA61/SHINE experiment

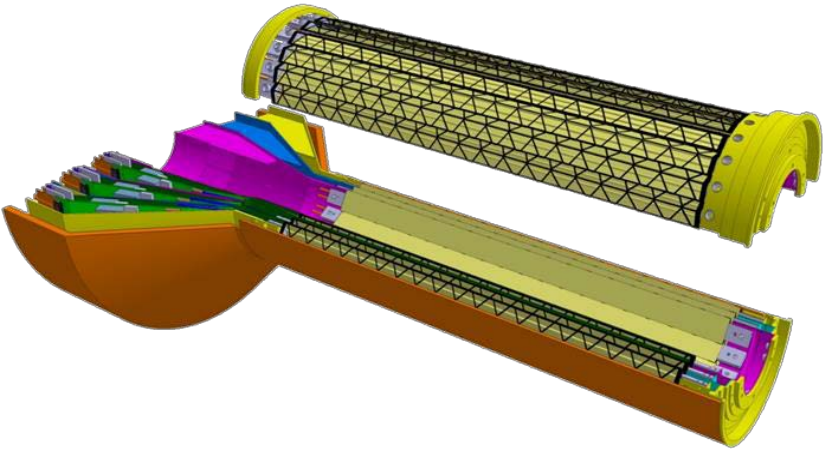
- Hit densities: up to 30 hits/cm^2 (realistic Pb-Pb ALICE running conditions)
- No cooling, no substrate reverse-bias used.
- **Fake hit rate < 10^{-10} hits/pixel/event (10 pixels masked)**
- **Detection efficiency: >99%**
- **Performance comparable to standalone ALPIDE chip**



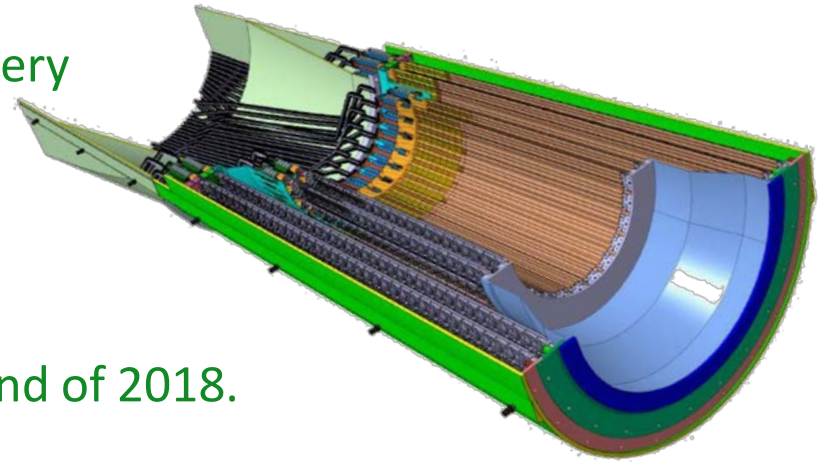
IB HIC in NA61 setup



CONCLUSIONS

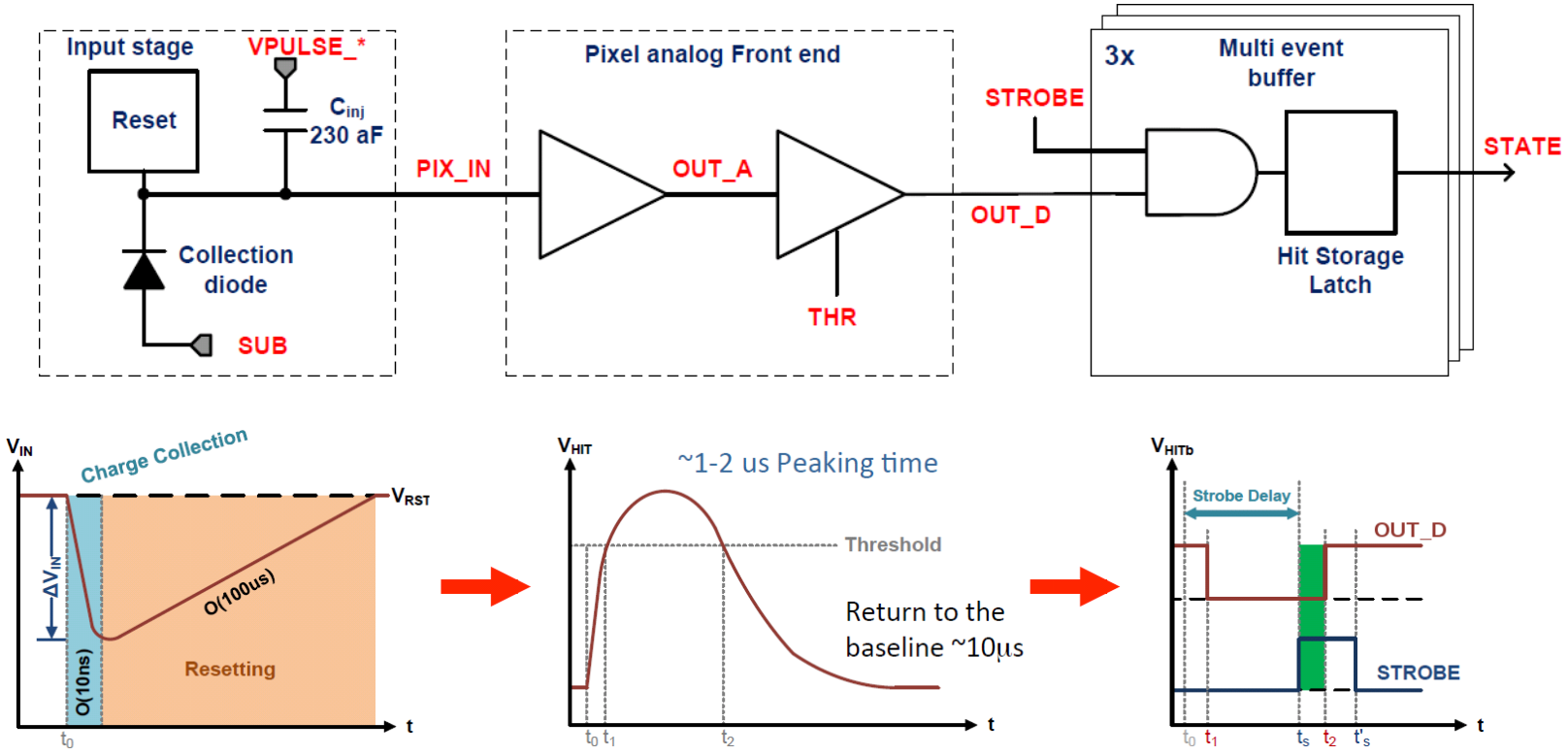


- The ALICE collaboration will perform a major detector upgrade during LS2 to improve readout and tracking capabilities for runs 3&4 at LHC.
- The ALICE Inner Tracking System Upgrade project has successfully completed the R&D phase. All requirements have been met or exceeded.
- The ITS Upgrade will be the largest existing pixel detector with an innovative monolithic pixel sensor with in pixel full CMOS circuitry.
- Detector production started Dec 2016 with the ALPIDE chip start of production.
- Fabrication of staves and barrel mechanics and cooling structures in a very advanced stage.
- HIC production is starting.
- All sites are entering the production phase, expected to finish by the end of 2018.



SPARE SLIDES

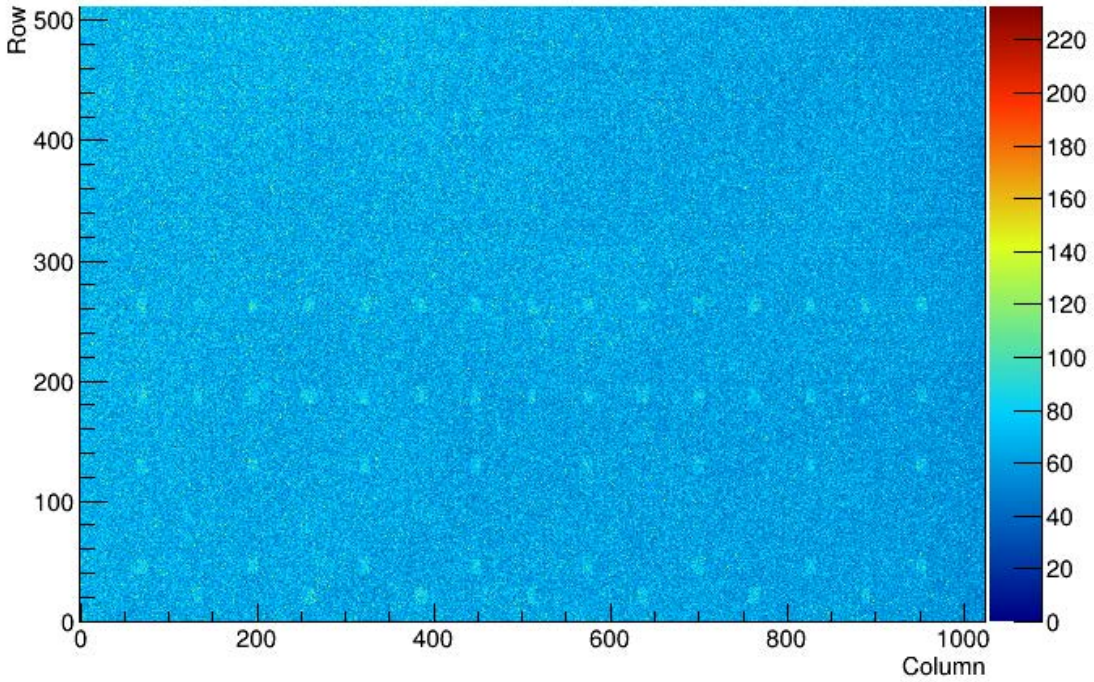
PIXEL

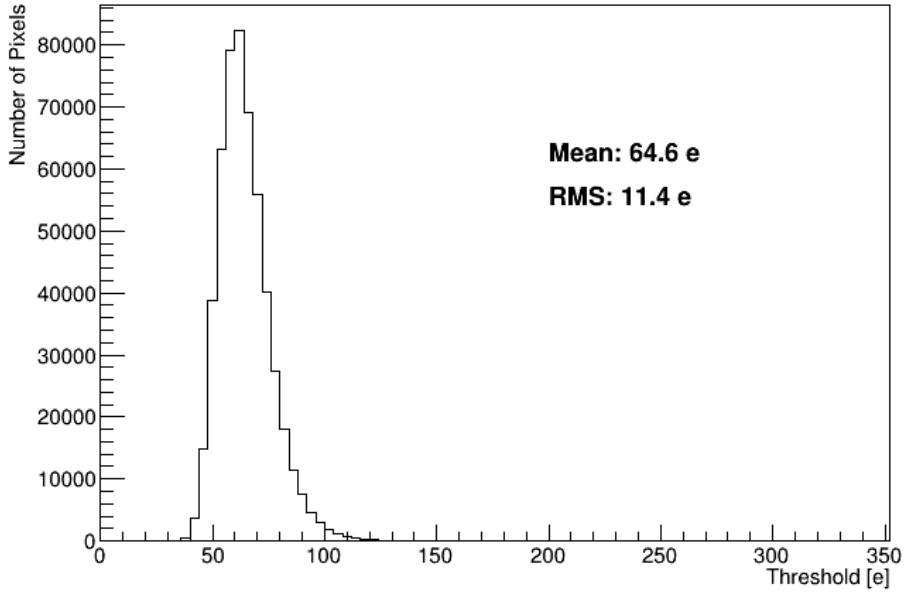


- Charge generated in epitaxial layer is collected
- Signal is shaped and compared to threshold
- Signal is strobed (global shutter) into an in-pixel memory (3 hit storage register)
- Hit pixels are read out asynchronously (priority encoding)

SINGLE CHIP THRESHOLD SCAN

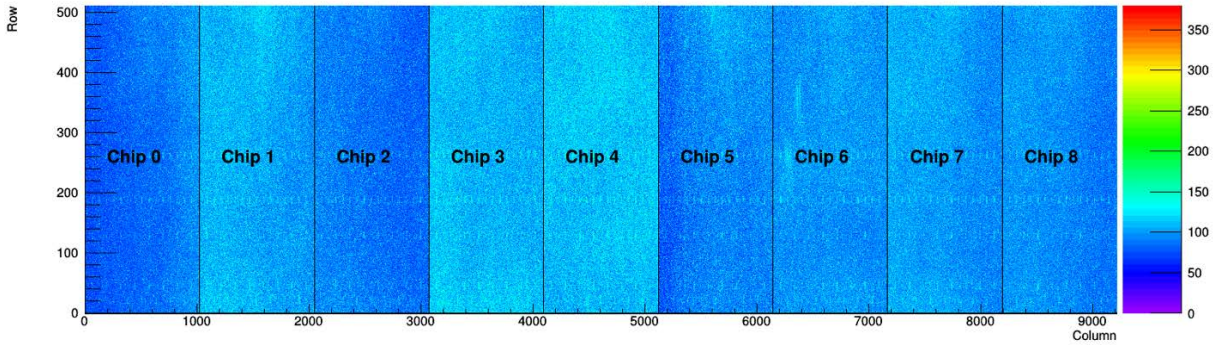
- Example of thresholds from S-curve scans (obtained with charge injections)



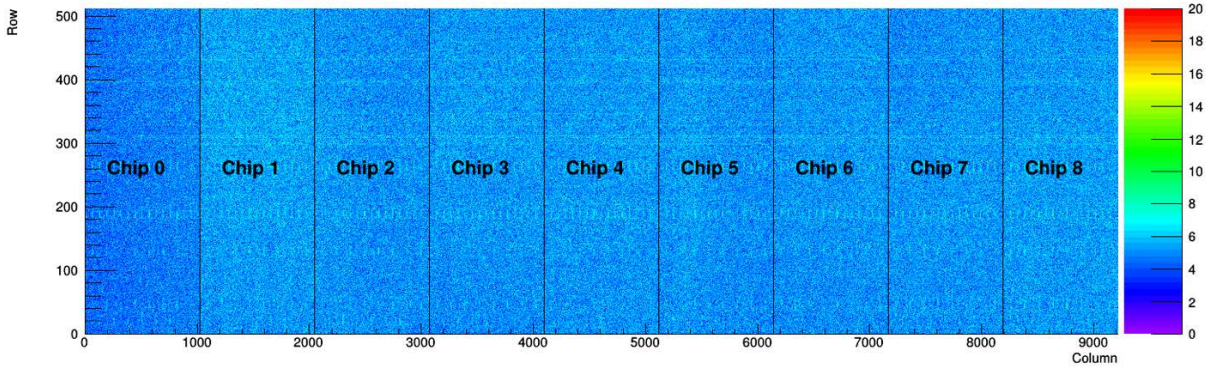


HIC THRESHOLD AND NOISE SCANS

Threshold scan



Noise scan



- Example of threshold and noise scans of an Inner Barrel HIC
- Chip-to-chip fluctuations comparable to single chips

OVERALL ITS PLANNING