Readout board upgrade for the Pixel Detectors: reasons, status and results in ATLAS

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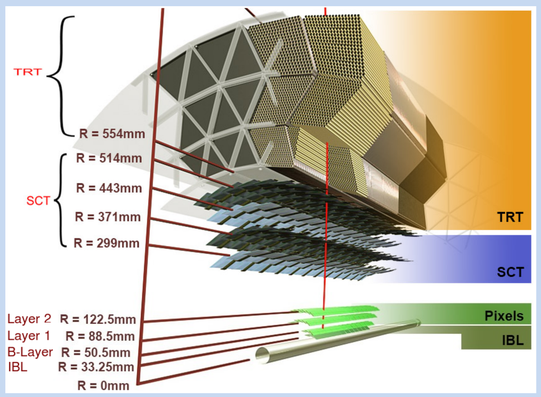
The LHC design luminosity, 10^{34} cm^{-2} s^{-1}, has already been reached and surpassed during Summer 2016. LHC is planning, in the short term future, to further enhance the luminosity, the trigger frequency and the pileup. These factors constitute a challenge for the data readout since the rate of data to be transmitted depends on both pileup and trigger frequency. In the ATLAS experiment, the effect of the increased luminosity is most evident in the Pixel Detector, which is the detector closest to the beam pipe. In order to face the difficult experimental challenges, the readout system was upgraded during the last few years. The main purpose of the upgrade was to provide a higher bandwidth by exploiting more recent technologies. The new readout system is composed by two paired electronic boards named Back Of Crate (BOC) and ReadOut Driver (ROD).
In this poster the main readout limitation related to increased luminosity will be discussed as well as the strategy and the technological solutions adopted in order to cope with the future operational challenges. In addition the general progress and achievements will be presented.

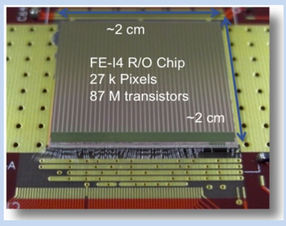
A new readout system for IBL



ATLAS Inner Detector; the four layer of the Pixel Detector are shown: IBL (innermost), B-Layer, Layer 1 and Layer 2

Insertable B-Layer (IBL)

- Innermost detector of ATLAS
- Installed during **2013 - 2015** shutdown
- Increase tracking robustness against failures
- High precision tracking
- **FEI4** front-end chips (130 nm technology)
- Readout speed: **160 Mbit/s**



Old off-detector electronics:

- **Obsolete components** (Spartan 3 FPGAs)
- **Limited bandwidth** (1.04 Gbps per pair)
- **Limited speed of VME bus**, used to calibrate pixels
- Limitations in **control and recovering system**

→ **NOT SUITED TO INTERFACE IBL**

New off-detector electronics

- 2 new cards: **IBLBOC** and **IBLROD** (also called simply **BOC** and **ROD**)
- Maximum bandwidth: **5.12 Gbps**
- Calibration via **Gbit-Ethernet**
- **PowerPC (PPC)** to interface software facilities

→ **DESIGNED TO INTERFACE IBL**

Readout upgrade for all the Pixel Detector Layers

Limits of the old readout

- Limited bandwidth
- Very high **link occupancy** (throughput/bandwidth)
- Link **saturation** for Layer 2 foreseen in 2016 (readout speed: **40 Mbps**)
- Link **saturation** for Layer 1 foreseen in 2017 (readout speed: **80 Mbps**)
- High level of **desynchronization** and **data loss**

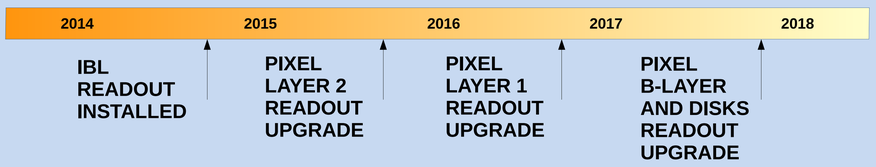
Module Link Occupancy at 100kHz L1

	μ	B-Layer 160 Mbps	Layer 1 160 MBps	Layer 2 80 Mbps
25 ns 13 TeV	40	60%	81%* → 41%	119% → 59%
(Estimation based on 2016 Run)	60	81%	103% → 52%	159% → 79%
	80	101%	125% → 63%	188% → 98%

*Assuming bandwidth before the upgrade

Readout upgrade

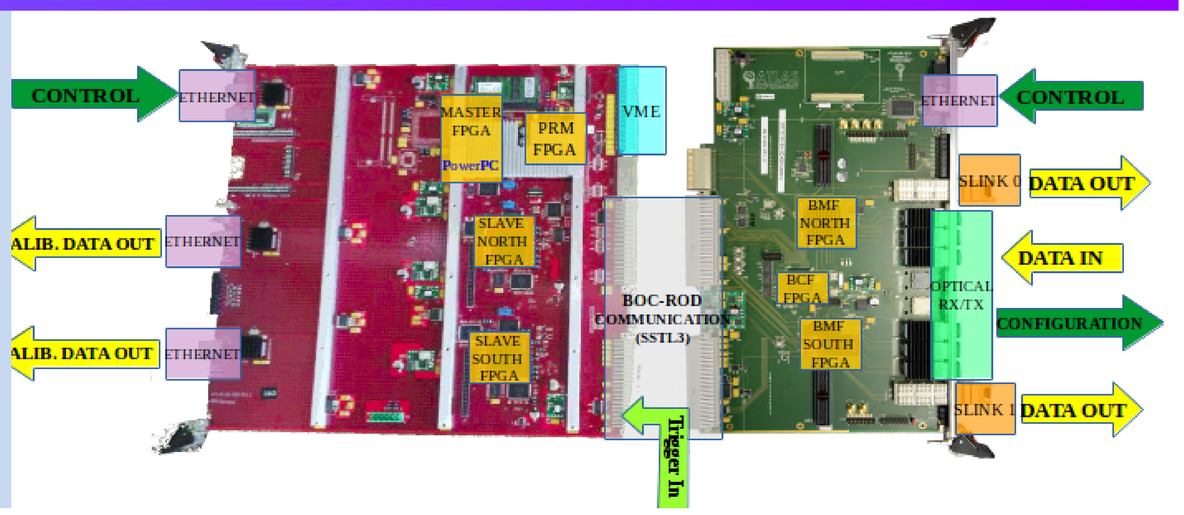
- Same electronic boards as IBL ones (**BOC** and **ROD**)
- Only **firmware** adjustment needed
- **Double readout speed** for Layer 2 (40 → 80 Mbps), Layer 1 (80 → 160 Mbps) and Disks (80 → 160 Mbps)
- **Smaller link occupancy** for Layer 2 (159% → 79 % [μ = 60])
- **Smaller link occupancy** for Layer 1 (103% → 52 % [μ = 60])
- B-Layer upgrade for **system uniformity** (readout speed not enhanced)



New readout overview

ATLAS Pixel Detector readout chain:

- **TIM:** interface with L1 ATLAS trigger
- Front-end Module (**FEI4** for IBL and **FEI3 + MCC** for the other layers)
- **BOC:** clock + optical interfaces
- **ROD:** data processing and histogramming
- **ROS**: data gathering and event reconstruction



Main features

	Old Readout	New Readout
Max Bandwidth (Gbps)	1.04	5.12
Software interface	DSP + VME	PPC + Ethernet
Calibration interface	VME	Gbit-Ethernet
# of FPGAs per ROD	12	4

Readout upgrade results

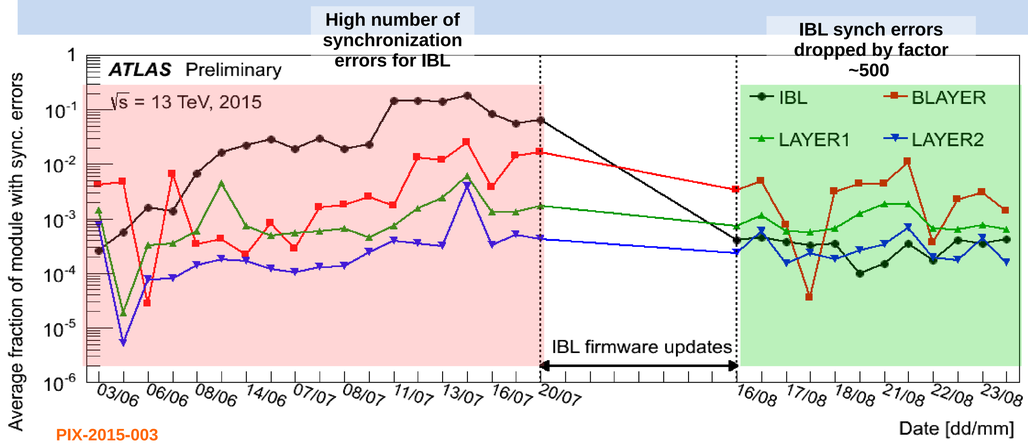
Firmware developments and effects on readout

- Firmware development still ongoing → bug correction and new features implementation (i.e. more debugging signals/registers and improvement in the resynchronization algorithm)
- 2015-2016 → firmware problem for IBL and Layer 2: high ROD induced desynchronization and limitation on trigger rate.

→ **FIXED: NOW SITUATION UNDER CONTROL**

READOUT UPGRADE RESULTS:

- **Link occupancy** reduction
- Reduction in **data-losses**
- Reduction in average **desynchronization**
- **Increased efficiency** in event reconstruction
- Increased **debugging** capabilities



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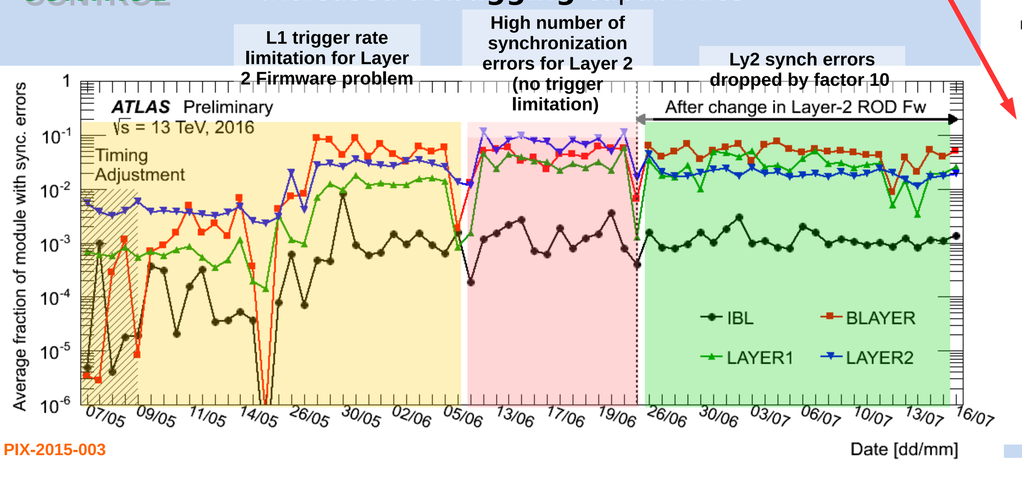

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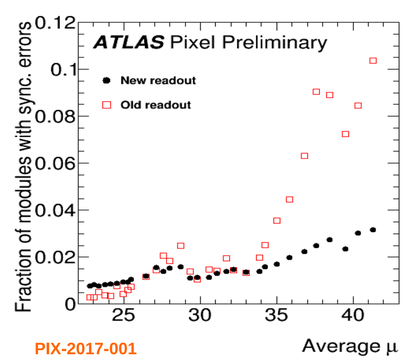

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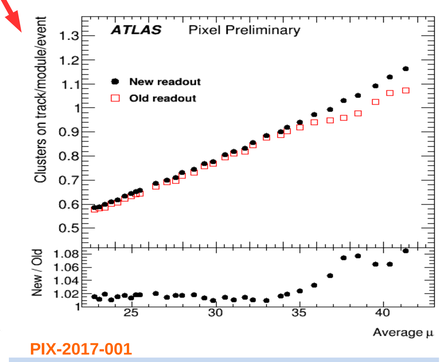

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