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Bonn Contributions to RD53

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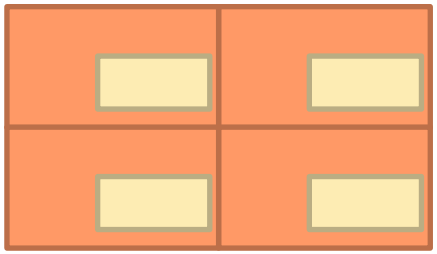
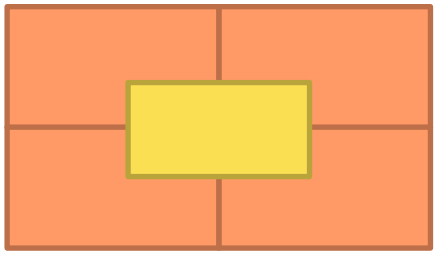
Outline

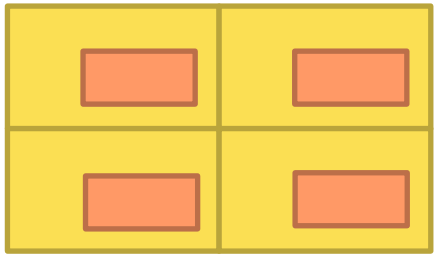
- Pixel chip digital design
- IP block development
- Test systems

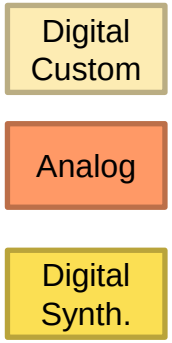
Top Level Integration

Evolution of pixel chip design flow concepts









Traditional full custom design

- Make one pixel
- Step and repeat identical copies
- Custom made digital
- Example: ATLAS FEI-3

More Recently

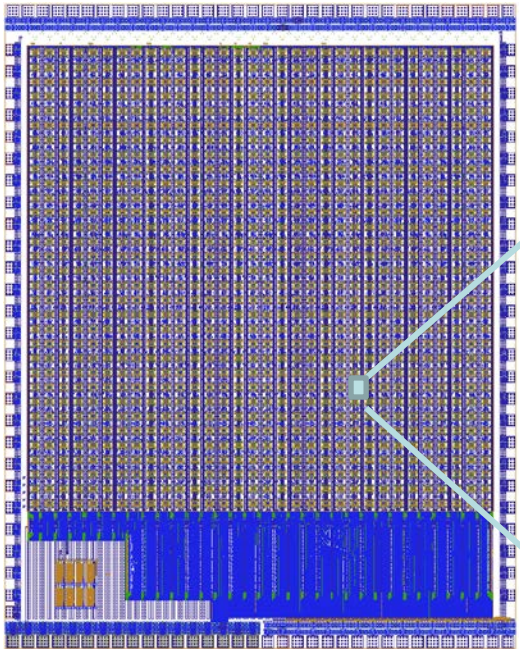
- Make few-pixel region
- Step and Repeat identical copies
- Synthesized digital
- Example: ATLAS FEI-4

New Approach (RD53)

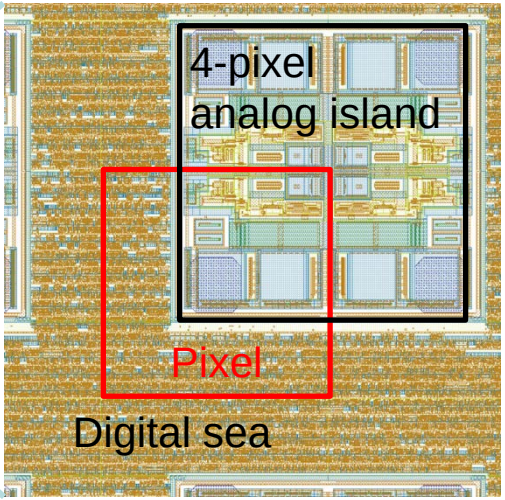
- Synthesized digital “ core” containing a large number of analog pixels
- **FE65_P2**, submitted 2015
- **RD53A**, to be submitted Q1 2017

ATLAS Pixel Matrix FE65_P2

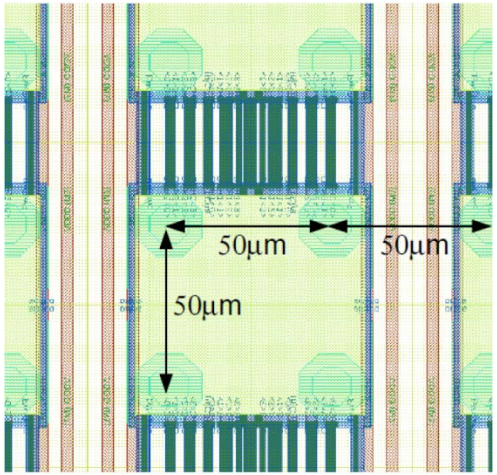
- Architecture and floor-planning concept
  - “Digital sea with analog islands”
  - Pre-routed power and global signal distribution
  - Analog-digital isolation with separate deep n-wells
  - Try to achieve constant digital power consumption



FE65_P2 prototype chip layout,
64 x 64 pixel, 50µm pitch

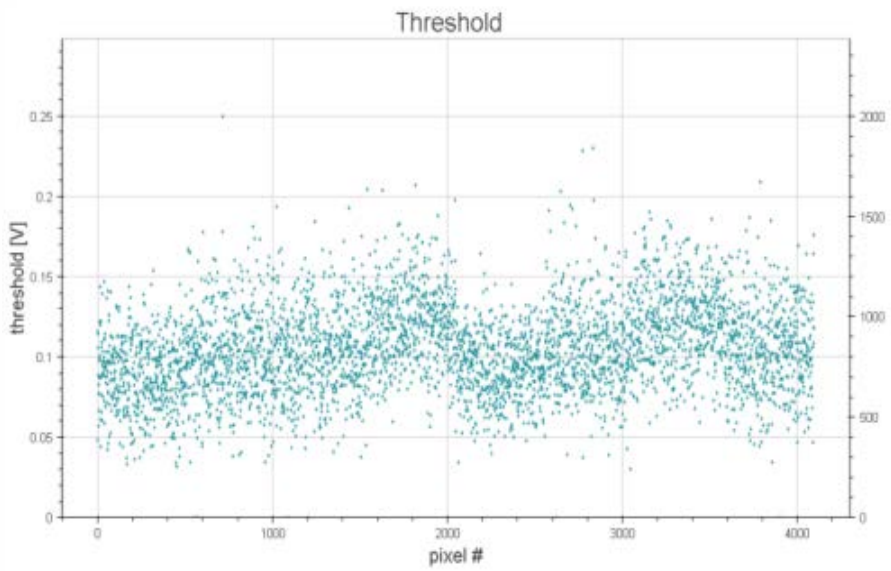


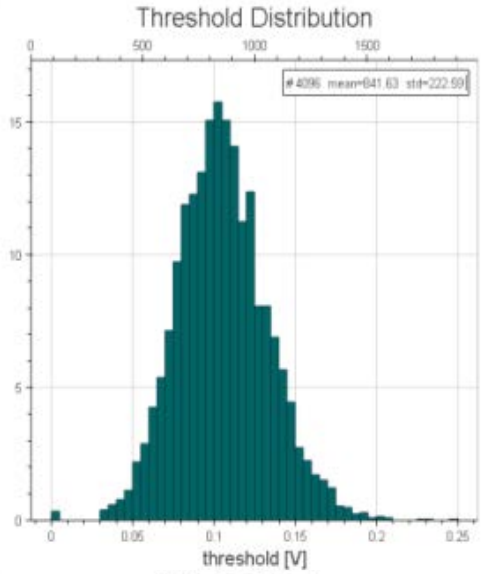
Pixel region with digital sea and analog islands



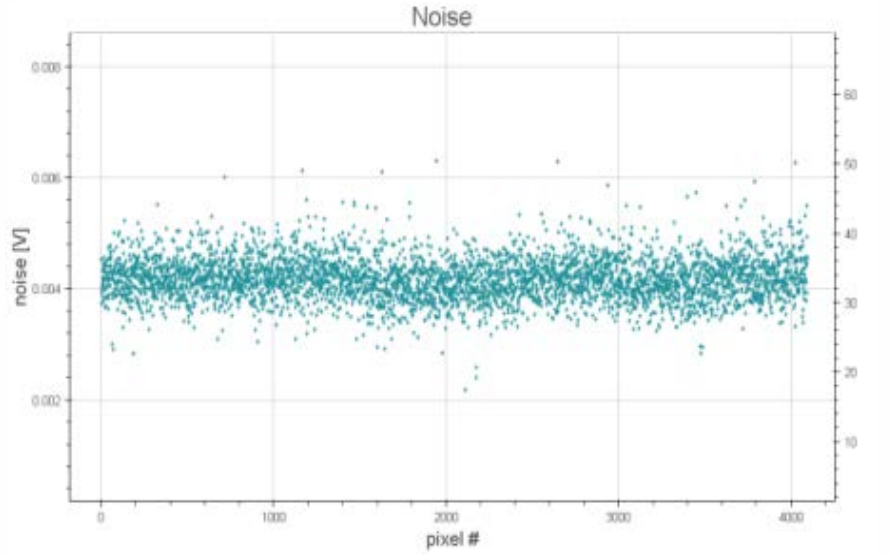
Pre-routed bias and power busses with placed bump pads

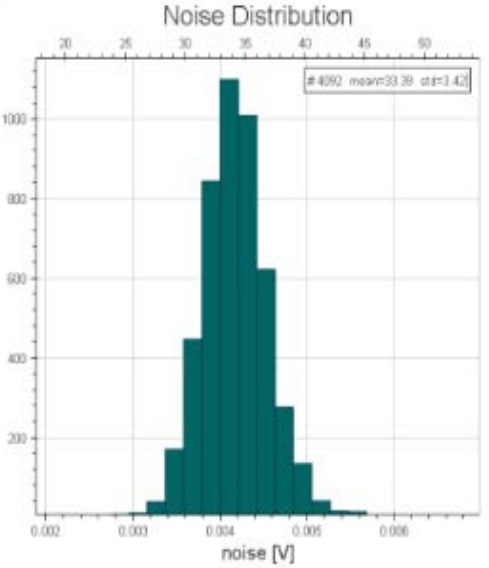
FE65_P2 - Threshold and Noise (untuned)





mean = 640e-
rms = 222e-

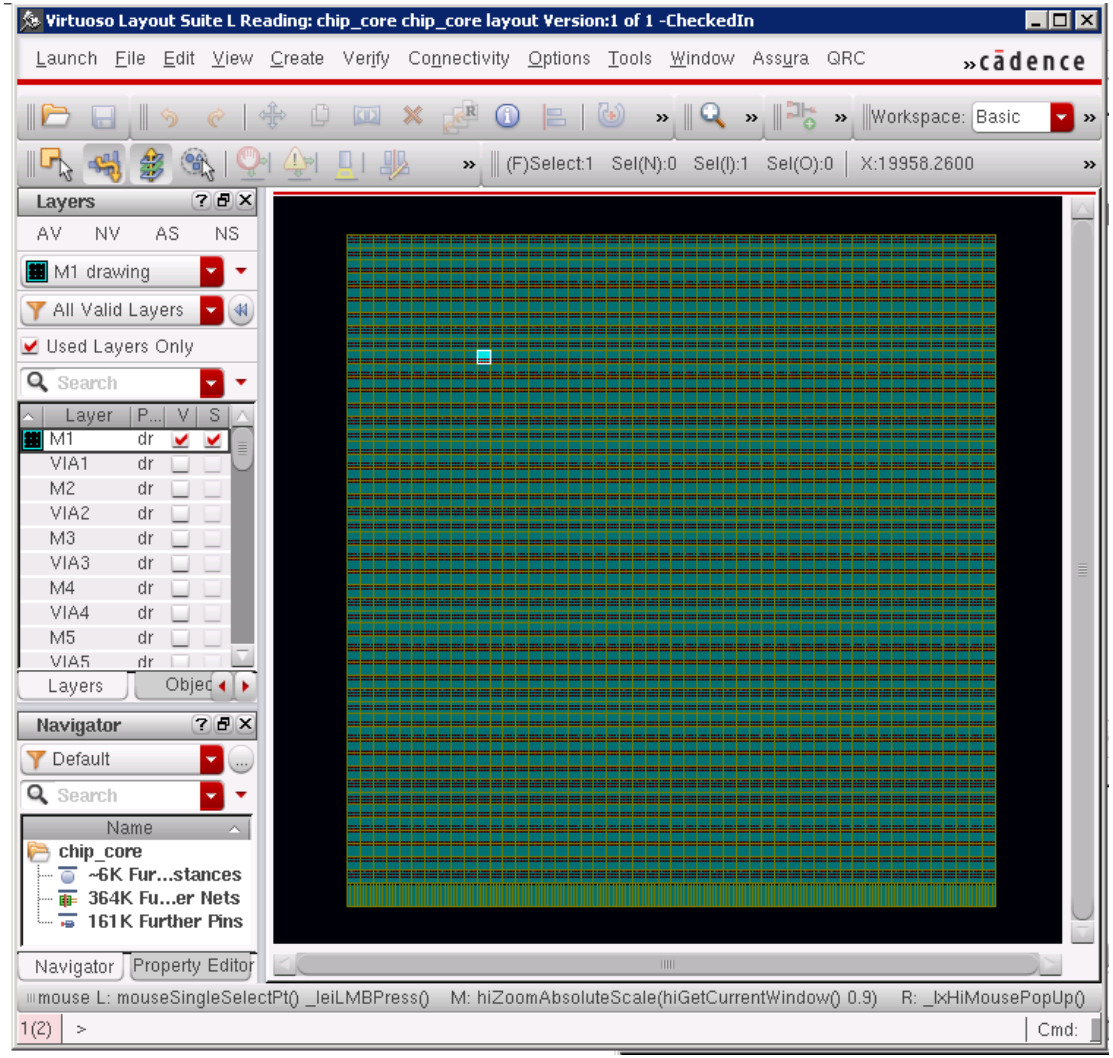




mean = 33.4e-

RD53A – Digital Design

- Initial full layout
  - Core size: 8x8
  - Array size: 50x50 (400x400 pixels)
  - End of Column: 200x



Contributions to IP Development

- Clock data recovery (CDR) and PLL
  - Command and clock information encoded on one differential line (@160Mbps)
  - CDR extracts command and clock information
  - PLL stabilizes the 160 MHz clock and generates
    - BCO_CLK = 40 MHz (adjustable phase)
    - SER_CLK = 1.6 GHz (tbd)

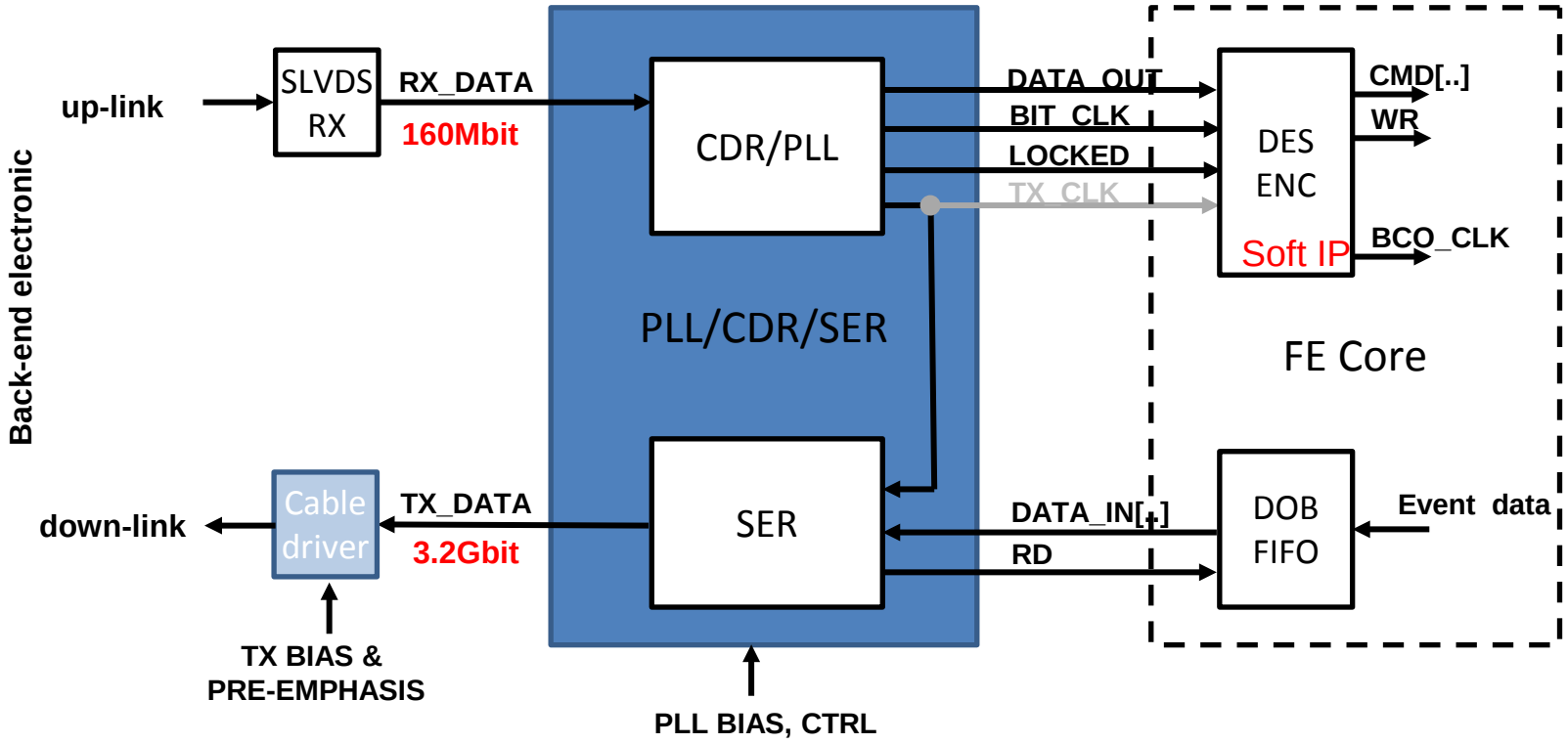
- Serializer (SER)
  - Runs at 1.6Gbps (or 3.2Gbps, tbd)
  - Generates the Gbit output stream for the hit data

- Gbit link cable driver
  - Transmits the hit data on a low mass cable
  - Driver uses pre-emphasis to compensate cable loss

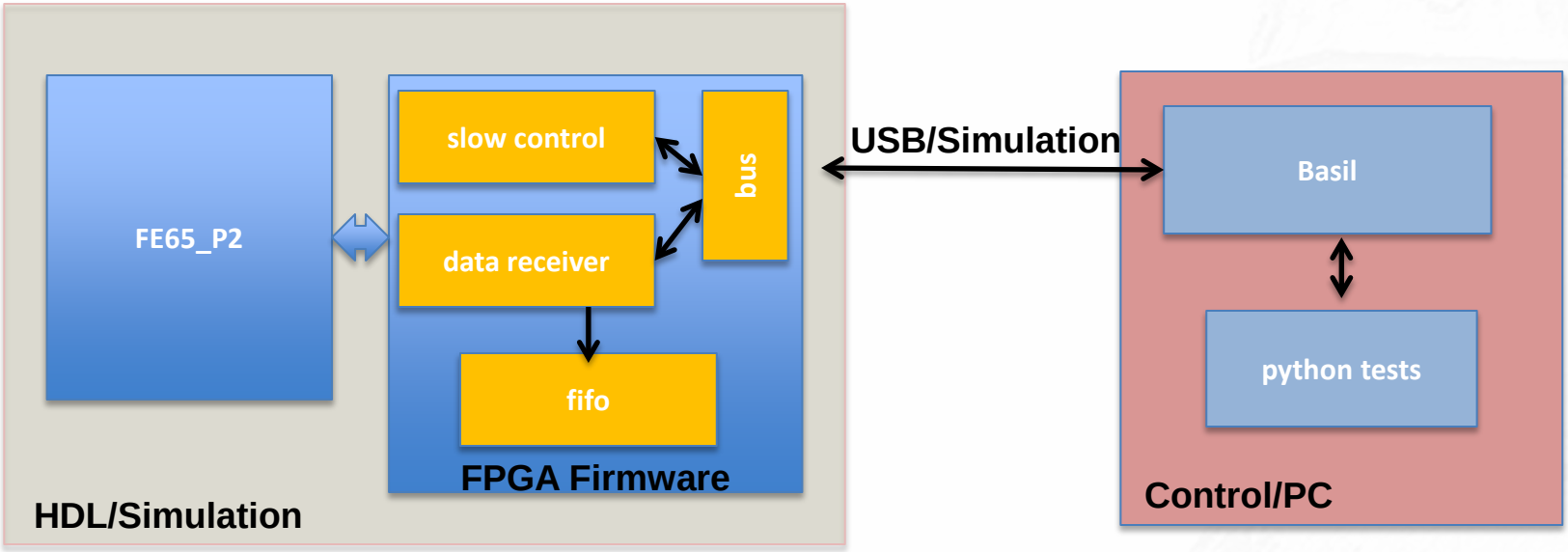
- Pad frame
  - Integration of IO blocks (driver/receiver) and voltage regulators (Shunt-LDO)

IP Development for I/O

- FE interface
  - One up-link, combining CLK and CMD → needs clock/data recovery (CDR)
  - One (or more) high speed (> 2Gbps) down-links → serializer (SER) and Gbit driver (TX)
  - Bit rates and encoding schemes currently under discussion



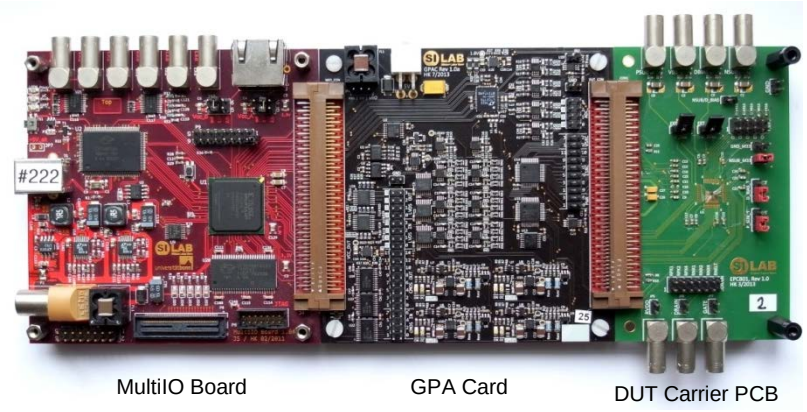
Verification



Exactly the same python code can be used for testing physical chip. Same firmware for FPGA (ready to use by USBpix/GPAC).

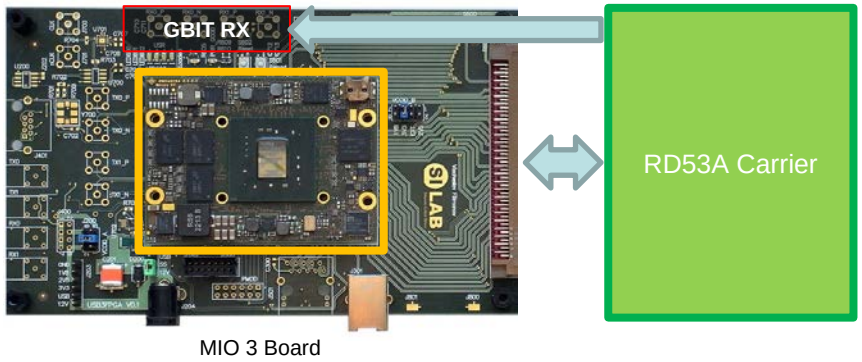
```
self.chip['global_conf']['InjEnLd'] = 0
self.chip['global_conf']['TDacLd'] = 0
self.chip['global_conf']['PixConfLd'] = 0
self.chip['global_conf'].set_wait(200)
self.chip.write_global() #send some test hit

while not self.chip['trigger'].is_done():
    pass

print 'fifo_size', self.chip['fifo'].get_fifo_size()
data = self.chip['fifo'].get_data()
```

Test Systems for FE65_P2 and RD53A



FE65_P2 test system

- Based on USBpix and GPAC for analog support functions
- Python-based software/firmware framework (Basil -> https://github.com/SiLab-Bonn/basil)
- Test software and firmware: https://github.com/SiLab-Bonn/fe65_p2



RD53A test system (planned)

- Based on USBpix 3 (MIO 3) with enhanced Gbit link support (4 instead of two links)
- Test SW und FW similar to FE65_P2 system

Conclusion & Outlook

- First prototype matrix chip FE65_P2 designed using a digital centered design flow
  - Chip tested successfully (ongoing), good analog digital isolation
  - Assemblies with bumped sensor on the way (MPW run, no wafers for bumping available)

- IP development and digital design for the demonstrator chip RD53A is ongoing

- Verification framework will be reusable for testing the physical chip (USBpix/basil)
  - Current USBpix test system will be upgraded to support multiple Gbit links for RD53A

- RD53A to be submitted on a shared engineering run in spring 2017