OMEGA Activities for WP4

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Organization for Micro-Electronics desiGn and Applications

WP4.3 tasks

- CNRS-IPNL, CNRS-OMEGA, DESY, AGH-UST. Coordination: CNRS-OMEGA
- Selection of best SiGe 130/180 nm process for high speed/high dynamic range ASIC design to upgrade current SiGe 350 nm AMS process
- Delivery of SPIROC3: SiPM readout ASIC for calorimeter readout of WP14
- Delivery RPC high timing resolution readout chip for WP13
- Share expertise within SiGe HEP community
- Study for LHC run 2, ILC ...

SiGe processes evaluated

- Tower Jazz SiGe 180 nm
  - After several requests, design kit never supplied
- ST Micro SiGe 130 nm
  - Design kit installed at OMEGA mid 2015 and running
  - Simulations performed for ATLAS LAr calo upgrade
  - Simulations for CMS HGCAL imaging calo and 50 ps timing
  - Simulations for timing detectors e.g. ATLAS HGTD
- Comparison with TSMC 130nm

Simulations made with SiGe process

- Low noise line terminating preamp for ATLAS LArG upgrade
  - Current version uses discrete bipolar transistors to achieve en=0.4 nV/√Hz
  - Dynamic range up to 10 mA
  - 25/50 Ω active termination over full dynamic range
- Low noise system on chip for CMS HGCAL
  - Charge and time measurement
- High speed readout for LGAD or RPC detectors
  - 1 GHz broadband amplifier

New preamp design for ATLAS LArG (1)

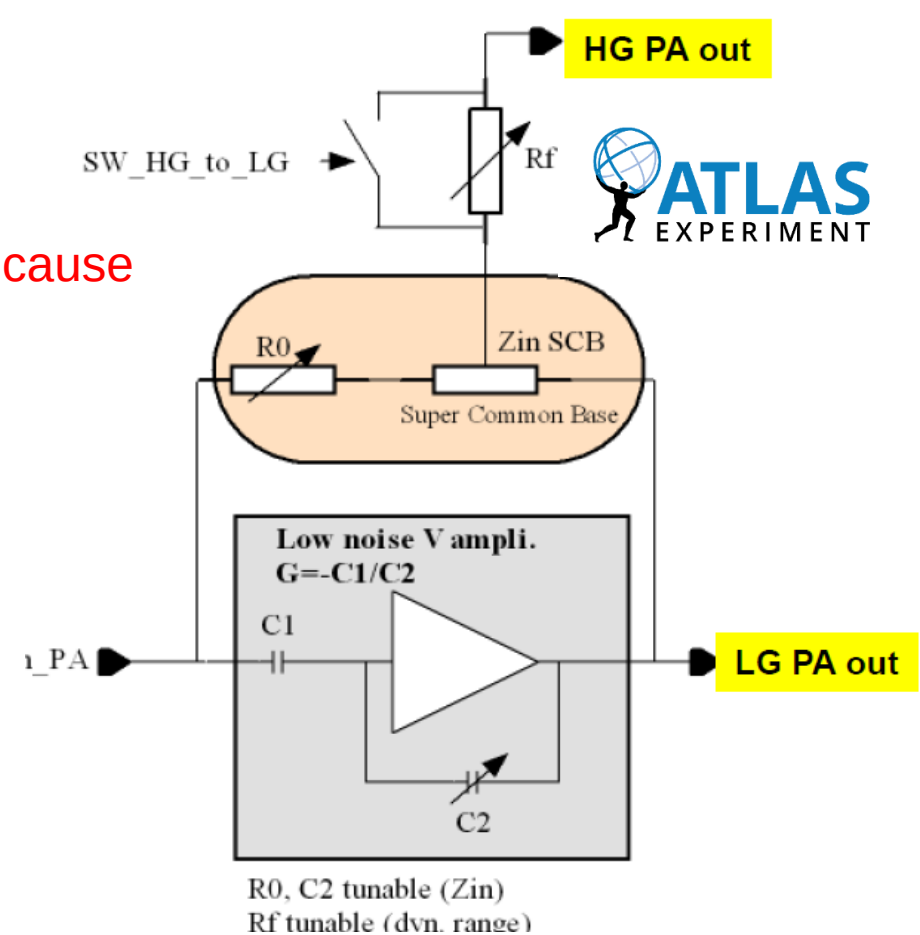
Super common base preamp (low Zin) Low noise voltage sensitive preamp

Input Impedance : $$Z_{in}\,PA = \frac{R_0 + Z_{in}(SCB)}{1 + |G|}$$

Noise $$\frac{4kTR_0}{(1+|G|)^2}$$

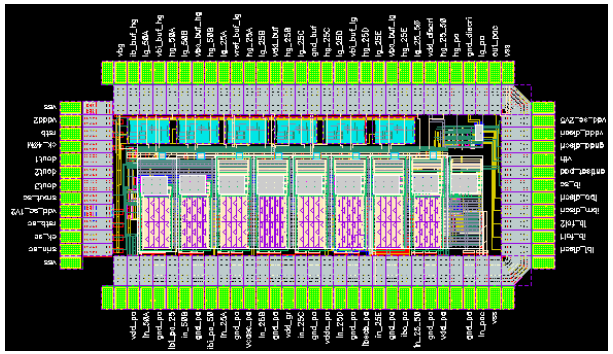
Better in CMOS than SiGe at Ic=10 mA because of $R_{BB'}$ and parallel noise

	50 Ω	25 Ω
R0	500 Ω	100 Ω
G	C1/C2=9	C1/C2=3
Noise	5 Ω	6Ω
Dynamic	2 mA with Rf=5kΩ	10 mA with Rf=1kΩ



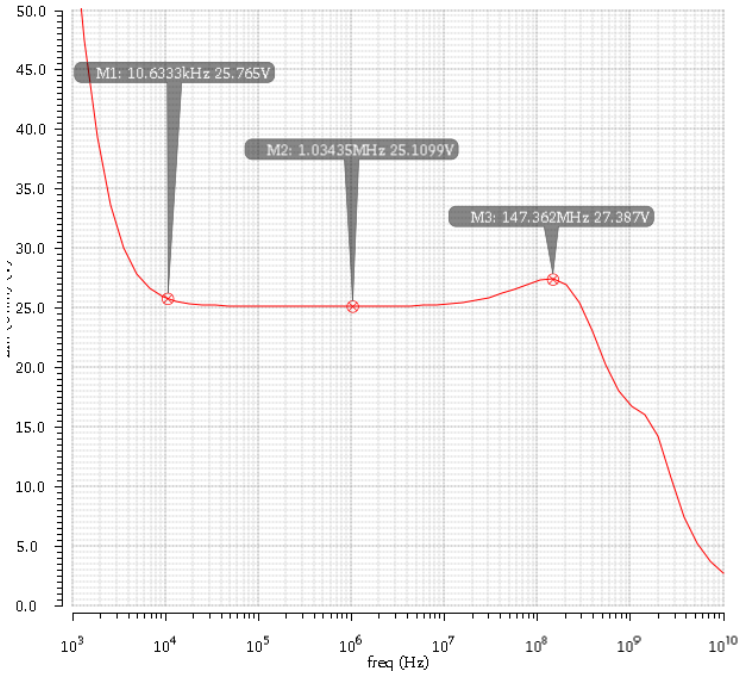
New preamp design for ATLAS LArG (2)

- TSMC 130 nm / SiGe 130nm: Better noise performance as better gm of SiGe is hindered by $R_{BB'}$ and base current



- First prototype with 8 channels, with or without tuning options (impedance/gain transition…). Various transistor sizes and capacitor types + protection diodes (against detector HV trip)

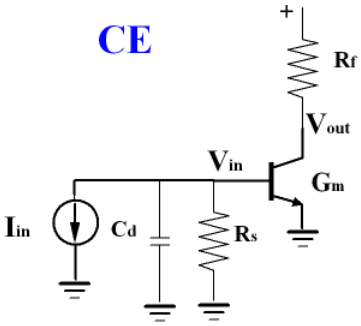
- Prototype chip submitted on May 15th through CERN/TSMC



- BNL/Omega/LAL Collaborative effort: Goal is to converge towards a common CMOS preamp architecture in CMOS technology

ATLAS HGTD: High speed preamps simulations

- High Granularity Detector for ATLAS (Phase 2): Time resolution 30 ps/channel, LGAD or Si Pin diodes detectors
  - Similar performance for Broad Band (CE) and Transimpedance (TZ) configurations
  - Performance dominated by detector capacitance Cd and signal duration td
  - Preamp transconductance gm determines noise, scaling as sqrt(Id)
  - Preamp bandwidth should match signal duration



$$\sigma_t^2 = \left(\frac{t_{rise}}{S/N}\right)^2 + \left(\left[\frac{t_{rise}V_{th}}{S}\right]_{RMS}\right)^2 + \left(\frac{TDC_{bin}}{\sqrt{12}}\right)^2$$

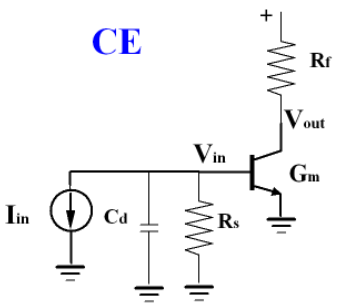
Jitter

Time Walk

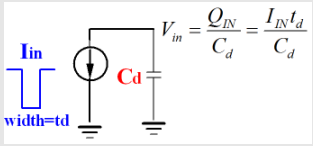
TDC

CE in SiGe 130nm and in TSMC 130 nm

- Broad Band amplifier CE configuration
- Same current (Ic=700 µA), same Rf=4K, vdd=1.2V
- Higher gain with SiGe but larger noise due to rbb'

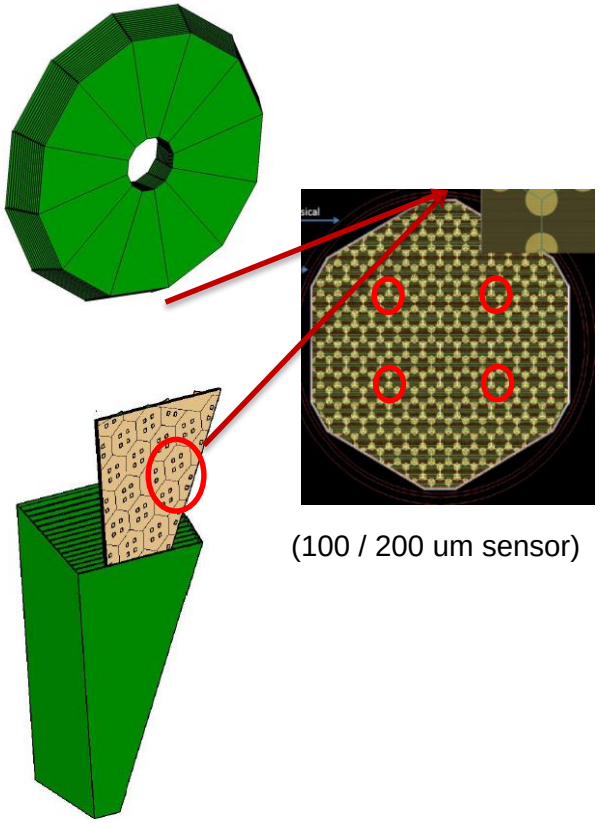


$$\sigma_t^J = \frac{t_r}{\frac{S}{N}}$$

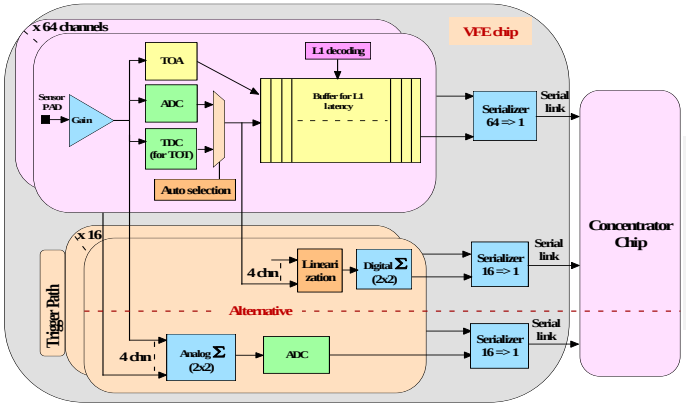
	CE 10pF TSMC 130 nm	CE 10pF SiGe 130nm Trans size= 10	CE 10pF SiGe 130nm Trans size= 20
td=10ps Qin=Iin.td= 100µA.10ps=**1fC** 	out=3.7mV tr=220ps BWa=1.6 GHz rms=1.3 mV S/N=2.8 σj=220ps/2.8=78 ps	out=9.07mV tr=140ps BWa=2.4 GHz rms=4 mV S/N=2.25 σj=140ps/2.25=62 ps	out=8.95 mV tr=176 ps BWa= 2GHz rms=3.14mV S/N=2.85 σj=176ps/2.85=60 ps
td=1ns and tr_ampli=td CL=100fF Qin= 1µA.1ns=**1fC**	out=3.52mV(CL=100fF) tr=1.1ns BWa=440MHz rms=0.66mV S/N=5.3 σj=1100ps/5.3=206 ps	out=7.5mV (CL=120fF) tr=1.1 ns BWa=440MHz rms=1.6 mV S/N=4.7 σj=1.1ns/4.7=235 ps	out=7.5mV (CL=110fF) tr=1.1 ns BWa=440MHz rms=1.4 mV S/N=5.4 σj=1.1ns/5.4=204 ps

High granularity Silicon-Tungsten end cap calorimeter

- Large dynamic range : 0.2 fC – 10 pC, low power < 10 mW/ch
- Good timing capability : 50 ps/Channel
- High radiation tolerance : 200 Mrad and 5. 10^{15} N/cm²

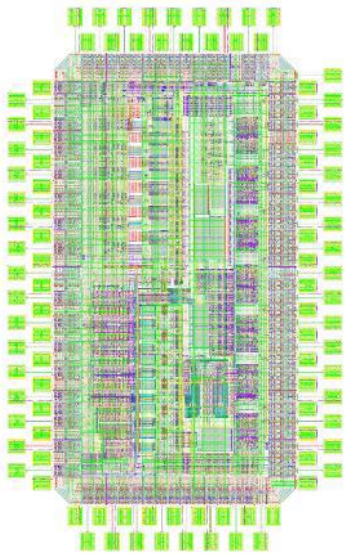


(100 / 200 um sensor)

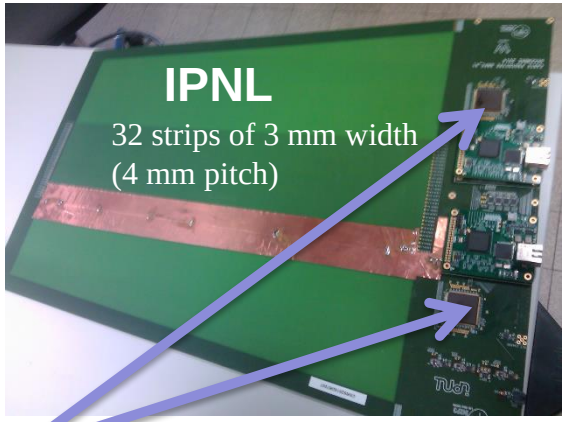


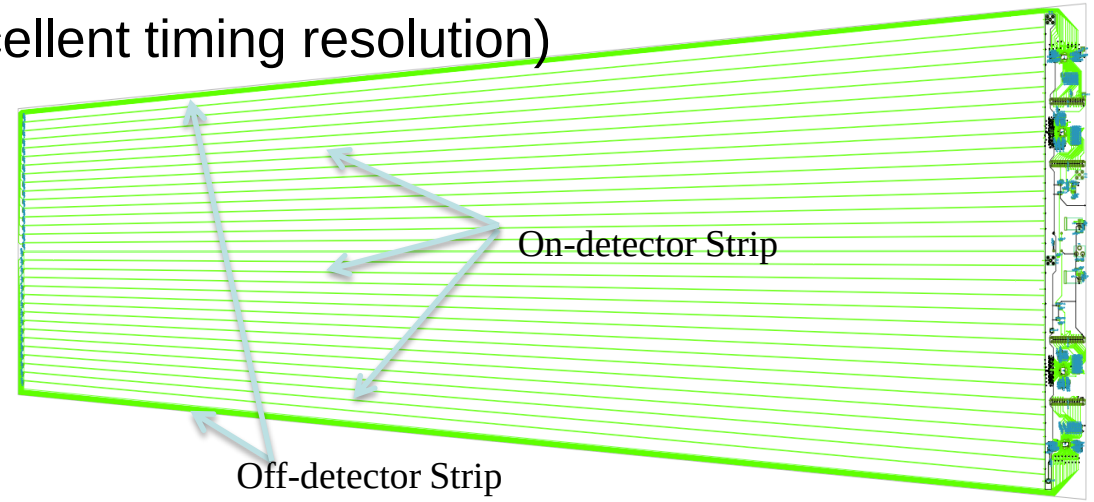
MOST OF THE CELLS CAN BE USED IN SPIROC3

- TSMC 130 nm, Test Vehicle chip submitted on May 15th through CERN/TSMC
  - 6 positive input preamp
  - 6 negative input preamp
  - 1 baseline channel (CERN)
  - 4 discriminators
  - HG and LG shapers
  - Digital part



- Multi gap CMS-GRPC (excellent timing resolution)





- PETIROC2: AMS SiGe 0.35µm,
  - 32-channel,
  - high bandwidth preamp (GBWP> 10 GHz),
  - <3 mW/ch, dual time and charge measurement (160 fC-400 pC)
  - **low-jitter < 25 ps rms**
  - **Couplings through the substrate**

=> PETIROC3: redone in TSMC 130nm

CONCLUSION

- Proposal to use TSMC 130nm instead of SiGe technology
  - Suitable radiation hardness for LHC upgrades (400 Mrad 10^{16}N)
  - Better noise performance as better gm of SiGe is hindered by $R_{BB'}$ and base current
  - Similar speed performance for timing detectors ~1 GHz

- Test vehicles for CMS HGCAL and ATLAS LAr submitted mid May 2016, expected this summer, first tests in September

- Larger community (CERN, AGH, IRFU…)