Microelectronics for Calorimeter readout

- Development of the KLauS ASIC at Uni Heidelberg
- ASIC Characterization & System integration activities at DESY

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KLauS – a SiPM readout ASIC for calorimetry

Low power: 25uW/ch; Power pulsing with <1% duty cycle

Targeting high density SiPMs
[e.g. 10um MPPC, gain \( \geq 10^5 \), 10k Pixels]

Required equivalent noise charge \( \leq 3\text{fC} \)
dynamic range \( \approx 150\text{pC} \)

CMOS technology

KLauS2: AMS .35 technology
12 channel analog front-end

KLaus3 prototypes: UMC .18 technology
SoC: integrated front-end, ADC & digital storage/TX
New Front-end,
Low-power SAR ADC [10b; 12b for SiPM gain calibration]

Channel-wise ADC, immediate signal digitization
Front-end: Blocks

**Input stage:**
- Low input impedance
- SiPM bias voltage tuning
- 3.3V supply → 2V tuning range

**Analog processing**
- "High gain" - *SiPM gain calibration: Small range, low noise (ENC)*
- "Low gain": *Full SiPM dynamic range*
- 1.8V supply → Reduced power, but less headrooms

**Trigger branches**
- Event trigger
  - *initiate ADC conv., time stamp*
- HG/LG selection
**SiPM bias tuning**
2V tuning range
Resolution $\approx 8\text{mV/LSB}$

**Charge measurement**
Sufficient SNR to operate 10\(\mu\)m MPPCs

Dynamic range for INL $\leq 1\%$
$\approx 2.8\text{pC}$ (High gain)
$\approx 160\text{pC}$ (Low gain stage)

![Graph showing SiPM bias voltage tuning](image1)

![Graph showing HG stage linearity](image2)

Single pixel spectrum using 10\(\mu\)m MPPC
SAR ADC development for KLauS

1 ADC per front-end channel

Development of low power, fully differential SAR-ADC

Two operation modes:
MIP quantization – **10bit resolution**
9+1(sign) bit SAR ADC

SiPM gain calibration – **12bit resolution**
Additional pipelined stage (8 bit SAR)
Residual amplification & digitization

First prototype:
DNL larger than expected (layout bug)
Will be improved in next version
Multi-channel prototype

Taped out 7 channel prototype
Expected back in September
1.5 x 4.5 mm² miniASIC (Final 36 channel chip size 5x5mm²)

7 Front-End + ADC + digital channel control modules

Digital part & readout options
Structured as future 36 channel version
Implemented “Testbeam” & “Japanese” features
e.g. event validation, coincidence logic, hit counters, etc

fast LVDS interface (160Mbit/s 8b-10b encoded)
I2C interface + redundant link
Power consumption & gated operation

DC power consumptions
Channel \( \approx 2.9 \text{ mW} \)
Shared bias block \( \approx 2.4 \text{ mW} \)

Power pulsing with 1% duty cycle
*Extrapolated to 36 channel chip:*

39 \( \mu \text{W/ch} \) for all analog blocks
*Front-end & ADC, Bias block ; no digital part*

Power-up cycle
Pedestals stable after \( \sim 10-15\mu \text{s} \)
Duty cycle can be reduced towards 0.5%

\( \rightarrow 25\mu \text{W goal well in reach} \)
DESY contributions to WP4 task 3

DESY and OMEGA cooperate since 2004 on development of calorimeter readout electronics:

- OMEGA: design and first tests
- DESY: multi-channel characterisation and system integration

Examples of measurements at DESY

- behaviour in larger systems
- interplay with SiPMs, influence of pulse shapes
- power-pulsing behaviour
- long term stability
- coherent noise
ASIC developments and tests

- **SPIROC2B**
  - working horse in all test beam prototypes
  - some bugs and rare instabilities found

- **SPIROC2C and D**
  - intermediate bug fix versions
  - additional features
  - extensive tests at DESY
  - DESY feedback for new version

- **SPIROC2E**
  - in production now
  - foreseen for next large calorimeter prototype
  - new BGA package in design

- **SPIROC3**
  - future version with I2C link and possibly independent channels
Summary & further development

KLauS3 development
• SiPM readout ASIC targeting low gain, high density SiPMs
• First multi channel SoC ASIC submitted
• 36 Channel version planned for 2017

System level ASIC characterization & operation
• ASIC in a “real environment” - Critical for Design maturation
• New version 'E' of SPIROC2 coming soon
  BGA package → new test-board closer to real hardware being developed
• The chip for next larger prototypes
Backup slides
Common gate & current feedback

$$R_{\text{in}}^{\text{DC}} = \frac{1}{g_{m1}} - \left( \frac{g_{m3}}{g_{m2}} \times \frac{1}{g_{m4}} \right)$$

Nominal input impedance $\sim 50\Omega$

150uA bias current @ 3.3V

SiPM Bias voltage tuning
['DAC' $\rightarrow$ 'feedback' $\rightarrow$ input]
~ 2V tuning range
Low power 8bit DAC
2nA / LSB

Power gating compatible
Small DC input voltage change in low power mode
Front-End, ADC & channel digital control

Digital sources from front-end:
- External / self generated trigger
- Gain selection result
- Trigger output to digital part:
  - Coarse counter registration
- Hold signal for ADC

FE hitlogic block:
- Initiate conversion after peak sampling
- Handshake with ADC control: start, busy
- Mask trigger pulses while ADC is busy
ADC input selection

ADC sources from FE:
- High gain branch signal
- Low gain branch signal
- External source (ADC calibration)
- External / self generated trigger

Selection:
- By configuration
- Automatic: HG/LG
  Additional comparator in FE
- Selection decision annotated to event
**L0 & Coincidence event validation**

**First level event validation:**
No validation flag - ADC conversion cancelled
→ Also reduces dead time

**Validation signal sources:**
- External source
- Internal validation:
  Coincident events between channels
  Configurable OR of group of 12

→ Validation window 1..8 Clock cycles
→ External validation:
  maximum delay: ~300-500ns
Linear range for different VCC

Charge injection measurements
Cd=33pF

Voltage drop in supply lines expected

→ Check linearity for different VCC
“LL” corner: VCC18=1.6V ; VCC33=3.1V
“TT” corner: VCC18=1.8V ; VCC33=3.3V
“HH” corner: VCC18=2.0V ; VCC33=3.5V
Two DACs to tune threshold:
- Global 6 bit DAC + scaling (for all channels)
- 4 bit DAC for fine-tuning (each channel)

→ Charge noise: 8fC typ.
→ Threshold configuration resolution (4b DAC): 5fC