University of Glasgow | Department of Physics & Astronomy

LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

MAX-PLANCK-GESELLSCHAFT

cea leti

OPEN 3D BOOST YOUR INNOVATION

CERN

TSV development with CEA Leti in the FEI4 chip

R. Bates, C. Buttar, L. Flores / Glasgow University

G. Pares / CEA LETI

A. Macchiolo, R. Nisius / MPI

E. Gkoukgoussis, A. Lounis / LAL

M. Campbell, K. Dette, H. Pernegger, P. Riedler, D. Schaefer / CERN EP Department

Goal

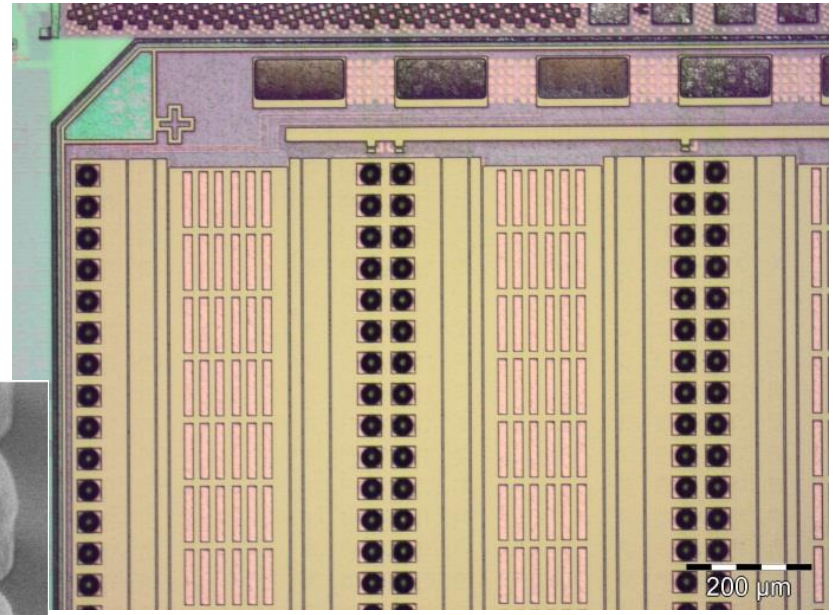
- **WP4 (NA3) Micro-electronics and interconnections:**
  - *Task 4.4 Interconnections and TSVs.*
- Interconnection of 65 nm CMOS readout chips to silicon pixel sensors by using through-silicon vias (TSVs) across the substrate, full qualification and testing.
- Fine pitch bump bonding techniques will be qualified by this WP

Contents

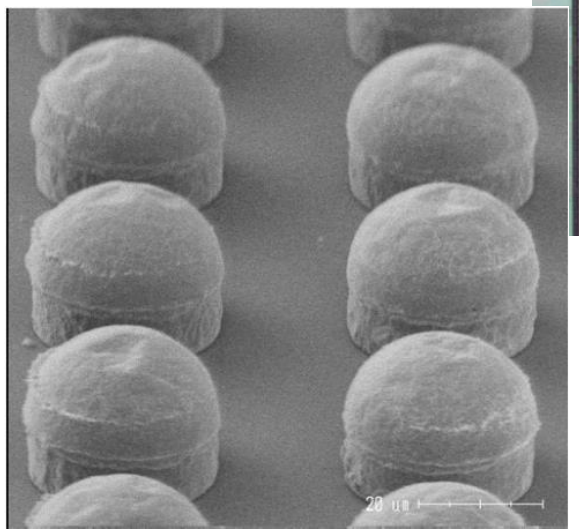
- Bump deposition at CEA LETI
- TSV project
  - Laser soldering
- Wafer bonding

Bump deposition at CEA LETI

- Developed process for SnAg solder capped copper pillars on FEI4 200 mm wafers
  - Minimum pitch 50 µm in one direction
  - 10µm Cu & 8µm SnAg solder cap
  - Electro-chemical deposition of bumps on seed layer



- High yield (<99%) obtained after significant effort on process
- Future work to transfer this to 300 mm wafer line for RD53 pixel chip

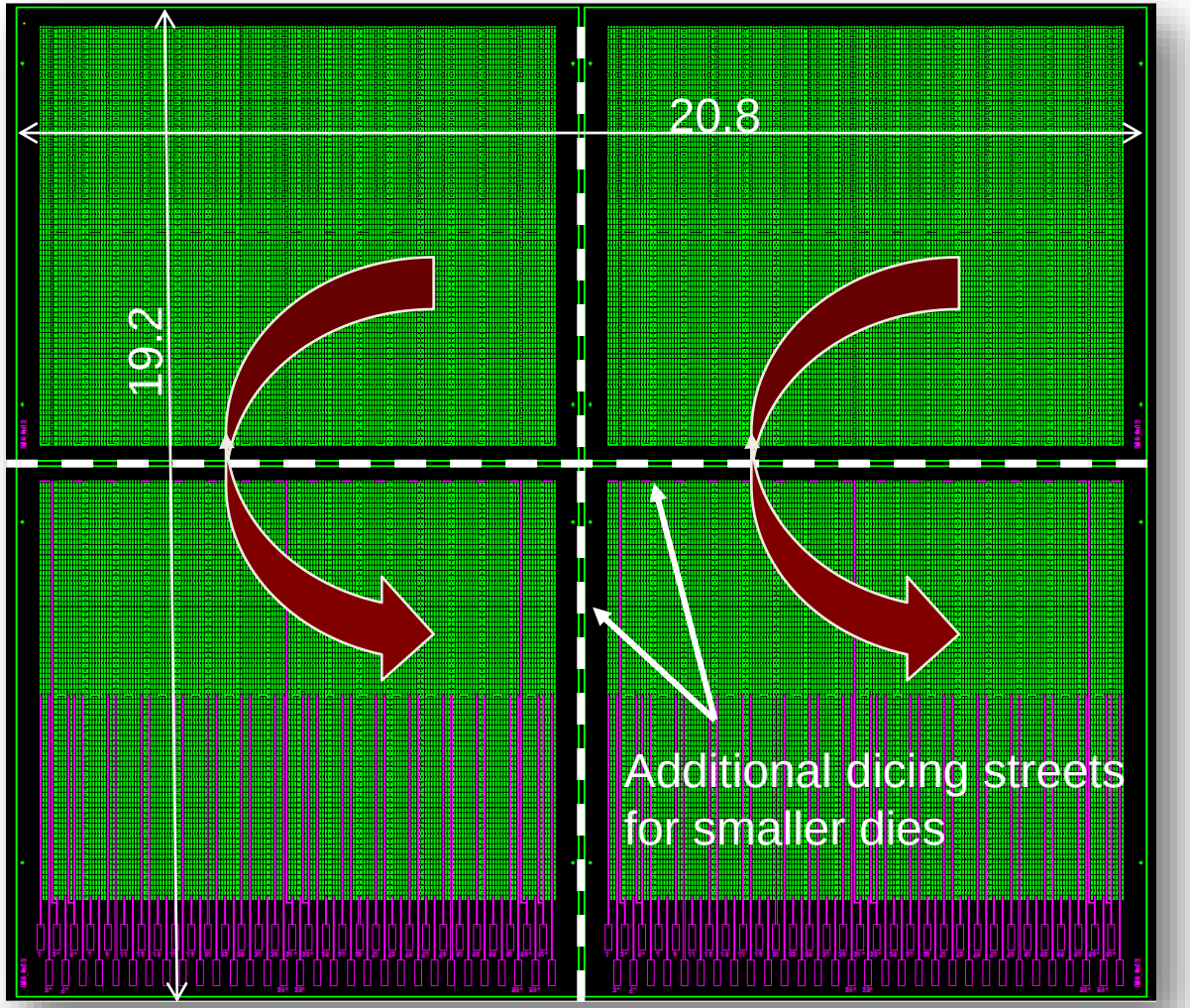


RD53 chip preparation

- Process will be different on RD53 wafers
  - Difference in tool set on 200 mm and 300 mm wafer lines
  - 50 µm pitch in both x & y direction
  - Difference in chip surface topology
- Building a test wafer for bump deposition and wafer handling tests
  - Presently obtaining quotes
- Daisy chain feature to measure bump and flip-chip yield
- Allows:
  - Early access to 300 mm wafer bump deposition experience
  - 300 mm wafer handling, thinning and dicing
  - Use of automated visual inspection tool
  - Flip-chip practice on large high density arrays

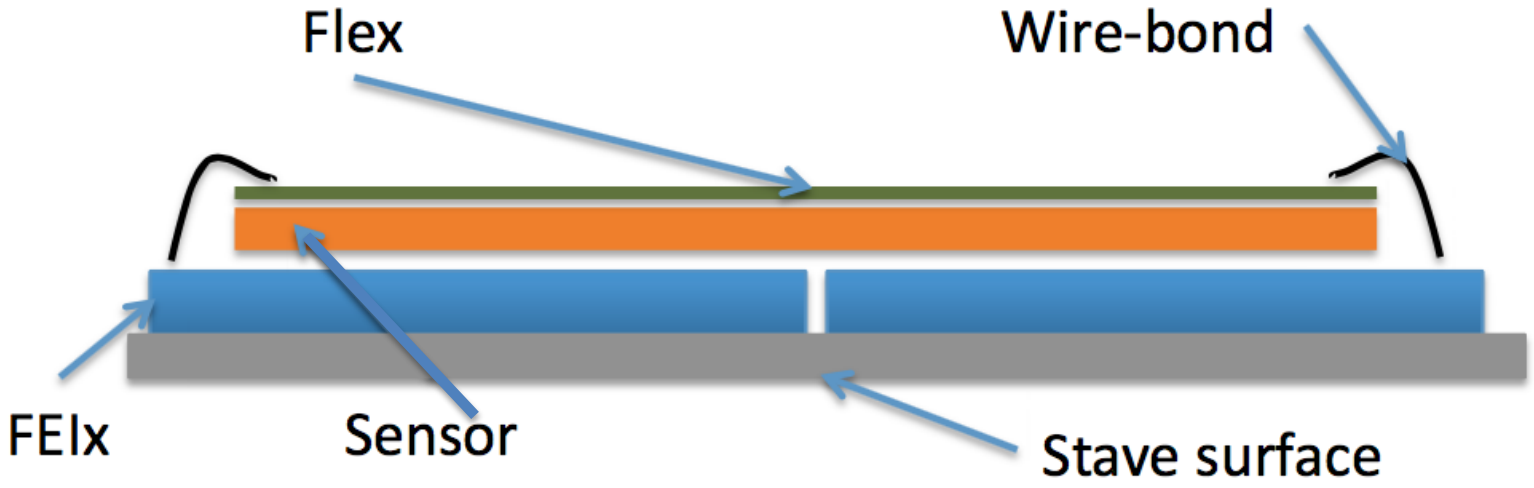
RD53 Daisy chain test wafer

- Example of FEI4 sized daisy chain
  - This one produced by Genova, Milano, Trento, FBK and Selex
  - 200 mm wafer fabrication
- **120 k-bumps/chip** with resistive chains
  - 5 x FEI4 bump density and number
  - 40k bumps electrical tested
    - Shorts and opens



Hybrid pixel modules

- Hybrid pixel are:

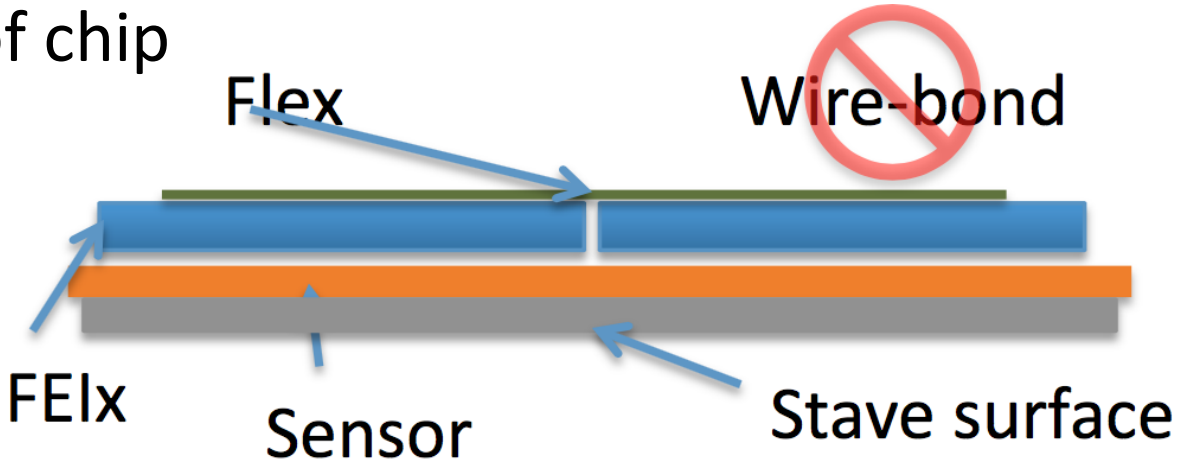


Inherent limitations

- Wire bonds connect FE to flex:
  - Oscillation in magnetic field
  - Protection required or desired “To pot or not to pot”
  - Limit on envelopes
- Access to bond area on FE limits the sensor active area (not 4- side buttable)
- Requires expensive die-to-die assembly
- Wire bond Inductance limits signal speed
- Edge access -> power distribution over large chip challenging

TSV module concept

- Using a TSV last process
  - Use existing chip set with post-processing technology
  - Build on Medipix experience with CEA Leti
- Remove wire bonds from the module
  - Connect flex via solder balls on back of chip
  - Less fragile module
  - Reduced interconnect inductance
- Remove wire bond pads
  - Reduced chip edge



- Compact, low mass hybrid pixel modules with minimal modification to the FE layout and using standard CMOS technology

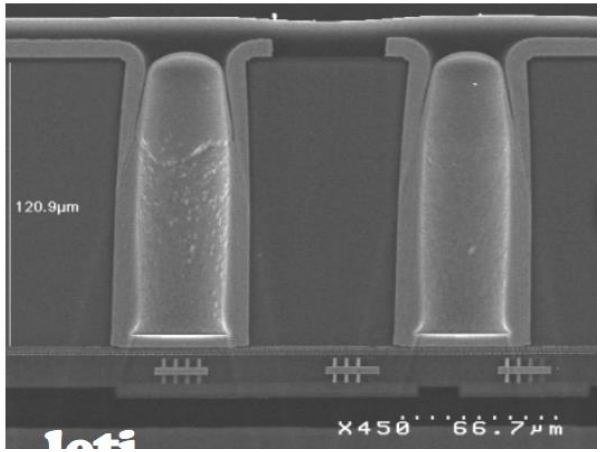
Wirebond less TSV enabling technologies

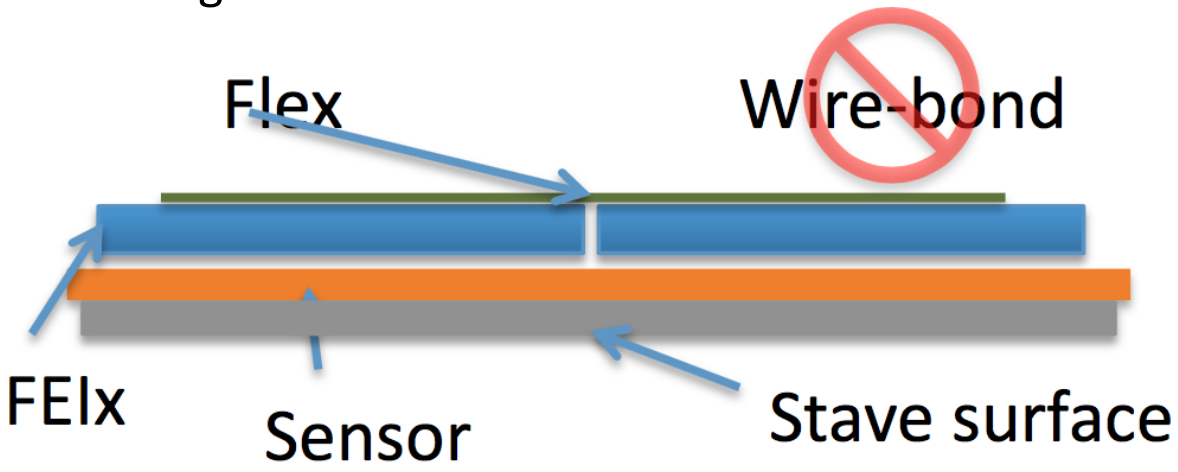
TSV-last + RDL

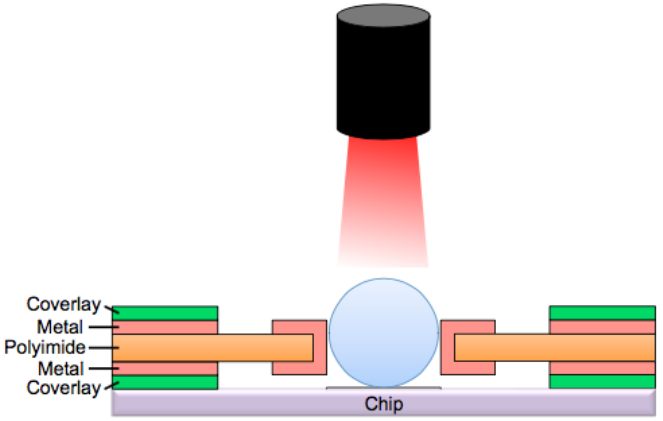
- TSV connect chip M1 from front to back of chip
  - TSV aspect ratio 2:1
- RDL distributes FEI4 connections over full chip surface.
  - Do not need fine-pitch connections.
  - Power can be brought to chip at several places , not just on the edge

Direct laser soldering: flex to FEIx

- Thin 2-layer Al flex
- No glue layer needed
- Connections are solder 1-by-1, module stays at RT
- Re-workable



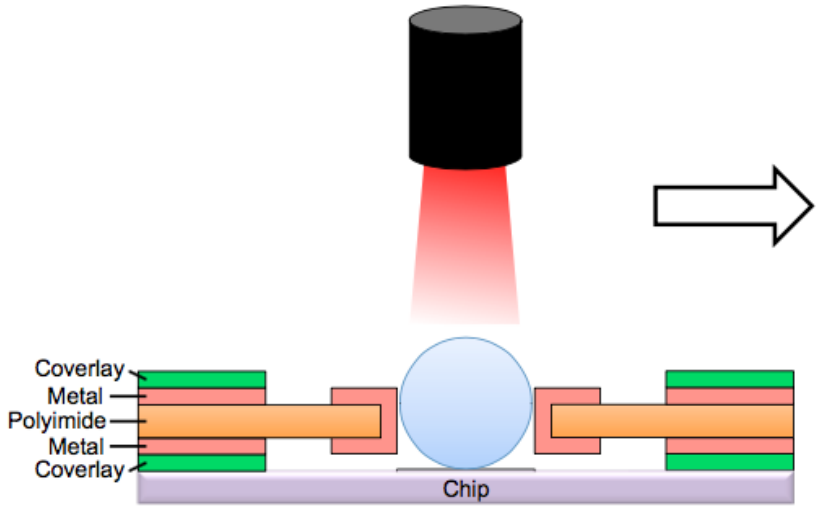


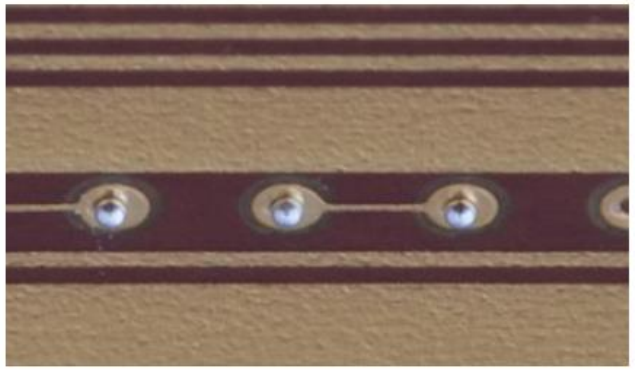


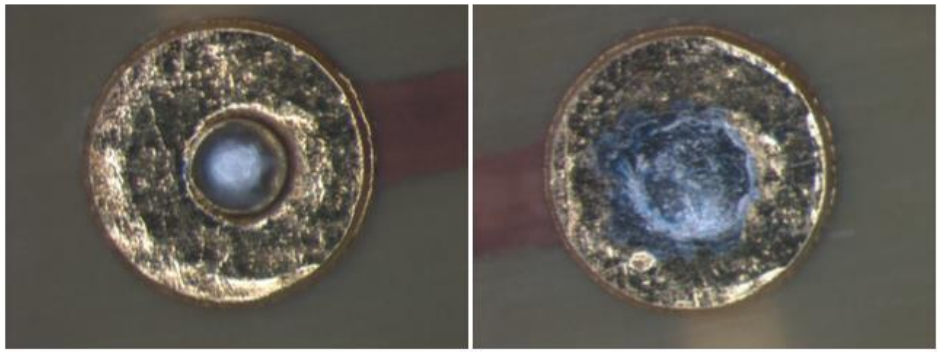
Direct laser soldering

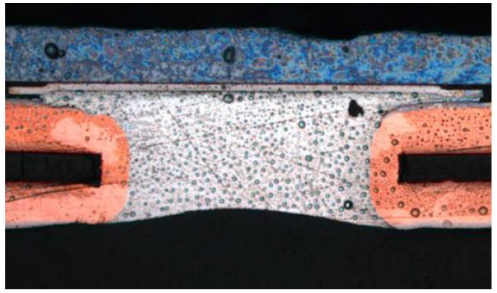
- Developed within the ALICS ITS project
  - Demonstrated & functional. Baseline for 10 m^2 of ITS assembly
- Flex is thin 2-layer Al on Kapton flex with Solder ball (200µm) inside which is melted by laser
  - No module heat up & No thermal stress on module
  - No glue is needed between flex and bare module
  - Solder holds flex mechanically well in place

P. Riedler, A. Di Mauro, A. Junique (PH-AID ALICE)







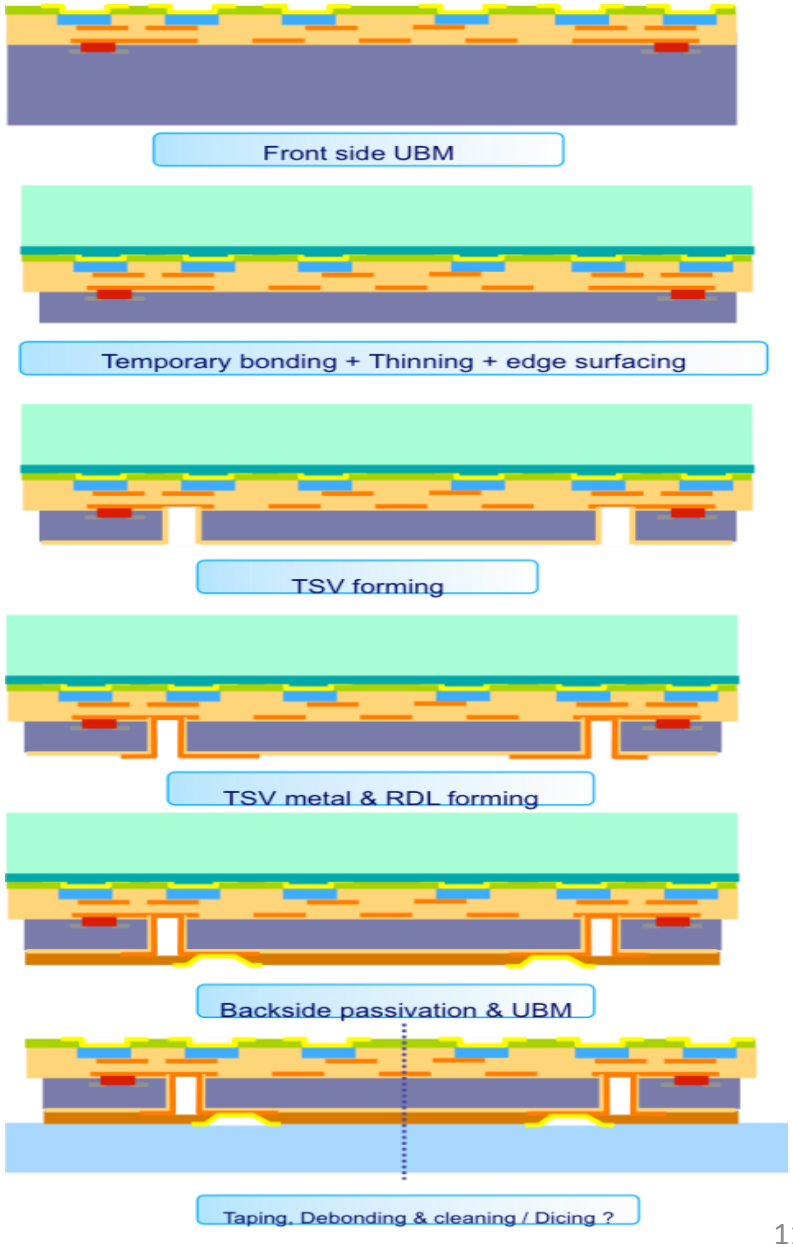


TSV + RDL project in FEI4

- Working with CEA LETI on TSV last process in FEI4
  - Connect chip M1 from front to back of chip via TSV
- Front side processing in two batches
  - UBM only (4 wafers) – solder on sensors
  - Bumps (3 wafers) – UBM on sensors
- Backside RDL distributes all FEI4 connections over full chip surface
  - Same specs as Medipix but with dedicated FEI4B layout for laser soldering to flex
  - Pad layout to compensate thermal stresses during reflow after flip chip (SCL)
    - Stress compensation has been previously demonstrated between Glasgow & LETI

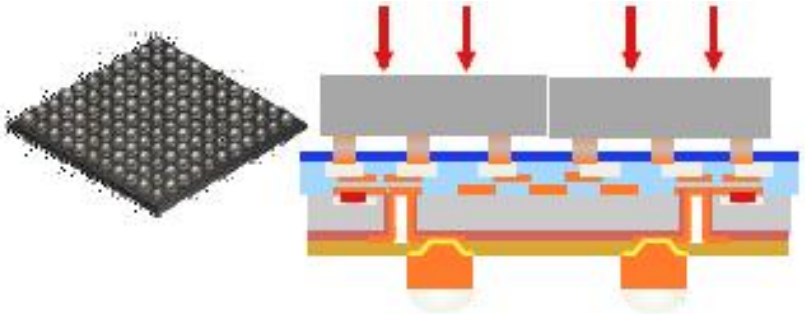
TSV process description

- Under Bump Metallisation is deposited on the front side of the wafer.
  - Identical to the step used normally by the bump bonding suppliers
  - Finished die can be flip-chip assembled to sensors with solder bumps.
  - Second batch with have solder bumps
- Wafer thinning
  - Wafer front side bonded using a temporary adhesive to a dummy support wafer.
  - The wafer is thinned to 120 um (2 times the diameter of the TSV opening).
- TSV formation
  - Vias are drilled in the wafer using deep reactive ion etching
  - Vias are coated conformally with an insulating layer.
  - Contact holes are etched through the insulation in the bottom of the vias
  - 5um thick Cu layer is deposited on the side of the vias and on the back side of the wafer.
- Redistribution layer
  - The Cu layer is then etched to form the redistribution layer on the backside.
  - The back side of the wafer is passivated and the openings for the solder contacts etched.
  - UBM metallization deposited on the solder pads the same way as on the front side.
- Wafers are probed for electrical functionality
- Die release
  - Wafers are released from the support wafer and transferred onto a dicing tape.
  - Wafers are shipped for subsequent dicing and flip chip assembly.

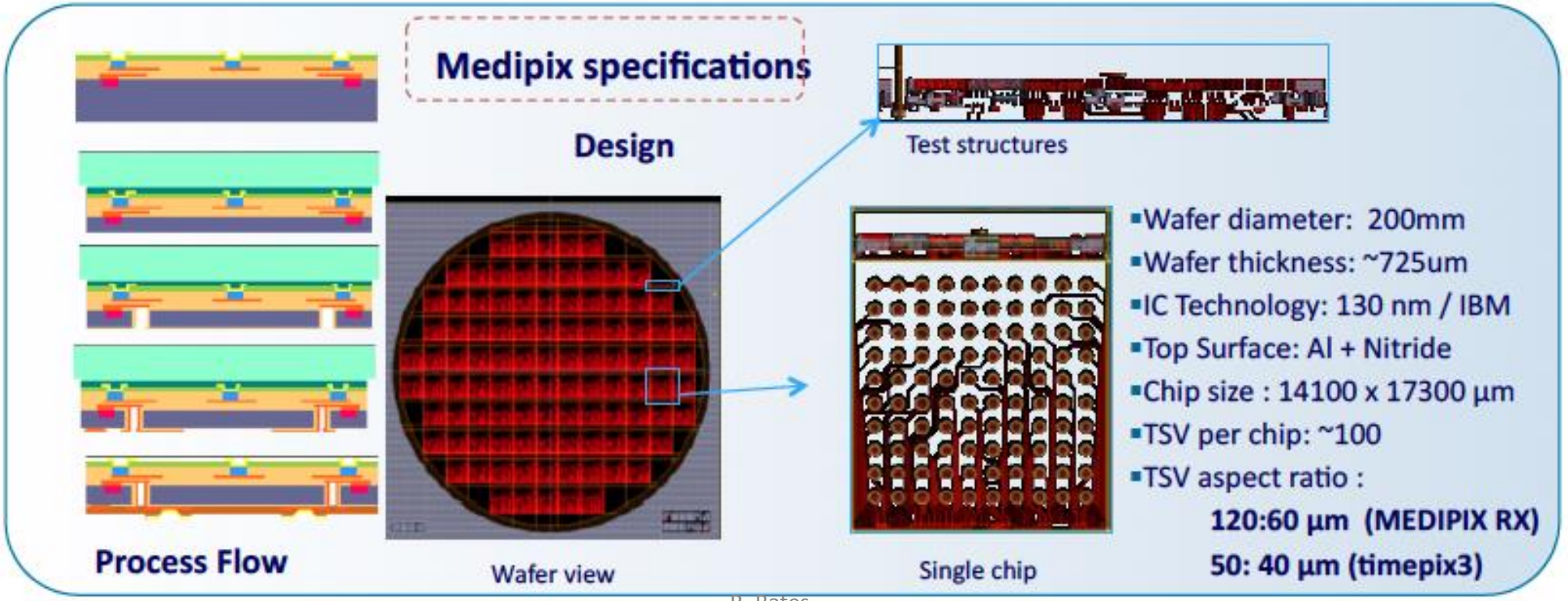


Medipix/LETI TSV + RDL experience

- Medipix & LETI developed TSV on Medipix IBM chip to allow for BGA assembly for buttable X-ray/ particle detectors

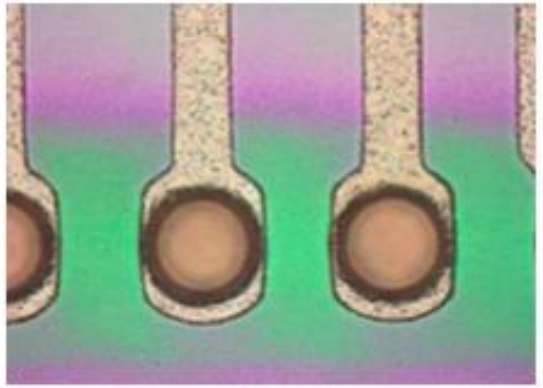


M.Campbell /CERN-PH – G.Pares / CEA-LETI

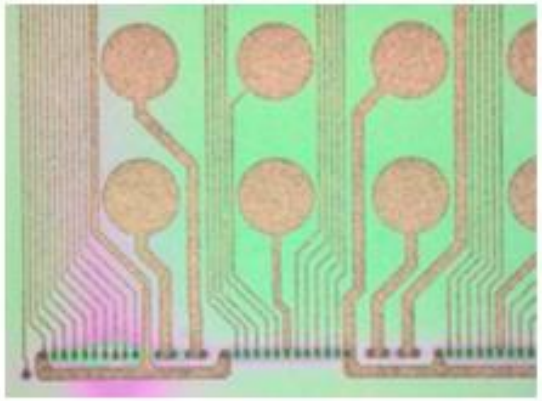


TSV last from Leti on Medipix wafers

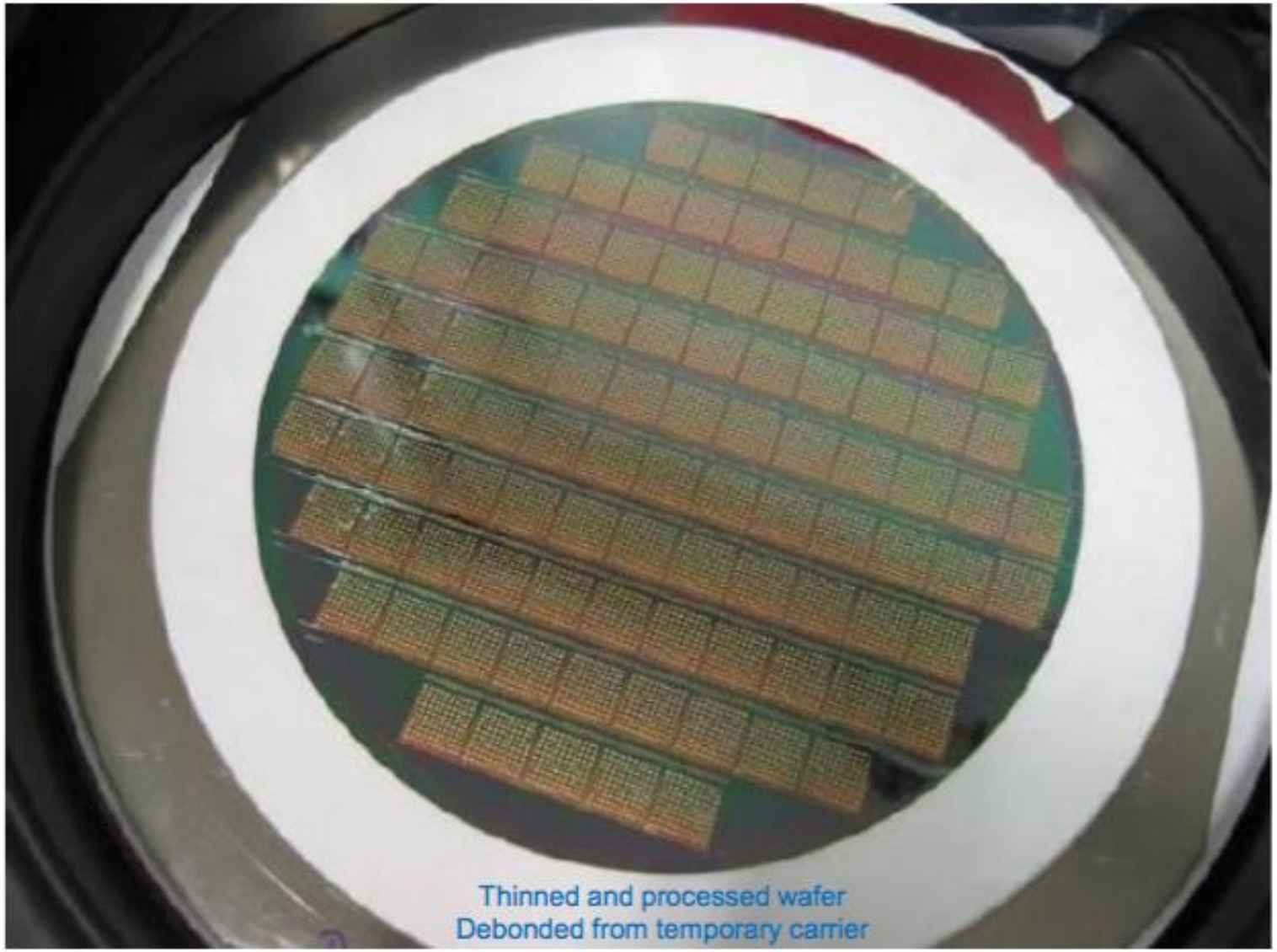
- Second run processed 6 wafers of Medipix3RX
- TSV yield ~ 70% to 80%



Through Silicon Vias diameter 60 µm
Wafer thinned to 110-120 µm



Redistribution layer
Back side of Medipix3 chip

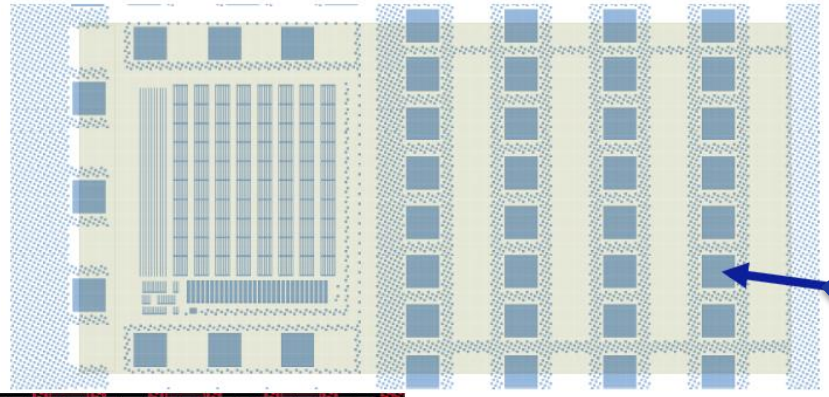


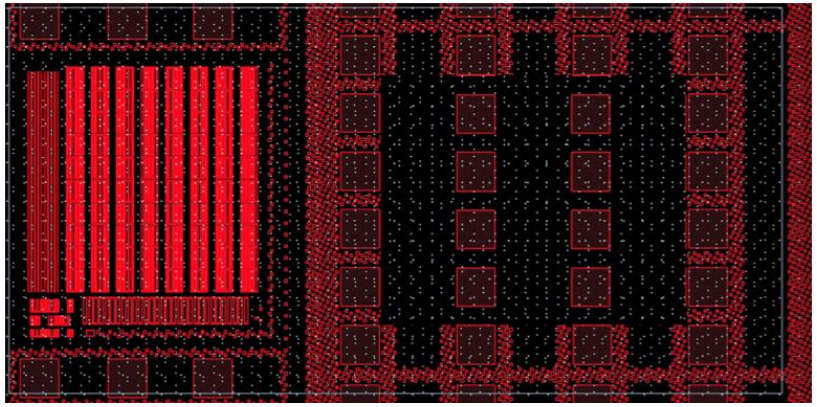
Thinned and processed wafer
Debonded from temporary carrier

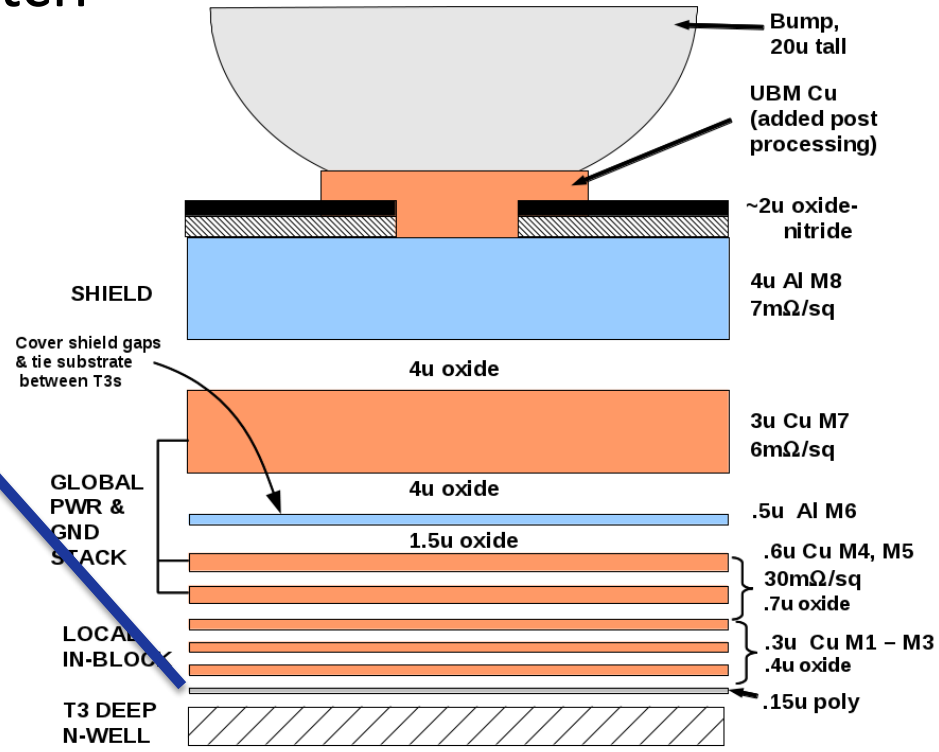
Images courtesy of CEA LETI

TSVs in FEI4

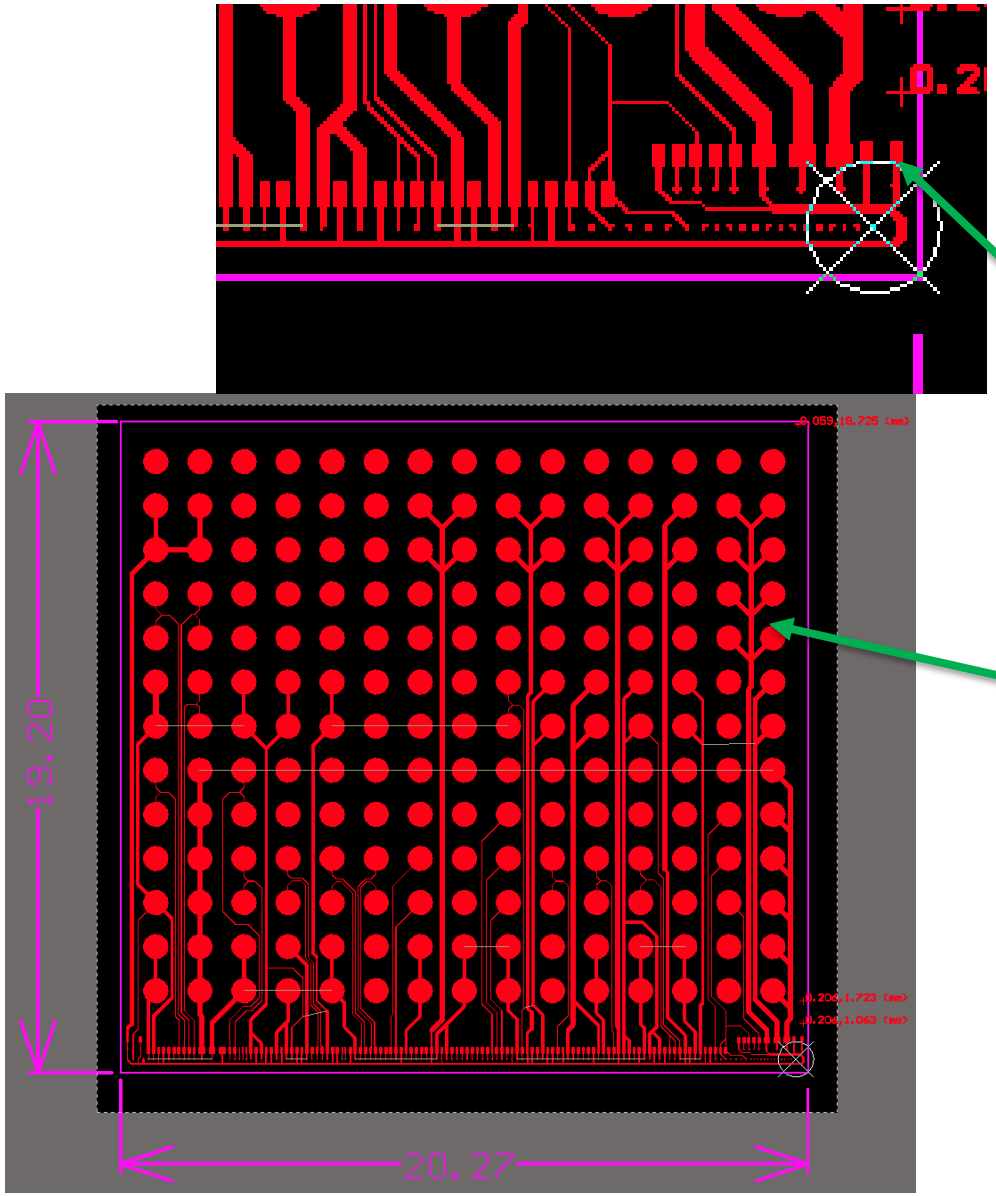
- Require access to M1 from the chip backside
- During MPI TSV project with EMFT understood that there was poly-Si under M1
  - Poly-Si causes issues with the TSV etch
- Last 72 wafers have reduced poly-Si to aid TSV etch







FEI4 ReDistribution Layer



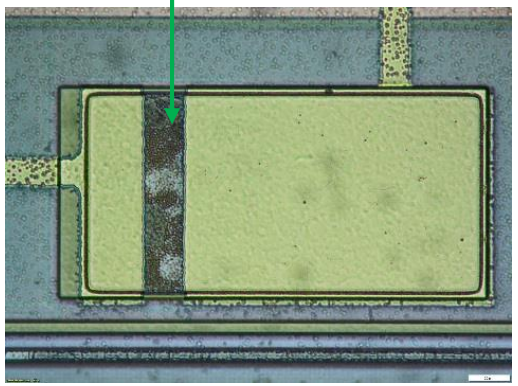
- **FEI4-B RDL design** completed at CERN
  - Design reviewed with LETI and ATLAS Module/ FEI4-experts https://indico.cern.ch/event/ 459471/
  - Include probe pads/wire bond pads near TSV to allow testing with mirrored test card after processing or wire bonding after processing
  - Large solder pad array compatible with direct laser soldering
  - Solder pads over full chip to compensate thin die bow
  - RDL mask processed at LETI
- RDL metal stack compatible with BGA solder technology

Present TSV status

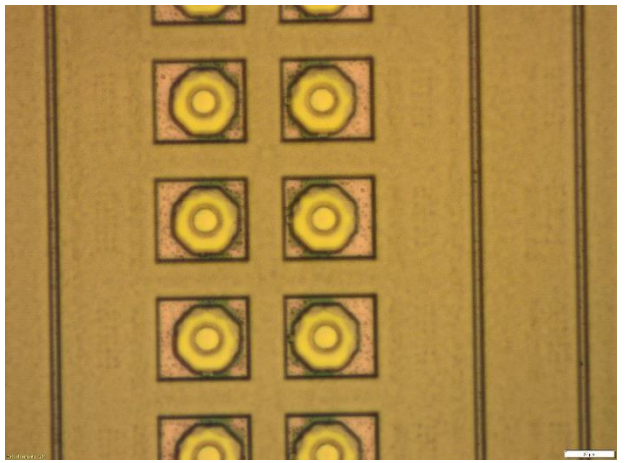
- Front side UBM deposition done
  - Good electrical characteristics of UBM
- Wafers bonded
- Thinned to 120um (need to check this number)
- TSV Photolithography done
- Oxide mask for deep etch done
- TSV etching in 2 weeks!
  - Detailed visual inspection to confirm etch to M1
- TSV oxide liner and filling in the weeks after TSV etch
  - 1-2 months before we get the wafers!

Front side UBM

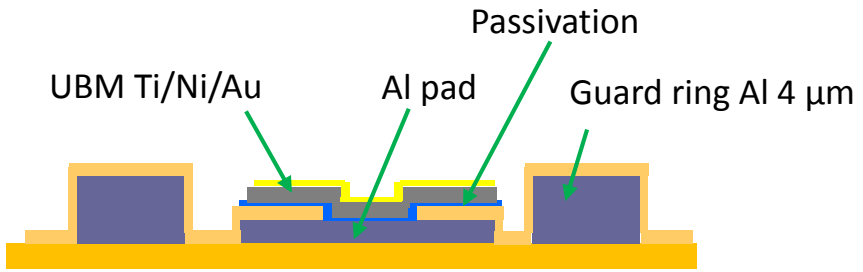
- Electrical characterization
  - Results in line with expectation on UBM layer
    - Critical dimensions
    - Sheet resistance
    - Planar insulation
    - **Contact with Al pads**



Contact structure on pad



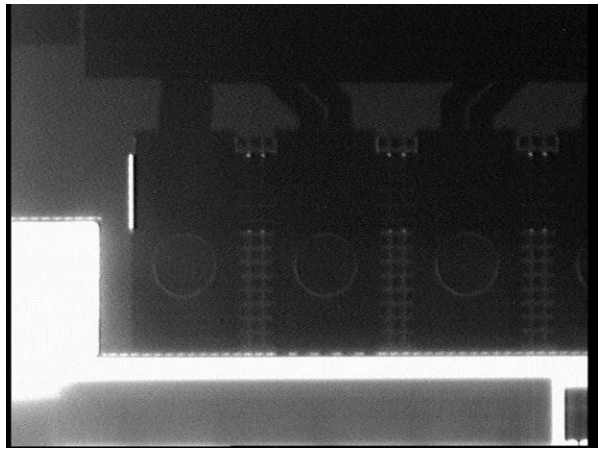
UBM pads – optical inspection



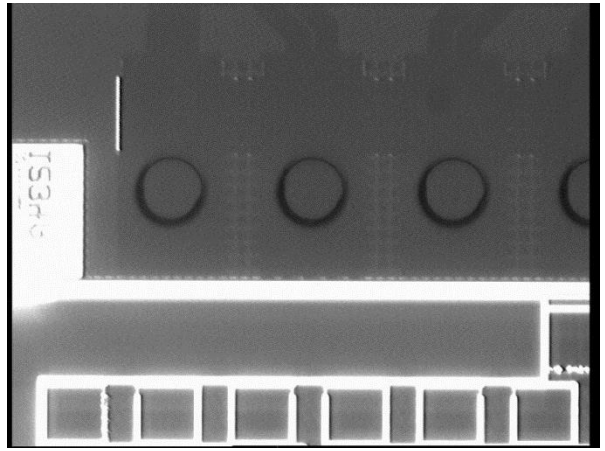
TSV last – Oxide etch mask

- IR image of Oxide DRIE mask
- Circles are mask
- Good alignment to M1

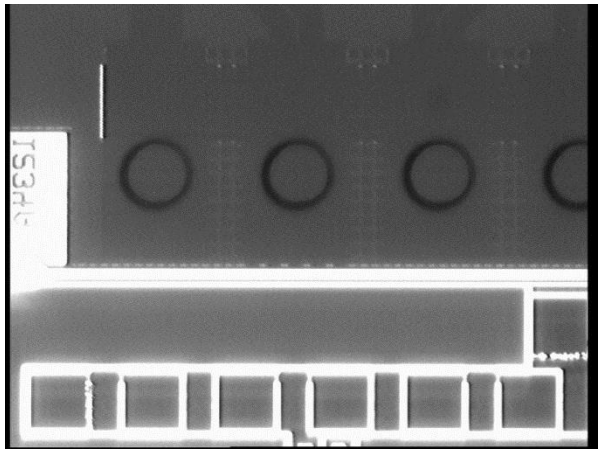
Wafer 01



Wafer 02



Wafer 03



Post TSV testing & assembly

- Wafer level chip testing
  - On probe station
  - Electrical contact to chip via TSV, probe on mirrored pad array
  - Probe card re-designed
    - Some connections made on RDL not required
    - Inverted needle stack as probing from the back
  - DAQ ready
- Aluminum flex PCB for laser soldering
  - Designed
  - Soldering trails with dummy parts taking place
  - Medipix scrap parts will be used
- Flip-chip to sensor to take place after bare chip testing
  - Sensors with solder bumps ready at Advacam

Wafer to wafer bonding

- Possible to join wafers without solder bumps using direct bonding
  - FE & sensor wafers post processed with copper layer
  - Wafers polished very smooth and flat
  - Wafer aligned, bonded (Van der Walls force), bond annealed to 400C, wafer thinned, TSVs added
  - Pixel assemblies diced from the wafer
  - Works for passive and CMOS sensors
- Requirements
  - Tight requirements on surface finish
  - Requires TSVs in the readout chip
  - Sensors must match readout chip on wafers
- Large area sensor wafer development with Infineon
  - Strip sensors on 200 mm wafers developed with CMS
  - n-in-p pixel sensors development started
  - Collaboration of experiments (ATLAS, CMS, CLIC, LHCb, MEDIPIX) to investigate suitability of the process (process split foreseen, especially for inter-pixel isolation doses)
  - Waiting on process trails at Infineon for modified pixel design rules
- Aim for FE-I4 single chip sensor wafer production to investigate feasibility of wafer-to-wafer interconnection in conjunction with TSV project at CEA-LETI

Summary

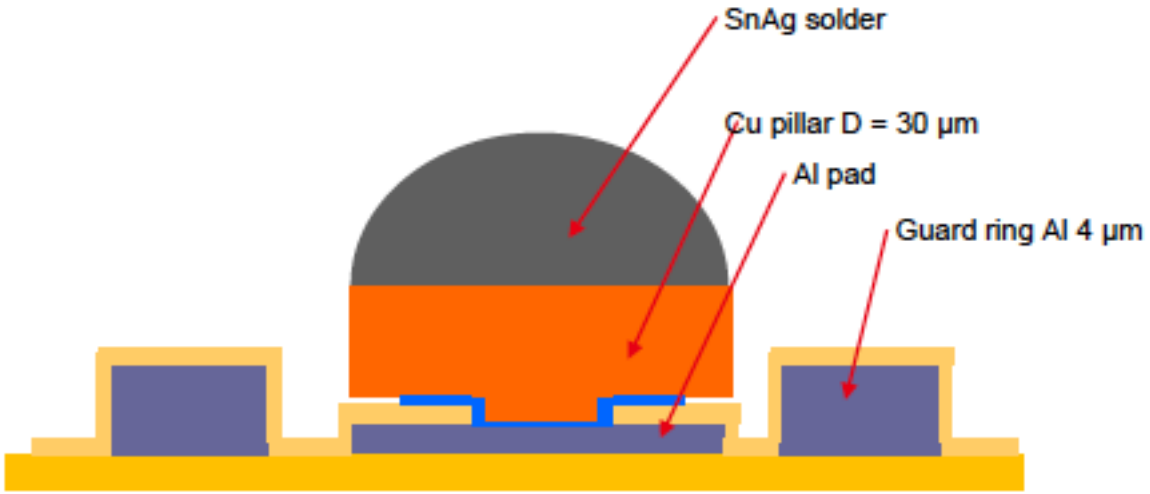
- TSV and laser solder module concept worked out
- CEA LETI TSV process well demonstrated on Medipix chip set
- FEI4 chip set modified to aid TSV formation
- TSV + RDL design done
- Wafer front side processing finished
  - UBM only wafers. Bumped wafers to start now
- TSV etch about to start
  - 2 weeks for etch, 1-2 months for finished wafers
- Testing and laser solder processes understood
  - Probe card designed
  - Laser soldering trails about to begin with Medipix items

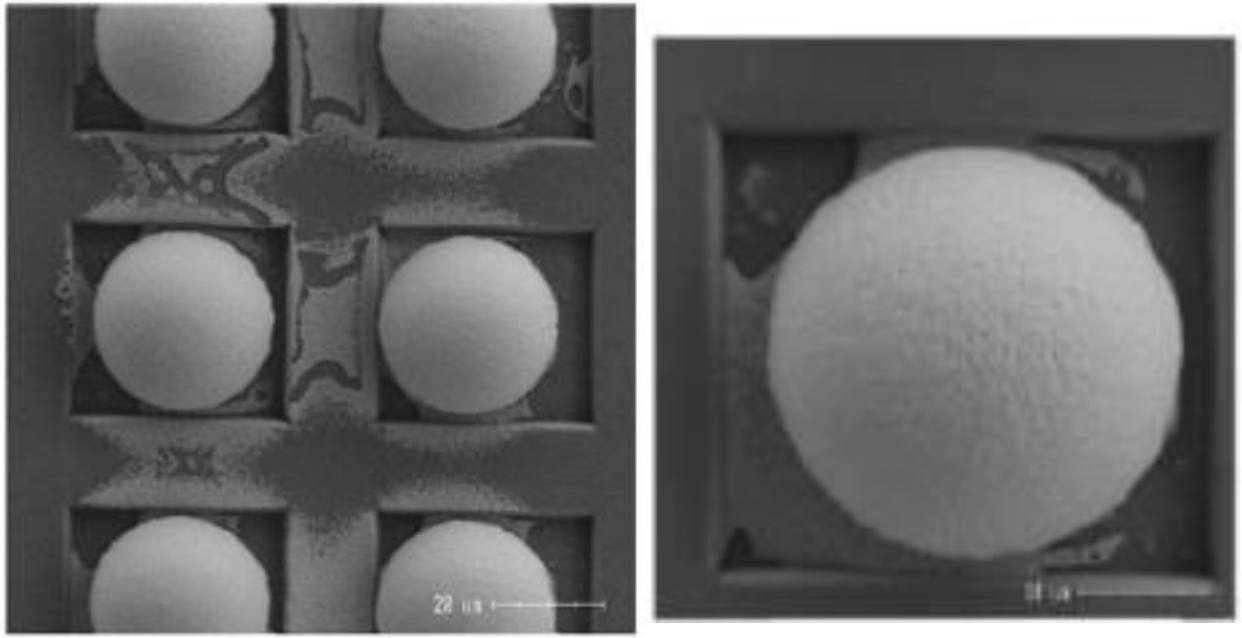
University of Glasgow

Backup

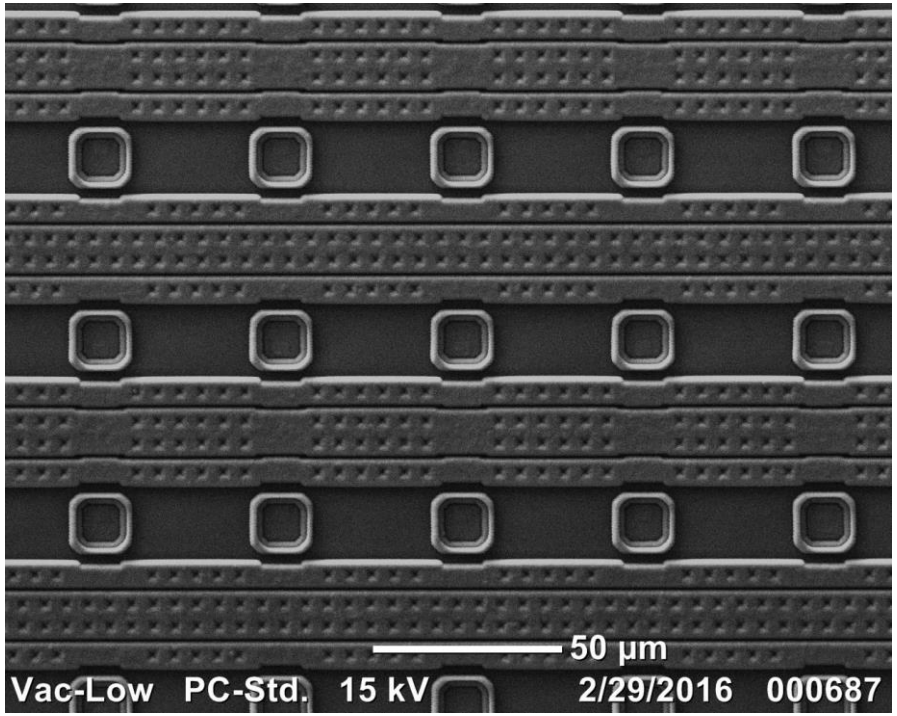
Topology of FEI4 wafer

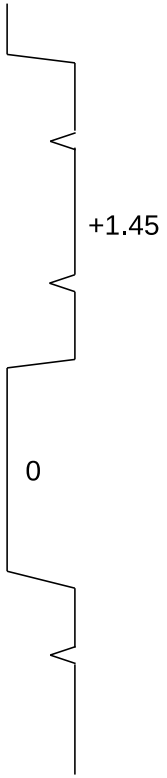
- 4 µm ring around the bump bond pad
- Topology caused seed layer etch issues
- Required long etches -> over etching of pillars

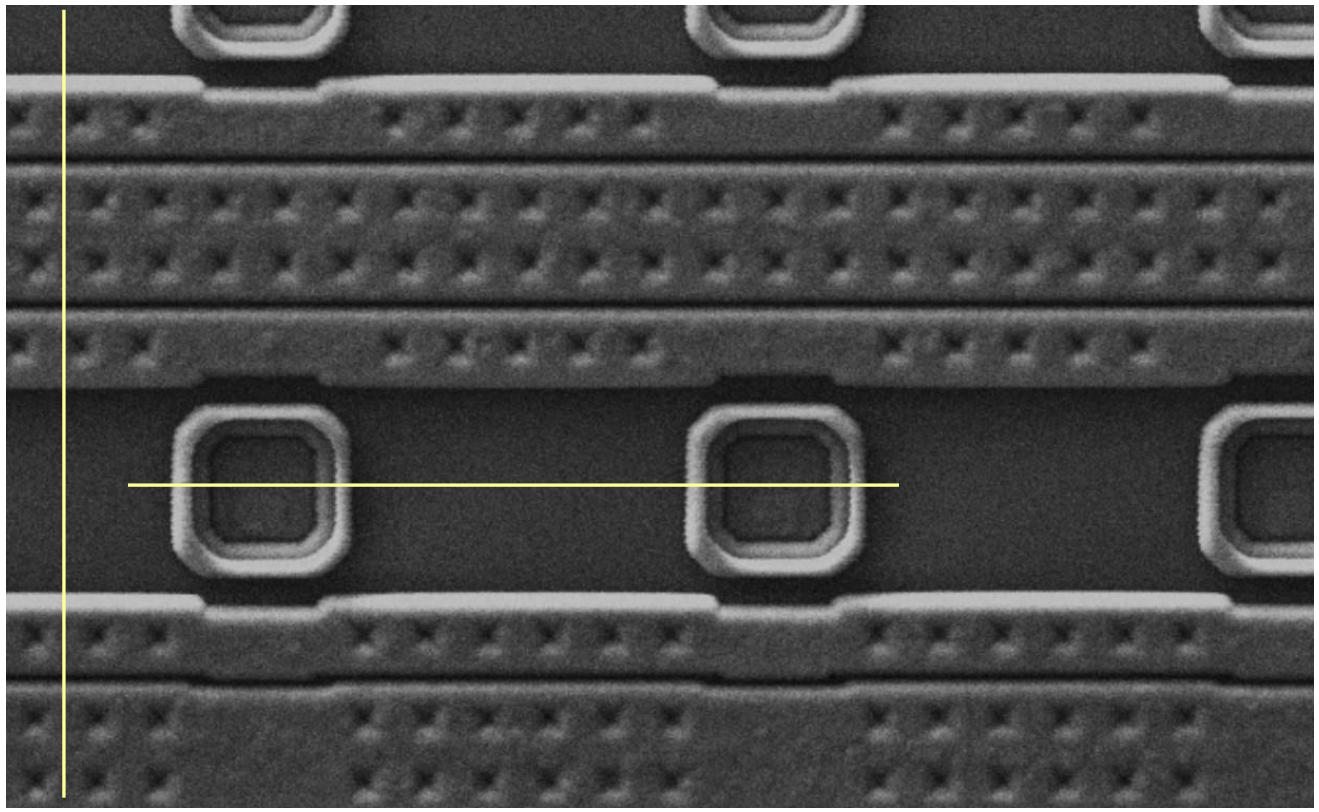


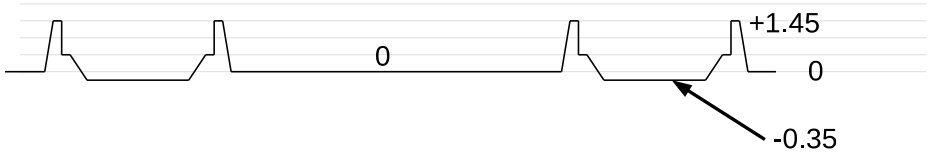


Topology of TSMC RD53 chip









Expect processing to be easier

- More open structure
- Lower height of enclosure around the bump pad