



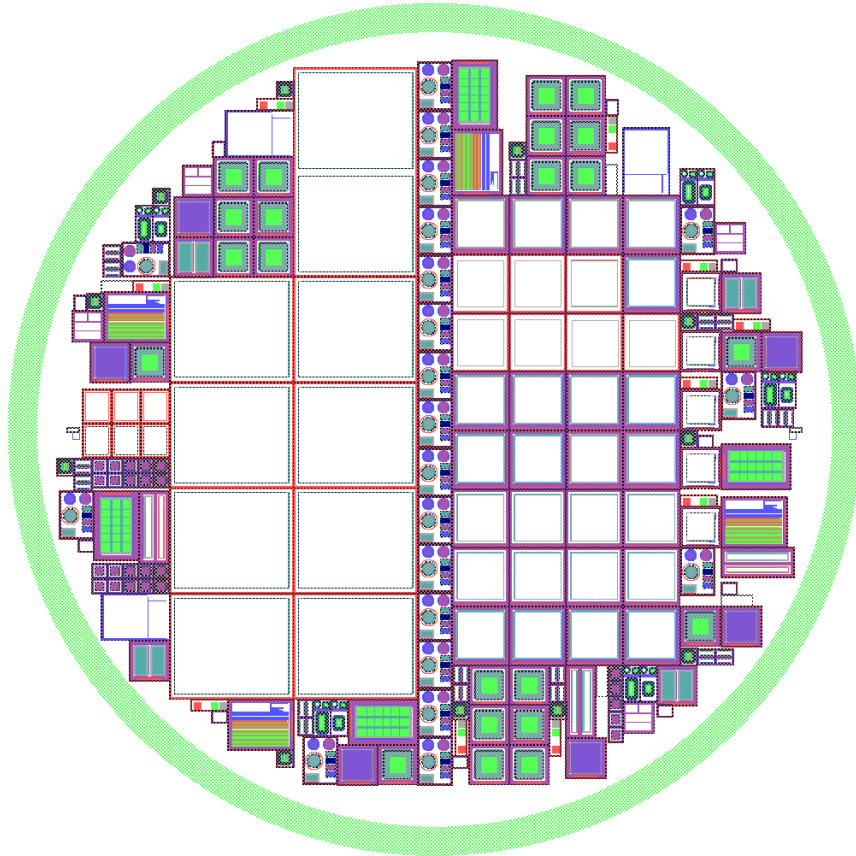
# Fondazione Bruno Kessler Centre for Materials and Microsystems

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## FBK in AIDA2020

- Si pixel on thin material : Si-Si and SOI
  - Planar pixel on Si-Si (100 and 130 um thickness)
  - 3D on thin substrate ( Si-Si)
  - Active Edge ( design completed)
    - *Project INFN-FBK "RD\_FASE2"*
- LGAD
  - Planar pixel on Si-Si (100 and 130 um thickness)
    - *Project MEMS : INFN Torino and FBK*

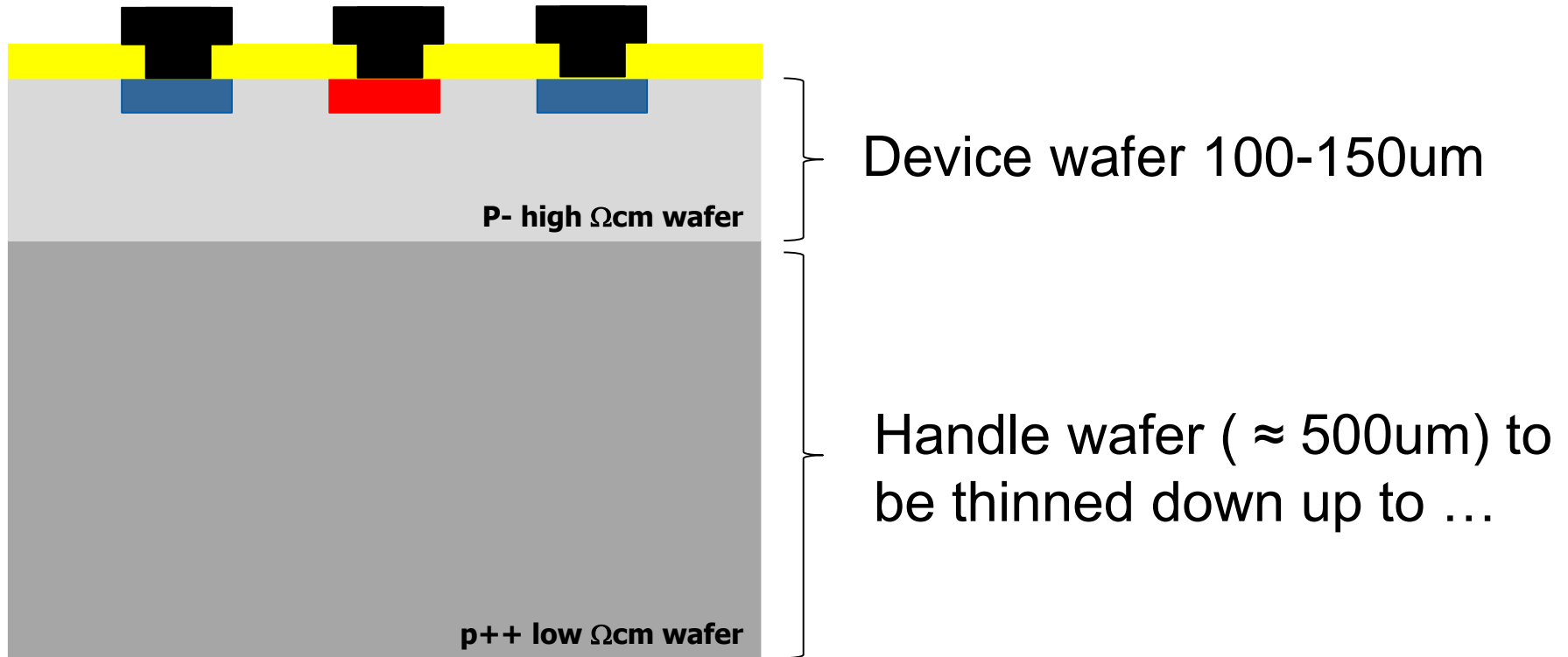
# Planar technology 1/3



- n-on-p technology
- Isolation by p-spray & p-stop
- Device layer 100 and 130um, support wafers 500um
- ATLAS & CMS pixels; test structures

Qualify the starting material

# Planar technology 2/3



Metal deposition on backside (if needed) after thinning

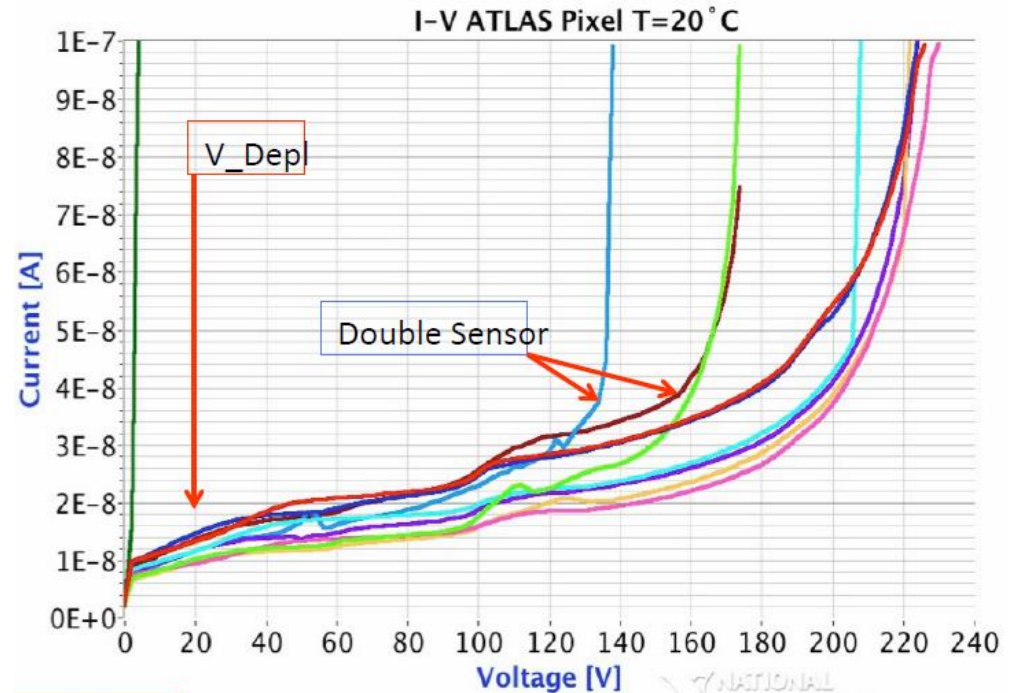
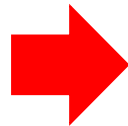
# Planar technology 3/3

V depl

16V for 100 $\mu$ m

20V for 130 $\mu$ m

ATLAS FE-I4 IV

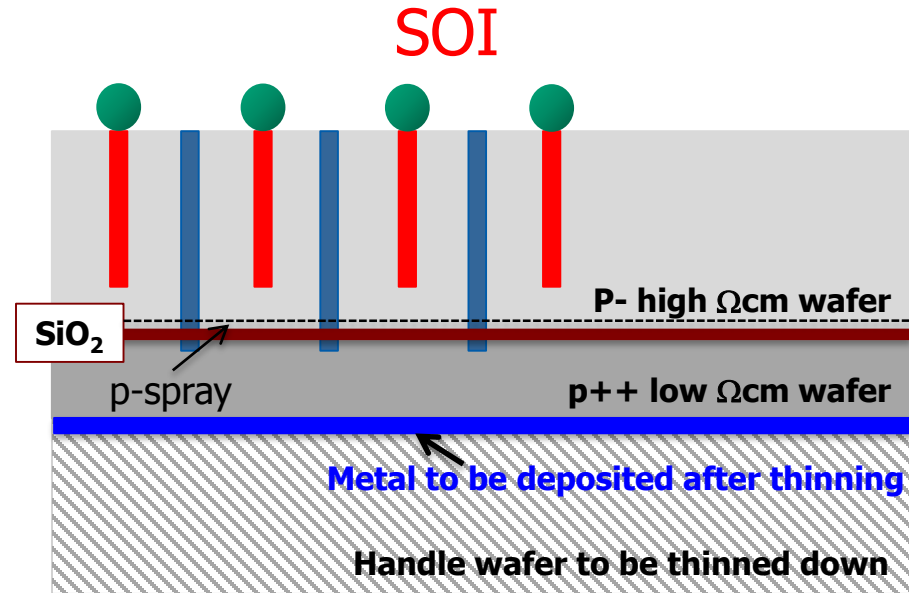
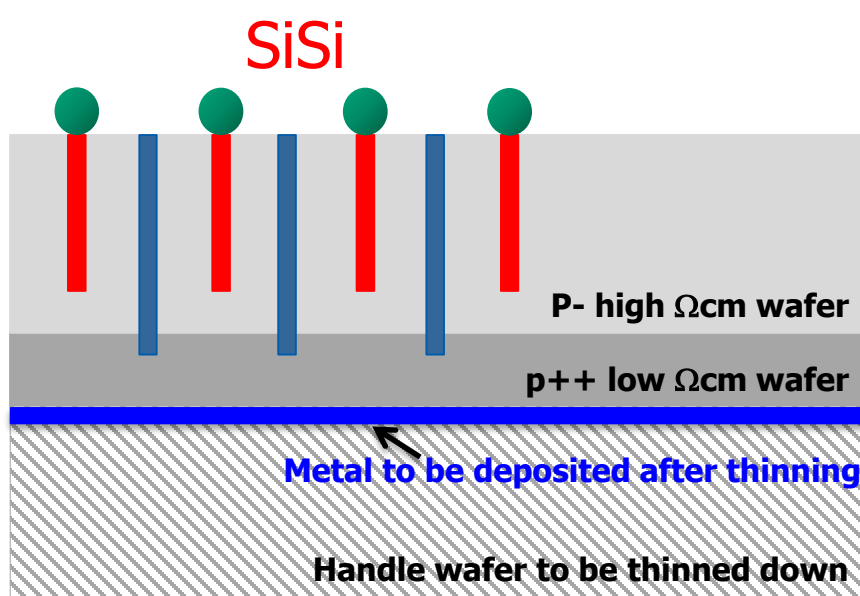


For more info see Marco Meschini talk

«Recent progress in AIDA2020 related activities in Florence»

# New single-side approach to 3D pixels

Double-sided process not favoured for thin sensors, especially on 6" wafers



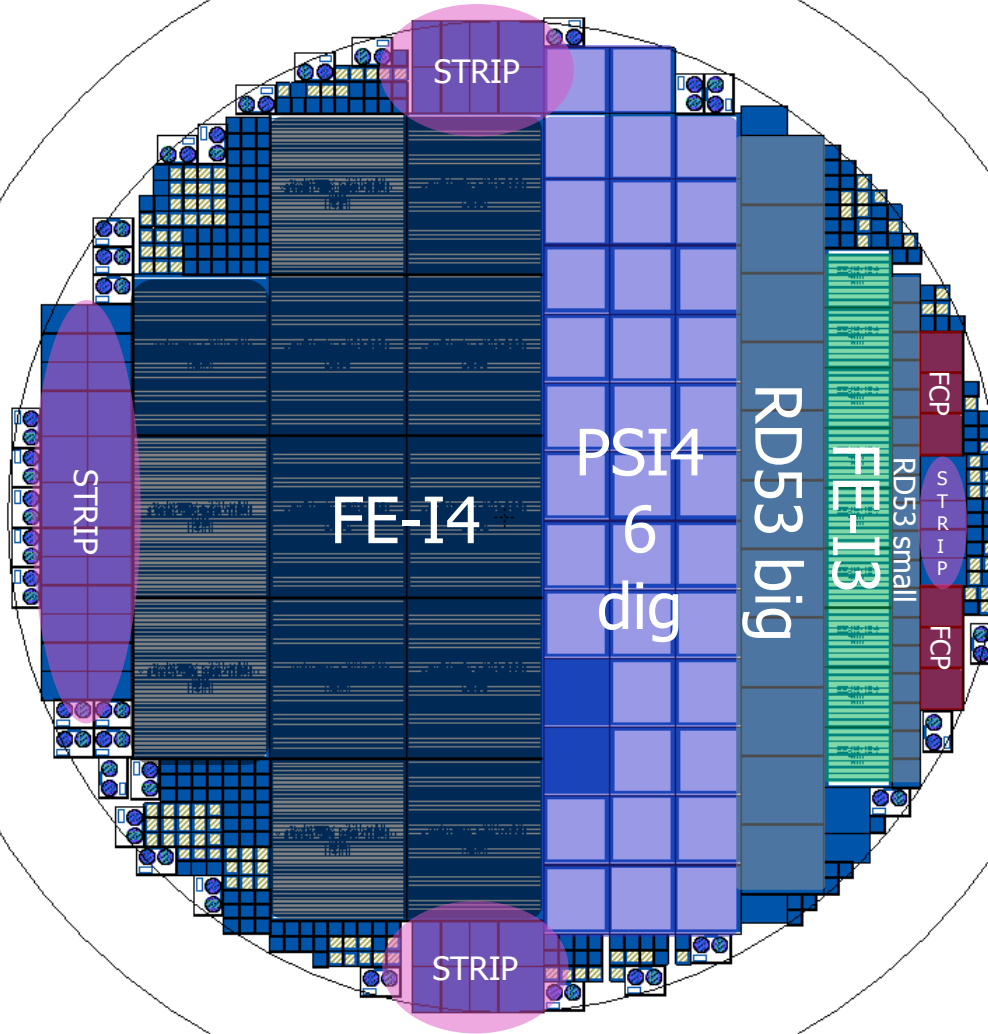
- Thin sensors on support wafer: SiSi or SOI → Substrate qualification
- Ohmic columns/trenches depth > active layer depth (for bias)
- Junction columns depth < active layer depth (for high  $V_{bd}$ )
- Reduction of hole diameters to ~5  $\mu\text{m}$
- Holes (at least partially) filled with poly-Si

Process  
Tests

# 3D Pixel Wafer Layout

Thanks to Dalla Betta

Many different pixel geometries and pitch variations:



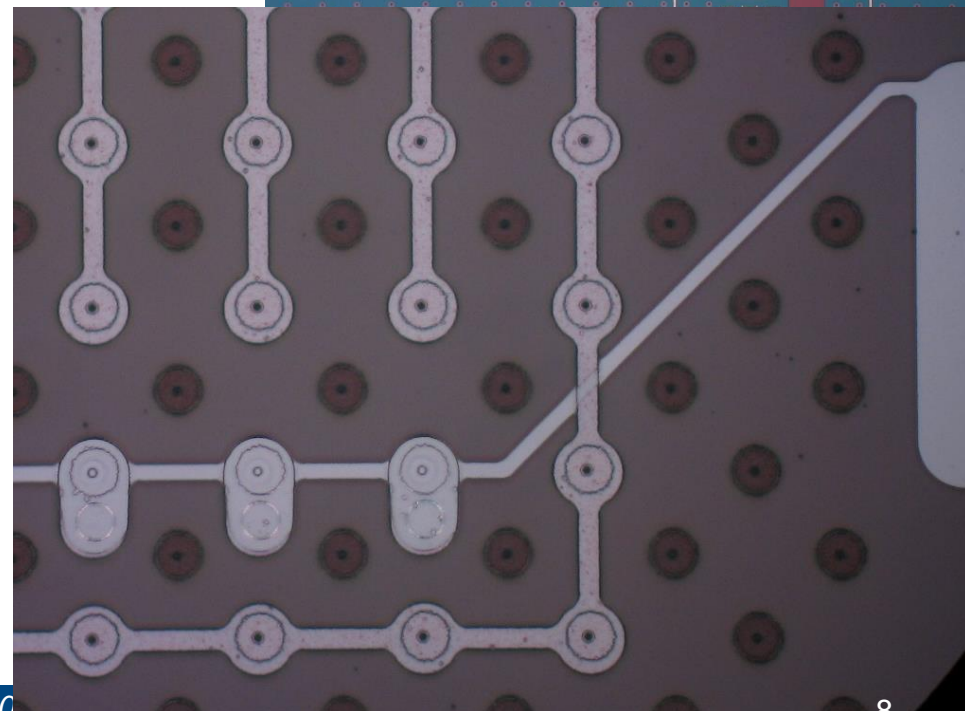
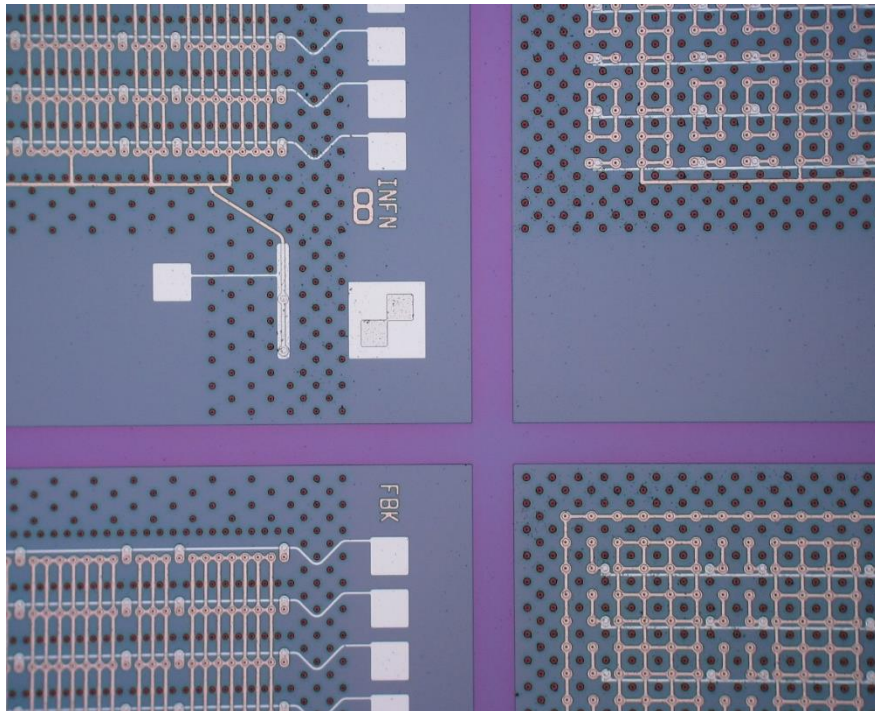
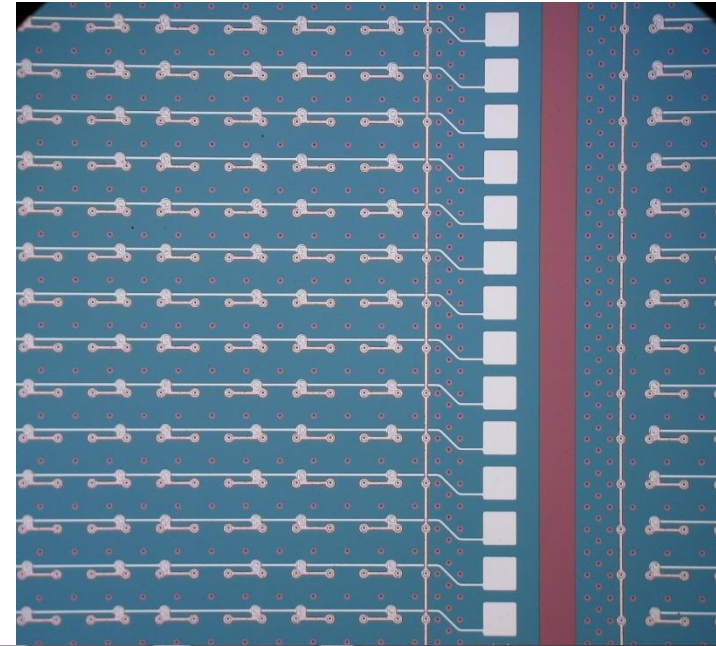
- **FE-I4**
  - 50 x 250 (2E) std
  - 50 x 50 (1E)
  - 25 x 100 (1E and 2E)
  - 25 x 500 (1E)
- **FE-I3**
  - 50 x 50 (1E)
  - 25 x 100 (1E and 2E)
- **PSI46dig**
  - 100 x 150 (2E and 3E) std
  - 50 x 50 (1E and 2E)
  - 50 x 100, 100 x 100 (2E + 4E)
  - 50 x 100, 100 X 150 (2E + 6E)
  - 25 x 100 (1E and 2E)
- **FCP**
  - 30 x 100 (1E)
- **RD53**
  - 50 x 50 (1E)
  - 25 x 100 (1E)
  - 25 x 100 (2E)

+ Test structures (strip, diodes, etc)



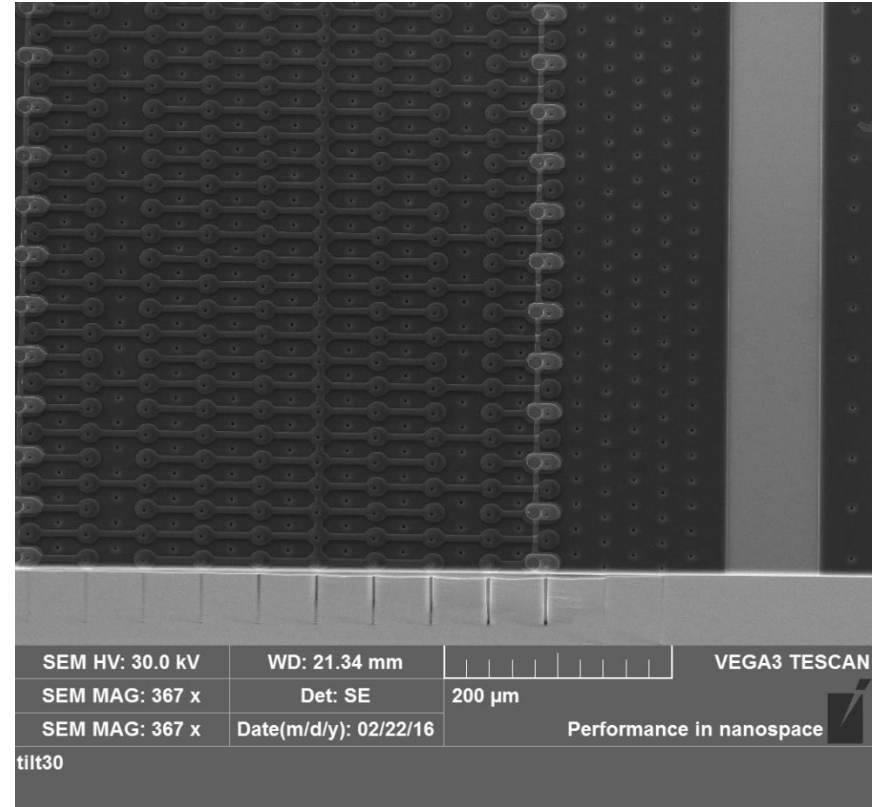
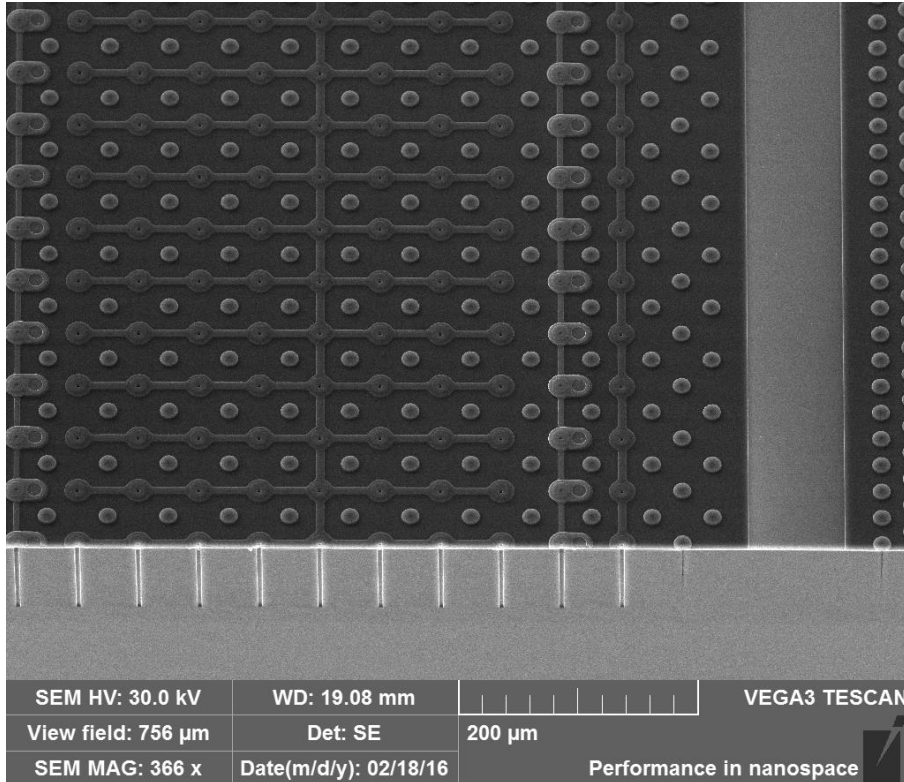
# A few pictures

- Wafers with temporary metal
- Good lithographical quality

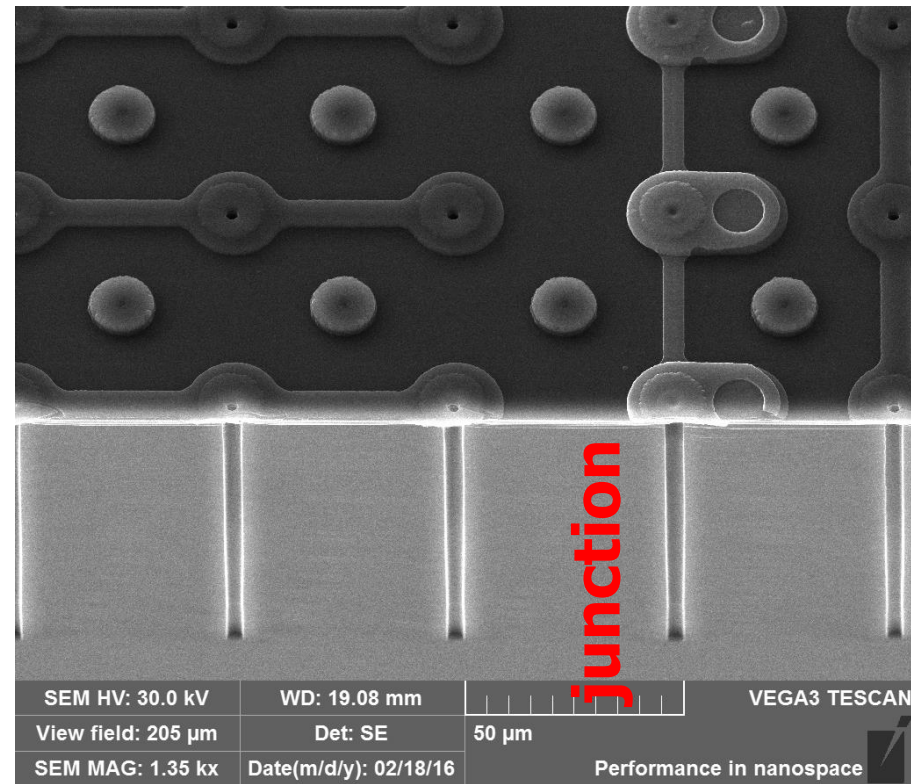
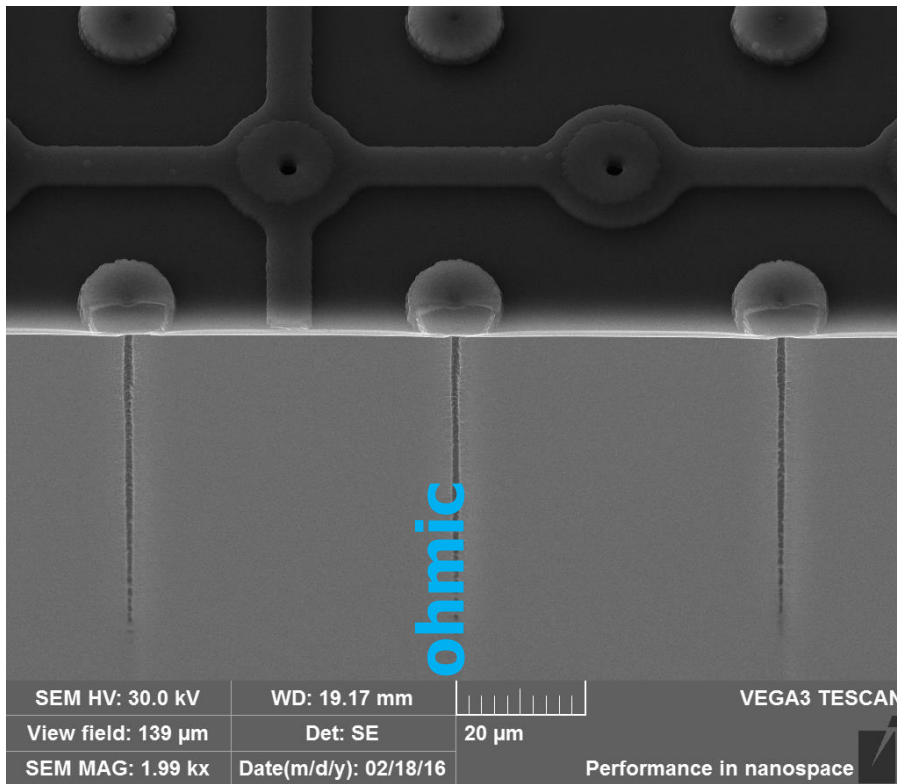




# SEM Pictures (1)

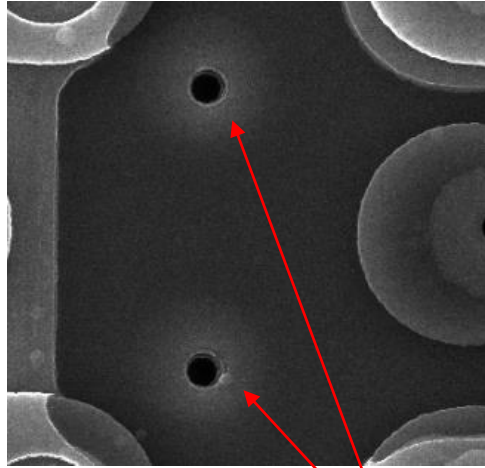


# SEM Pictures (2)

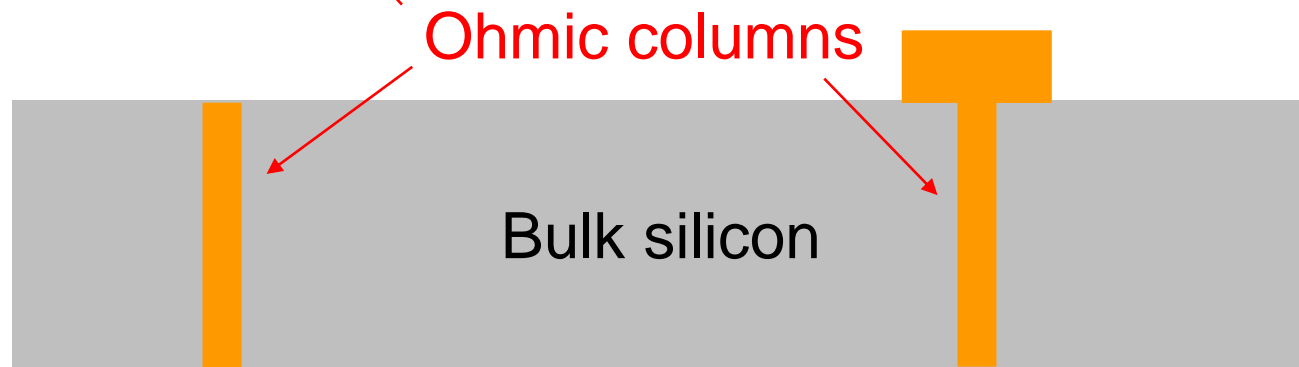
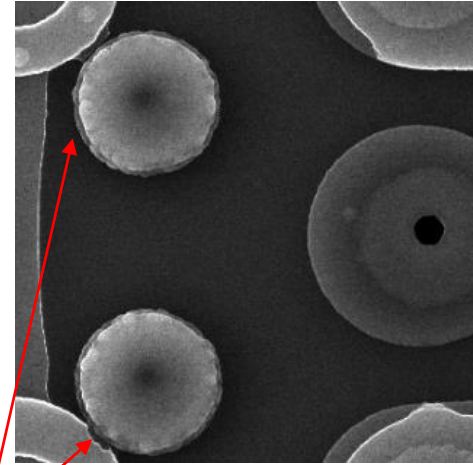


# Process details

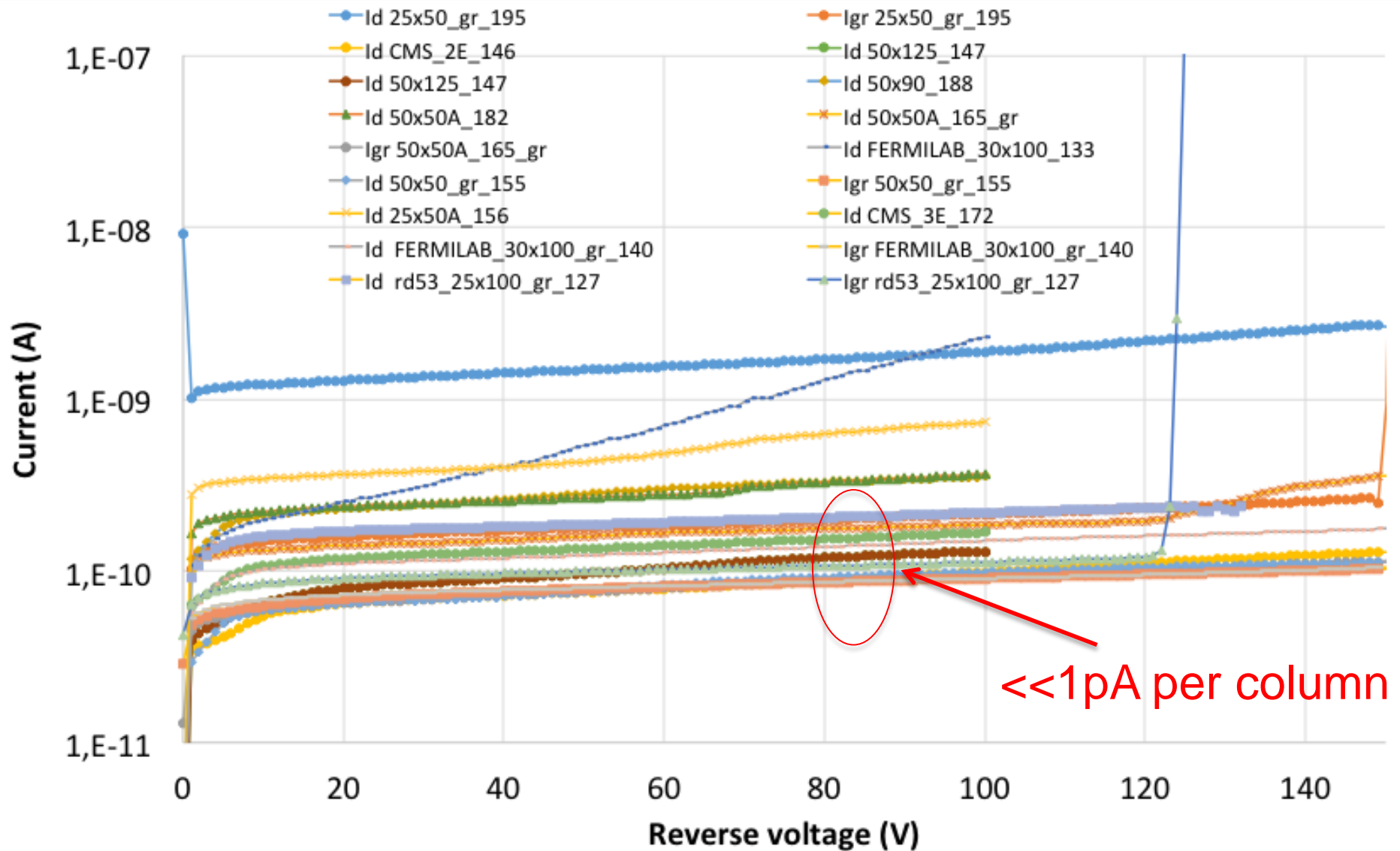
without poly cap



with poly cap

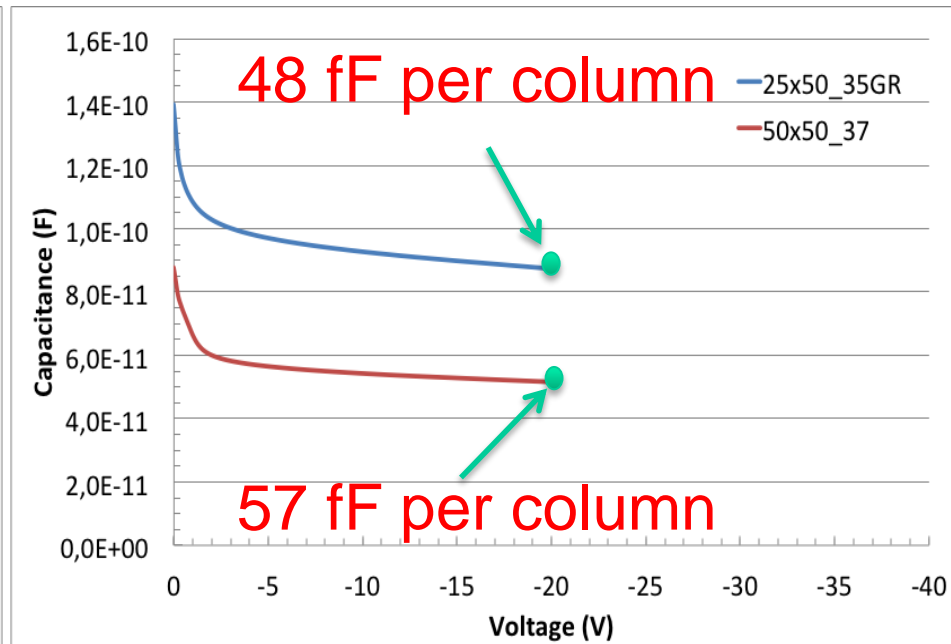
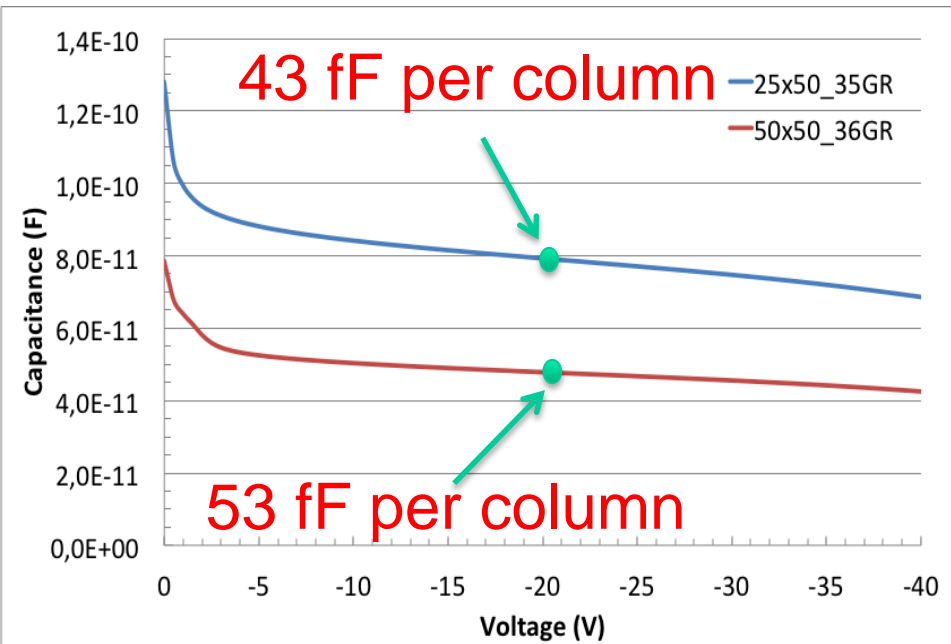


# W82 : 3D diode IV



# W48 diode CV

Device wafer thickness **100 um**      Device wafer thickness **130 um**

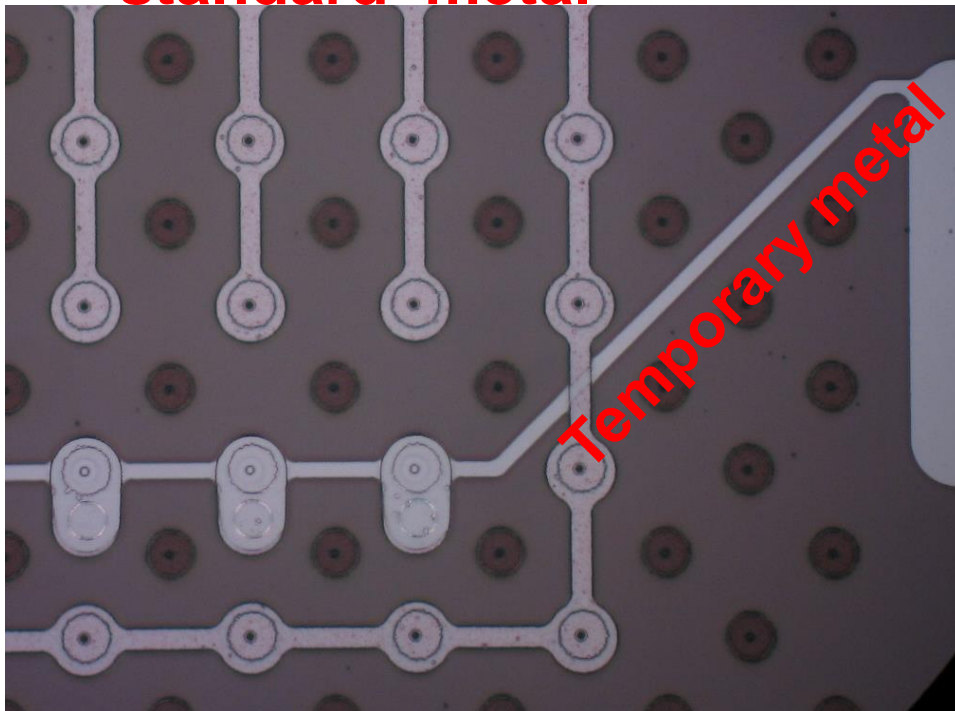




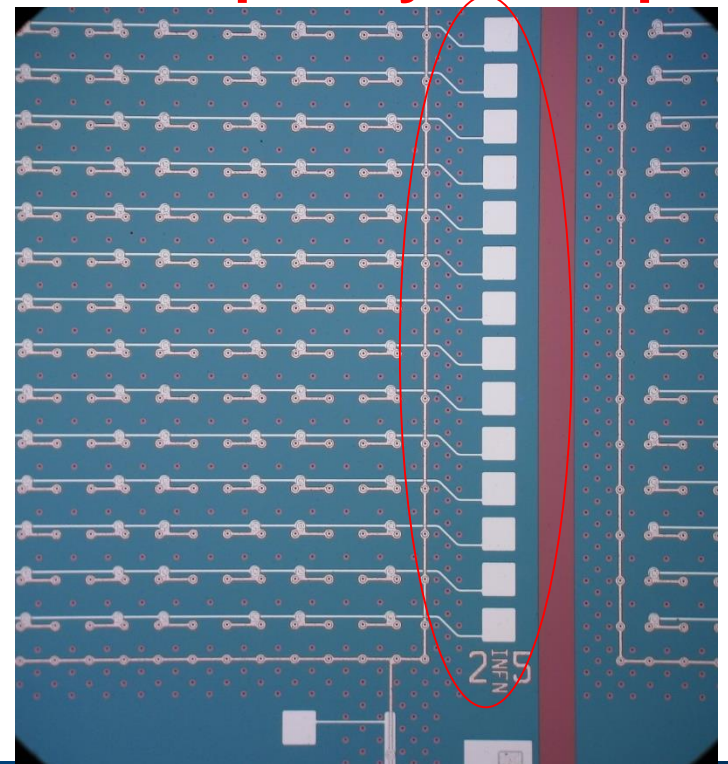
# TEMPORARY METAL

- The temporary metal shorts many pixels together in a strip
- The IV characteristics of all the strips that form a pixel sensor
- Allows to perform electrical tests on the pixel sensors before bump-bonding
- IBL production experience have shown a good correlation between wafers and module performance

«standard metal»



Temporary metal pads

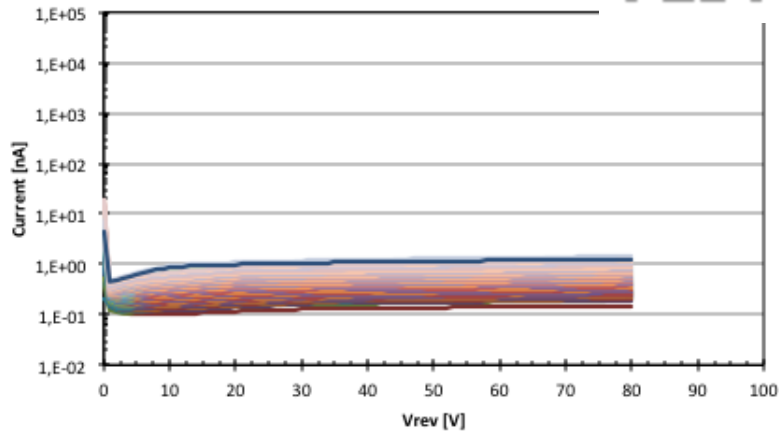




# Pixel sensors

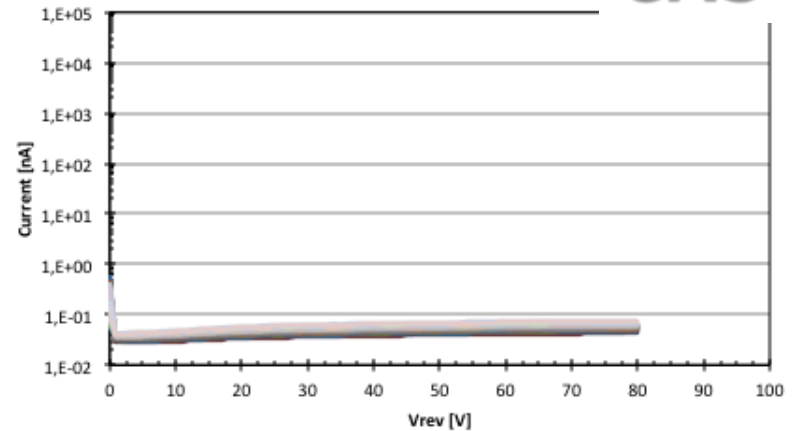
3DSS\_15 - W76

**FEI4**



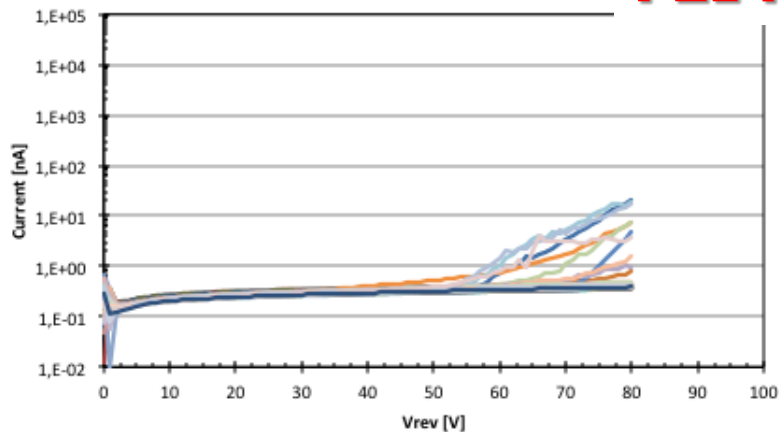
3DSS\_15 - W76

**CMS**



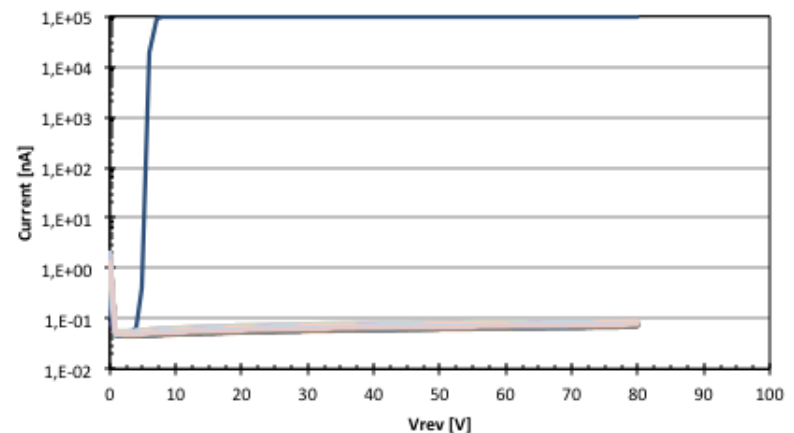
3DSS\_15 - W76

**FEI4**

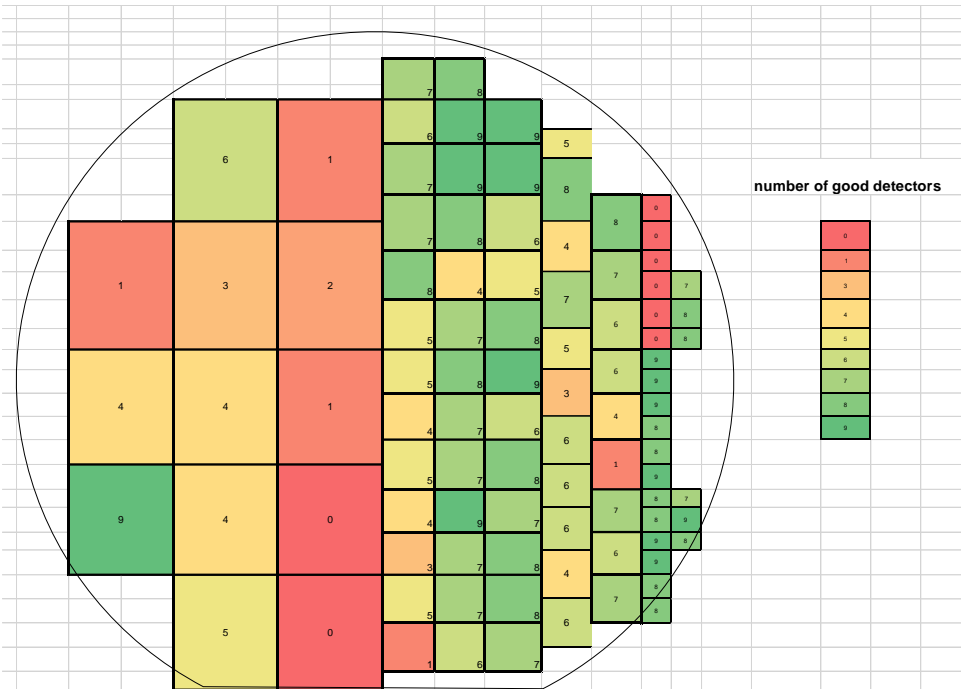


3DSS\_15 - W77

**CMS**



# Numbers of good detectors



- Yield it's related to area and to design
- A lot of CMS pixel it's OK
- Some FEI4 design have a good yield

it's too early to define a process yield

Now we are optimizing the fabrication process

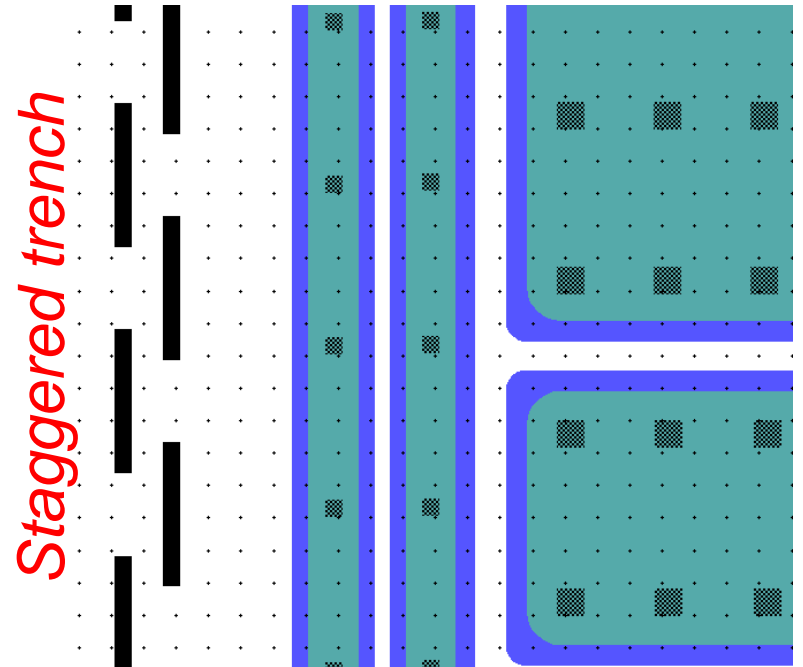
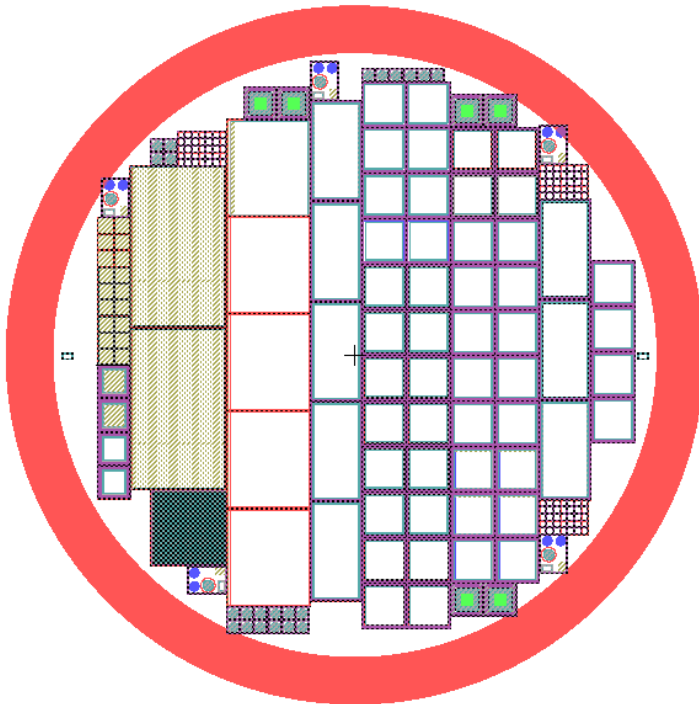
## Si 3D conclusions

- From initial electrical tests, good intrinsic sensor quality observed:
  - low depletion voltage
  - low leakage current
  - high breakdown voltage
- 25x100 pixel layout confirmed to be critical
- Automatic I-V curve highlighted the presence of defects, but there are a number of sensors usable for functional testing
- Wafers will be sent to IZM and to SELEX for bump bonding



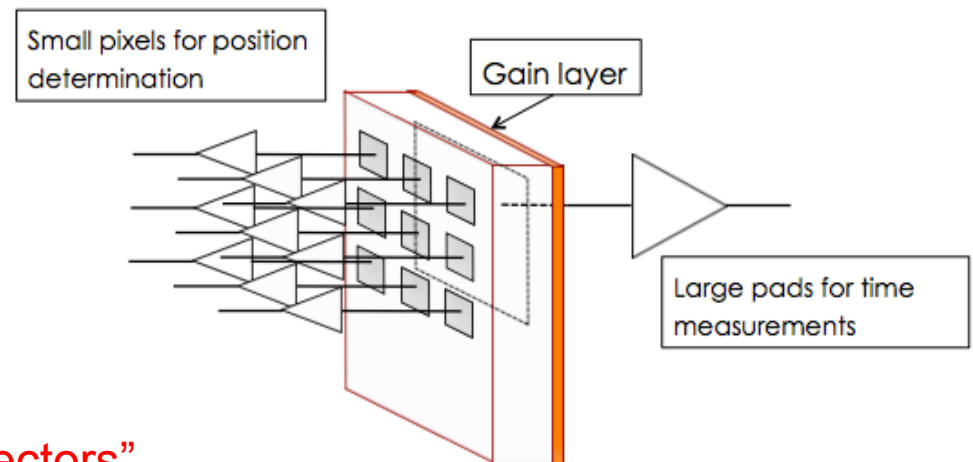
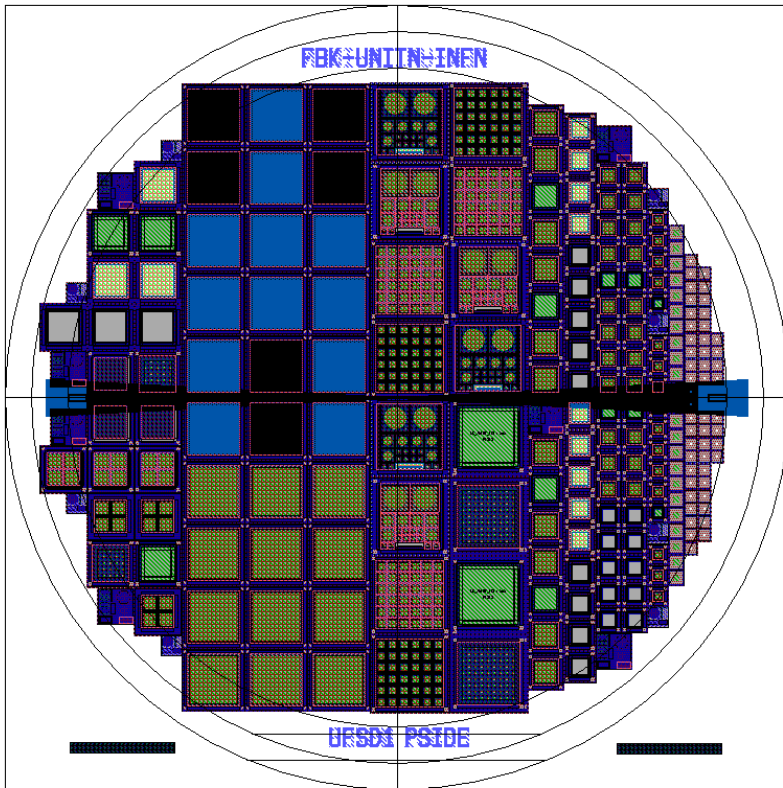
# Active Edge on thin substrate

- ATLAS & CMS pixels
- Si-Si & SOI
- n-on-p technology
- Design completed , ready to start with the fabrication



# Single & Double-Sided Pixelated LGAD

- In partnership with Torino/Trento
- Single and double sided devices on 300um silicon wafer
- First batch completed in March 2016
- In progress: definition of single side process on thin 50um Si-Si wafers



See Nicolò Cartiglia talks  
“Progress in the design of LGAD detectors”



*thanks for your attention*

# Fondazione Bruno Kessler



Consistent R&D investment by Local Government (2% of Province's GDP, Gross Domestic Product)

**Scientific and Technological Area**

**Humanities Area**

**CM  
M**  
Centre for Materials and Microsystem

**ICT**  
Centre for Information Technology

**ECT  
\***  
European Centre for Theoretical Physics

**CIR  
M**  
International Center for Mathematical Research

**ISIG**  
Centre for Italian-German Historical Studies

**ISR**  
Centre for Religious Sciences

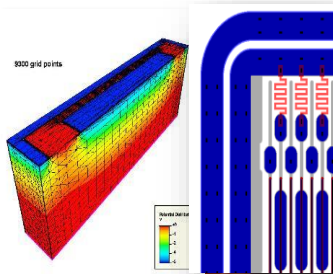
**IRV  
APP**  
Research Institute for the Evaluation of Public Policies

**CER  
PEG**  
Research Center on War, Peace and International Change

# Technologies & Competencies

## Full Custom Silicon Technology

## State-of-the art CMOS Technologies



Modeling-design



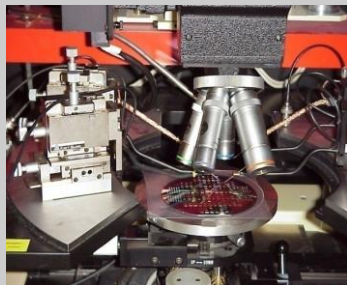
In-house  
production



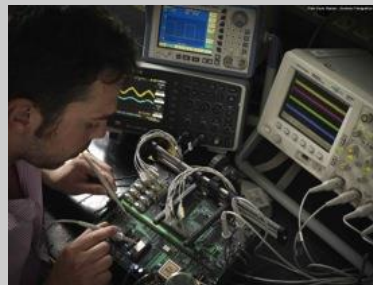
Analog and Digital  
IC Design

130nm-350nm  
external Fab

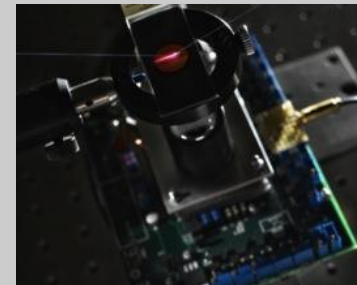
Parametric Testing



Functional Testing



Prototyping





## MICROFABRICATION AREA

*CMOS-like pilot line at 6" wafers with 2 CR for device fabrication:  
500mq, ISO 3-4 and 100 mq, ISO 4-5*

## TESTING AREA

*device parametric testing*

## INTEGRATION AREA

*packaging and microsystems assembly*

## MICRO-NANO ANALYSIS

*surface science analytical methodologies as SIMS, AUGER, AFM, SNMS ...*

# Technologies

## Silicon-based detector in full-custom technology

