TLU News

and

Common DAQ Interface Document

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10/06/2016

Common DAQ Interface Specification

- Need to define what is needed to participate in AIDA-2020 common beam-test
- WP5 deliverable (D5.1)

- Aims to be short – refers to external documents where possible.

- Draft for comments on AIDA-2020 WP5 pages: https://espace.cern.ch/AIDA2020-intranet/WP5/WP5%20Documents/AIDA-2020_D5-1_v0-1.pdf

- Needs to be submitted by end July
  - Comments & suggestions soon …….

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Hardware Interface

- Section on hardware interface
  - EUDET interface (asynchronous clocks)
    - Synchronize data using trigger numbers
  - AIDA interface (synchronous clocks)
    - Synchronize using timestamps and/or trigger number
    - clock , trigger , busy , sync
- Points to AIDA-TLU manual and EUDET TLU memo

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Software Interfaces

- Need to define interfaces for:

- Data storage
  - Have to be able to retrieve data with enough meta-data to correlate with other detectors

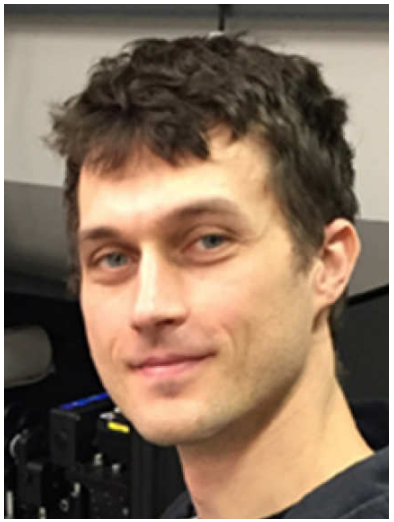
- Run Control
  - Define interface
    - Easy for EUDAQ based systems.
  - Define finite state machine for data producers
    - Have extra state INITIALIZED? (w.r.t. current EUDAQ)
    - Useful for Calorimeter and TPC
- On line monitoring (DQM)

TLU News

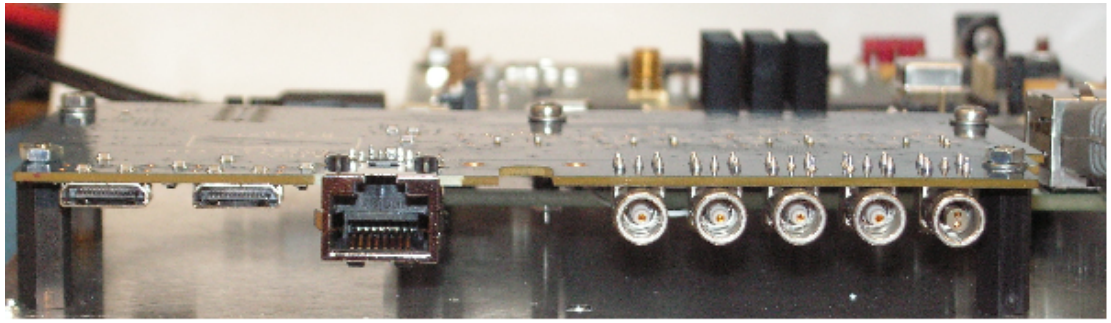
- New Physicist/Engineer started at Bristol 1/6
  - Paolo Baesso – DAQ expert.
  - 50% on AIDA-2020 for lifetime of project.
  - Currently learning PCB layout tools

- Schematic for next version of mini-TLU ready for review

- Porting firmware from Xilinx Spartan-6 to Artix-7 underway
  - Samer al-Kilani , UCL

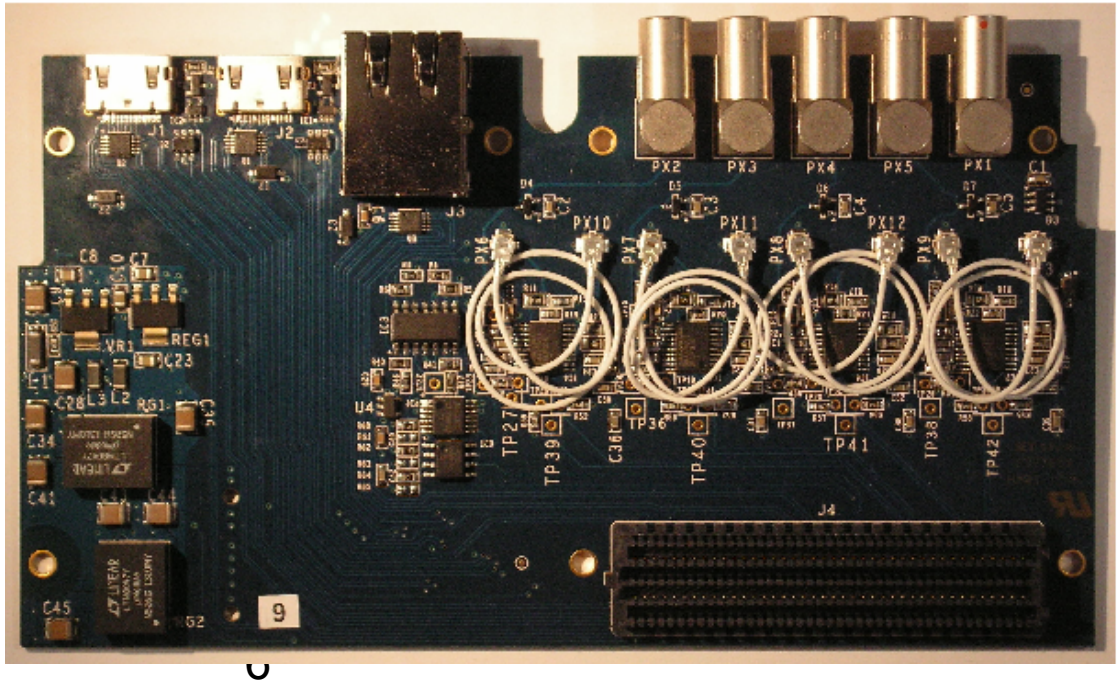


TLU Hardware Changes



DUT0 (HDMI) DUT1 (HDMI) DUT2 (RJ45) Trigger Inputs Clock I/O

← Current TLU



TLU Hardware Changes

- Moved to only threshold comparators
  - Current TLU has threshold and constant fraction discriminators (less time-walk)
  - Increased number of trigger inputs from 4 → 6
- (nobody was using the constant fraction discriminators, but were requests for more inputs).

- Added low jitter clock generator (si5345)
  - Allows TLUs to be chained together
    - Added HDMI connector that can receive clock
  - (Some beam-tests have used the TLU clock to drive TDCs. Not good - the clock coming out of the FPGA isn't low jitter)

TLU Hardware Changes

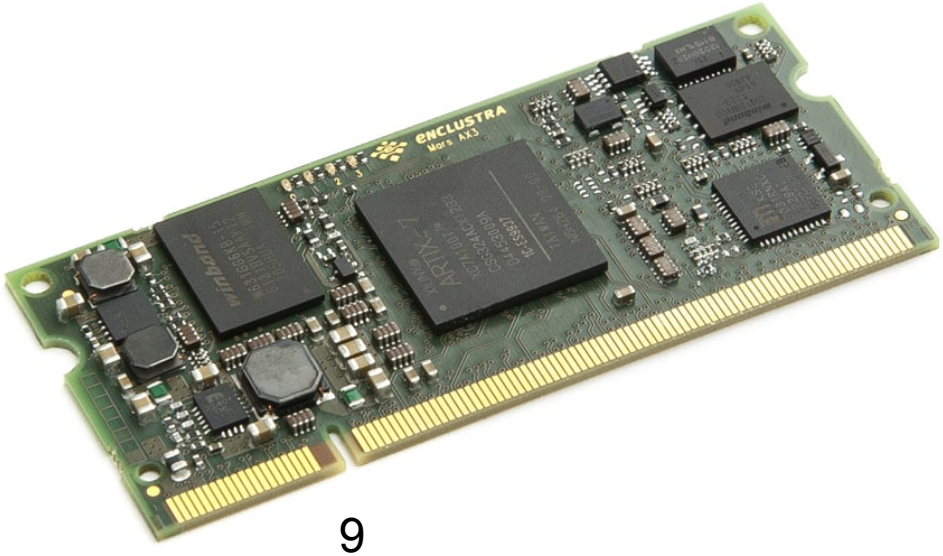
- Added external LVDS Rx/Tx chips
  - (instead of relying on FPGA I/O).
  - Should improve LVDS signal quality
    - (one beam-test reported that triggers were going missing between the TLU and the device under test. I think this was their problem, but can't be sure.)

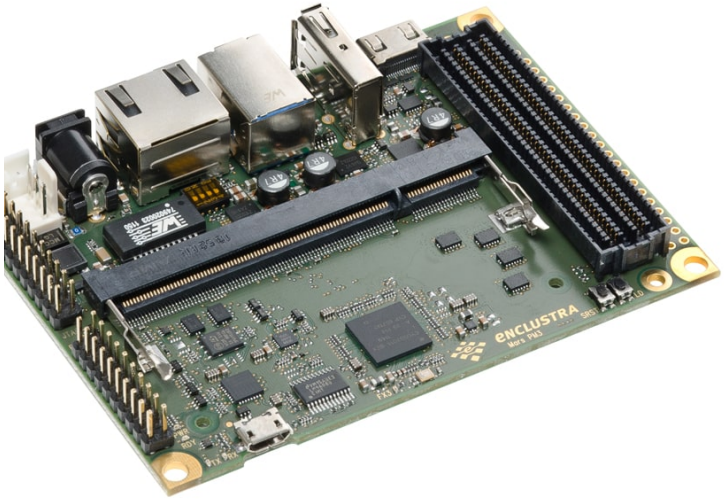
- Increased number of DUT connections from 3 → 4
  - One DUT connection can be used to receive clock.

- Start PCB layout after schematic review
  - … Volunteers welcome.
- Hope to send board design for manufacture before end July.

New FPGA Family

- TLU gets bigger
  - Not standard FMC size
  - Still uses FMC connector
  - Can use any FPGA carrier with LPC FMC connector
- Porting to Xilinx Artix-7 (currently Spartan-6)
  - Aiming for Enclustra MARS AX3 / PM3
  - IPBus already ported.





Summary

- Specification document will be published by the end of July
  - Not trivial since not all details are fixed.
- Contributions vital.

- Next version TLU in progress
  - Please let me know if you are able to take part in review of circuit schematics
  - PCB layout after review
  - Aiming to produce a small batch first placing order by end July