Simulation of RD53A architectures and power activity

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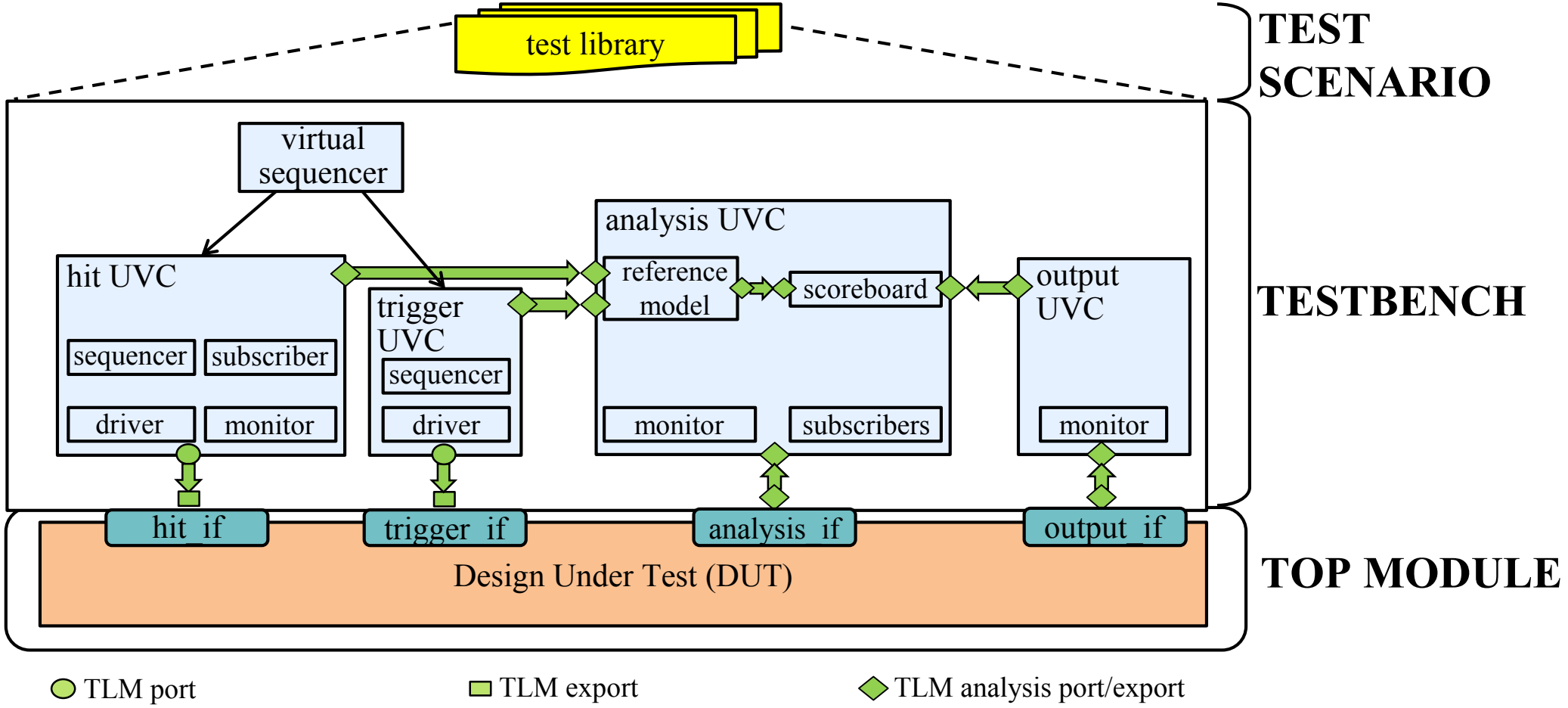
OUTLINE

- **Introduction**
- **RD53 simulation and verification framework** (VEPIX53)
  - Block diagram and interfaces
- **Digital architecture comparison**
  - Introduction
  - Summary of results
- **Power analysis for serial powering**
  - Digital power estimation
  - Power profiles
- **Conclusions and future work**



- **Flexible generation of input stimulus**
  - constrained-random (realistic/extreme cases), input from sensor/Monte Carlo simulations
- **Automated verification:**
  - statistics on performance, generation and classification of warnings/errors

Goal of digital architecture comparison

Determine digital architecture(s) that better meet(s) RD53A specifications

Different quantities under exam

- Inefficiency i.e. hit loss } ➔ simulation of **non-synthesized RTL** (within ***VEPIX53***)
- Occupation of area
- Power consumption

} ➔ comparison of **synthesized architectures**

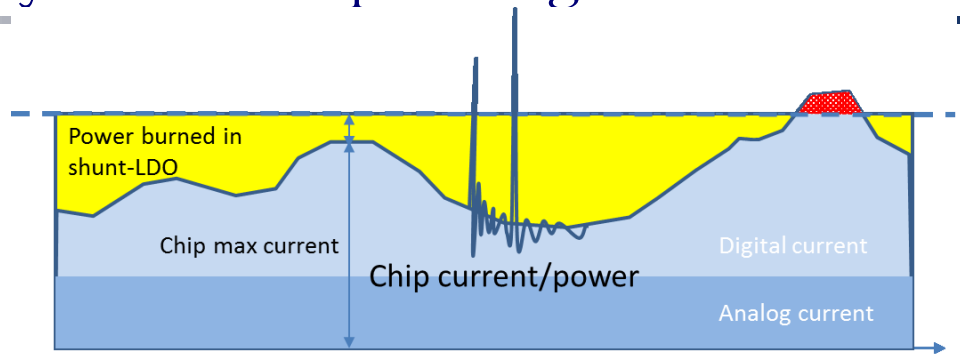
Architectures under exam

- ***Distributed* architecture** (2x2 pixel region)
- ***Centralized architecture*** *(4x4 pixel region)*
- *Same size of pixel array during comparison: 4x64 pixels*
  (= 1 double column for distributed architecture, 1 single column for centralized architecture)

Metrics	**4x4 centralized buffer architecture***		**2x2 distributed buffer architecture**	
Hit loss due to dead time (%)	Slow FE	Fast FE	Slow FE	Fast FE
	2.44	0.69	0.58 – 2.67	0.33 – 0.71
Hit loss due to buffer overflow (%)	14 locations: 0.46 15 locations: 0.16 16 locations: 0.06		7 locations: 0.57 – 0.81 9 locations: 0.04 – 0.07	
Hit charge info loss due to limited ToTs (%)	0.29** (6 ToTs max)		–	
Pixel region area*** *(digital, post synthesis, pre-P&R) (μm²/pixel)*	664 (14 loc.) **728** (16 loc.)	761 (14 loc.) **786** (16 loc.)	1039 (7 loc.) (***TBC***) 1165 (9 loc.) (***EST***)	*n.a.*
Power consumption *(average, post-P&R) (μW/pixel)*	*coming soon*		4.832 (typical) 6.203 (worst)	

* Centralized architecture features 5-bit ToT; ** to be repeated with MC edges of barrel data; *** No TMR in either architecture

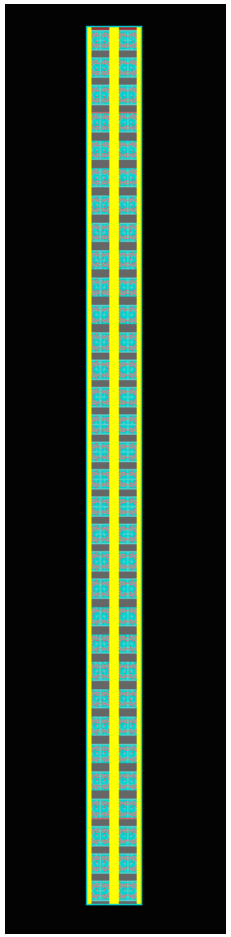
- ***RTL simulations***: in the current implementation distributed architecture preferrable in terms of dead time (for a generic analog FE) and no limit in ToT storage
- ***Area***: centralized architecture shows on the other hand much lower area thanks to data reduction
- ***Power***: more detailed characterization will be performed (design of 4x4 architecture not finalized)



- **Serial powering issues:**
  - constant (maximum) current is provided from the powering system
    - the **shunt-LDO will burn "surplus" current** to keep the serial power current constant
  - **need** to know **maximum current/power visible to the powering system**
  - **low-pass filtering** from the chip to the serial power network (on-chip decoupling, shunt-LDO decoupling, module decoupling, …)
  - → **Power variations** are **averaged over a time window** (comparable with **decoupling time constant**)
- **Detailed chip power analysis is performed**
  - **average** (over long simulation, with realistic operation)
  - **peaks** (look **power evolution over time**, i.e. **power profile**):
    - **short time constant** (~ps-25ns): should be filtered by on-chip decoupling
    - **longer time constant (~1us):** power averaged over such time window seen at the powering system level

Digital power analysis

- 4x64 pixel array simulated (from FE65P2), **no periphery**
- power averaged over **100µs**
- **delay corners** considered (temperature variations not actually in the .lib; typ 25°C, worst 0°C)
  - **RD53A typ**:
    - **RC corner**: **RC typ** (qrcTechFile)
    - **library set**: tcbn65lptc_ecsm (**typ**)
    - **library operating condition** (process: 1 , **voltage: 1.2 V**)
  - **Worst** (powerwise):
    - **RC corner**: RC best (qrcTechFile)
    - **library set**: tcbn65lplt_ecsm (**fast**)
    - **library operating condition** (process: 1 , **voltage: 1.32 V)**
    - **with** extracted **parasitics** (***.spef*** files)
- **activity conditions** → use of VEPIX53 to provoke chip activity
  - with **hits** (3 GHz/cm^2 hit rate) **and triggers** (1 MHz trigger rate)
  - without hits and trigger (**only clock** sent to the logic)
  - with **hits** (3 GHz/cm^2 hit rate) and **no trigger**
  - with **triggers** (1 MHz trigger rate) but **no hit**

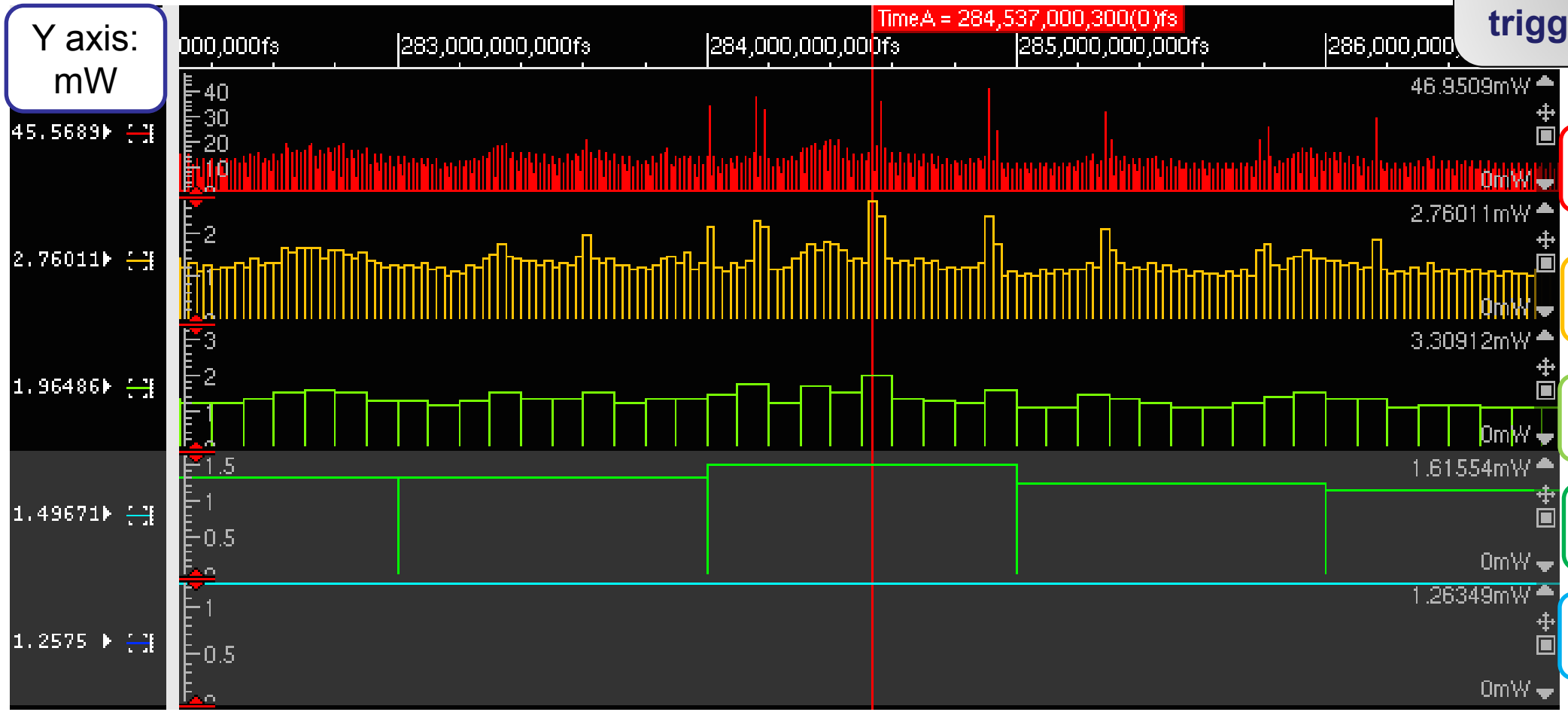


Understand the **impact of different activity conditions** on digital power consumption

Power profiling example

- **Time resolution: 1ns, 25ns, 100ns, 1 µs, 10 µs** (zoom on shorter simulation window)
- delay corner considered: RD53A typ
- **main power variations** are **handled by decoupling**

Activity: hits (3GHz/cm2) and triggers (1MHz)



CONCLUSIONS and FUTURE WORK

- **RD53A architecture**

  Developed simulation and verification framework **VEPIX53 successfully used to simulate different architectures** (and prototypes)

  – main results available

  – design progress will show which one/s will be implemented

  – VEPIX53 will be used for design simulation and verification

- **Power estimation**

  – criticality of **serial powering**: **dynamic power analysis** to understand variations

  – **power profiles** of digital logic being used **as input to detailed simulation of shunt-LDO (powering circuit)** and decoupling
    - results are **promising**

  – **design optimization** is also being focused on **finding best compromize between low and constant power consumption** based on such analysis