CPPM activities towards HV/HR CMOS in LF

Marlon Barbero – AMU / CPPM

AIDA-2020 first annual meeting, June 15th 2016

CPPM activities in WP6

- Participate to design of HV/HR CMOS sensor in LF technology, in particular by TCAD simulations, studying and optimizing vs:
  - Input capacitance.
  - Breakdown voltage.
  - Depletion voltage vs. bias / resistivity
  - Transient charge collection behavior.

In presence of NIEL + TID!

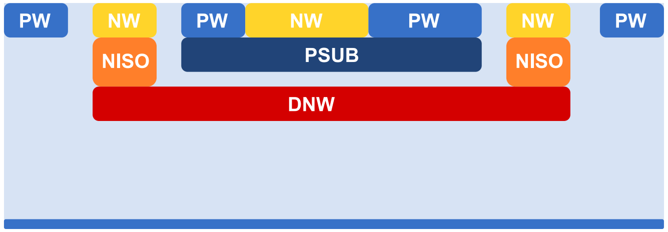
- Characterization in lab, under radiation…
- Design!
  - → CCPD LF Demonstrator submission in February.
  - → On-going: Monopix design, submission target date end June.
- First tries towards assessing potential physics performance of technology at small radius.
- 2-day simulation workshop in CPPM https://indico.cern.ch/event/497449/

Background

- Team: Bonn/CPPM pursue long standing collaboration → HV/HR-CMOS LF since ~2014. IRFU has joined forces more recently on this topic (2015).
- **LFOUNDRY technology & projects**

LFoundry CMOS3E technology:

- 150nm CMOS (Avezzano, Italy)
- 2kΩcm p-type bulk
- Deep NWell available in real triple-well process
- HV process
- Thinning and back size metallization possible
- MLM3 (25.840mm x 9.505mm)



LFoundry Projects

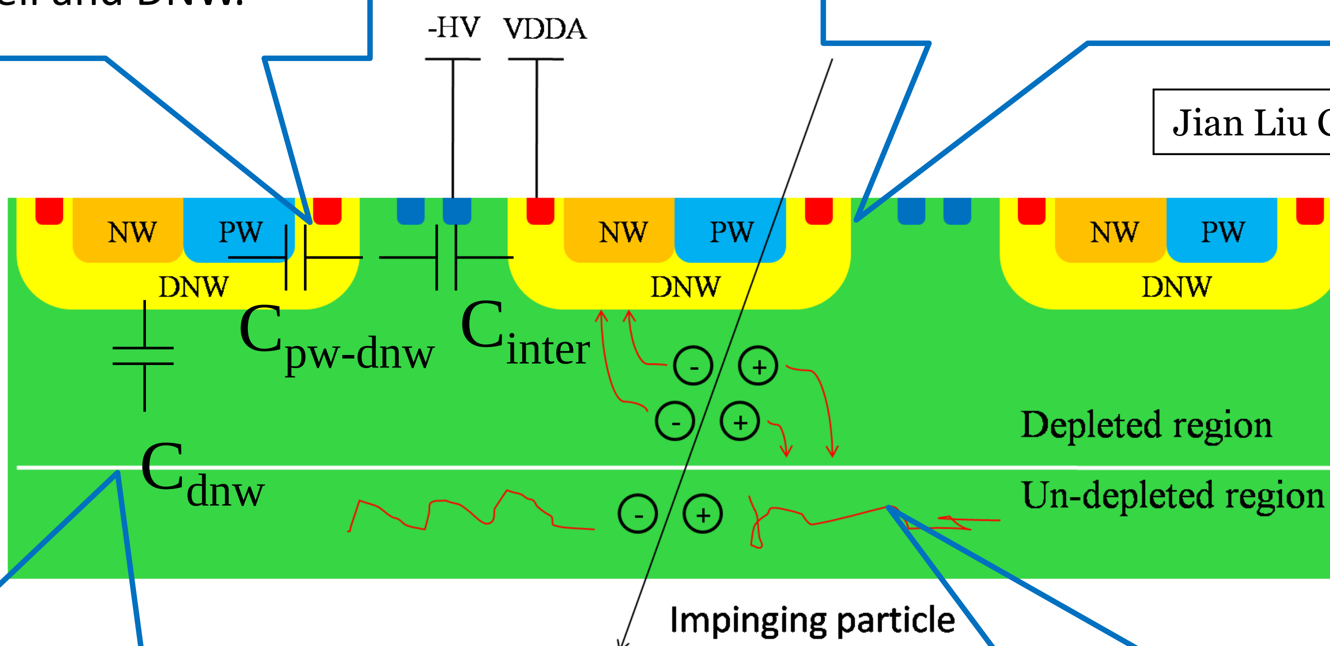
- CCPD-LF VA chip : 5 x 5 mm² (Bonn, CPPM,KIT) submitted july 2015
- CCPD-LF VB chip : 5 x 5 mm² (Bonn, CPPM,KIT) submitted july 2015
- LFCPIX VA chip : 10 x 10 mm² (Bonn, CPPM, IRFU) submitted Feb 2016
- LFCPIX VB chip : 10 x 10 mm² (Bonn, CPPM, IRFU) submitted Feb 2016
- LF_MONOPIX_01 chip : 10 x 10 mm² (Bonn, CPPM, IRFU) submission summer 2016
- COOL 1 chip : 12 x 10 mm² (SLAC, UCSC, KIT) submission summer 2016

What has been done using TCAD

AC: Input capacitance from the Pwell and DNW.

DC: Breakdown voltage in the critical region.

Jian Liu CPPM/ SDU

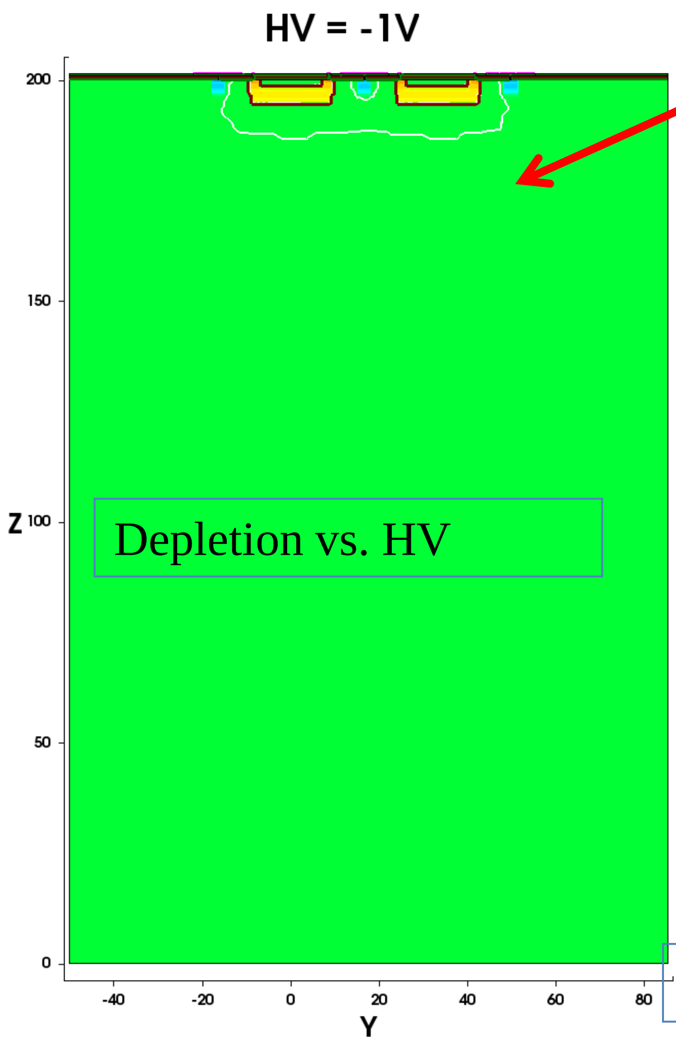


DC: Depletion evaluation depending on the biasing voltage and the resistivity.

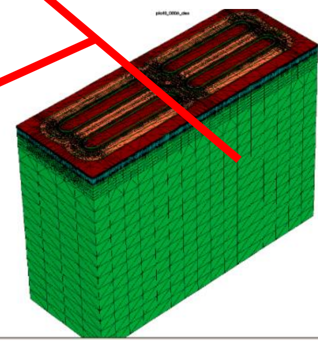
DC: Leakage current.

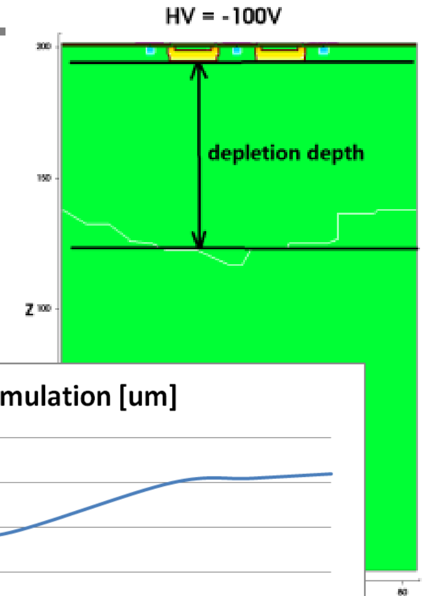
Transient: Charge collection behavior.

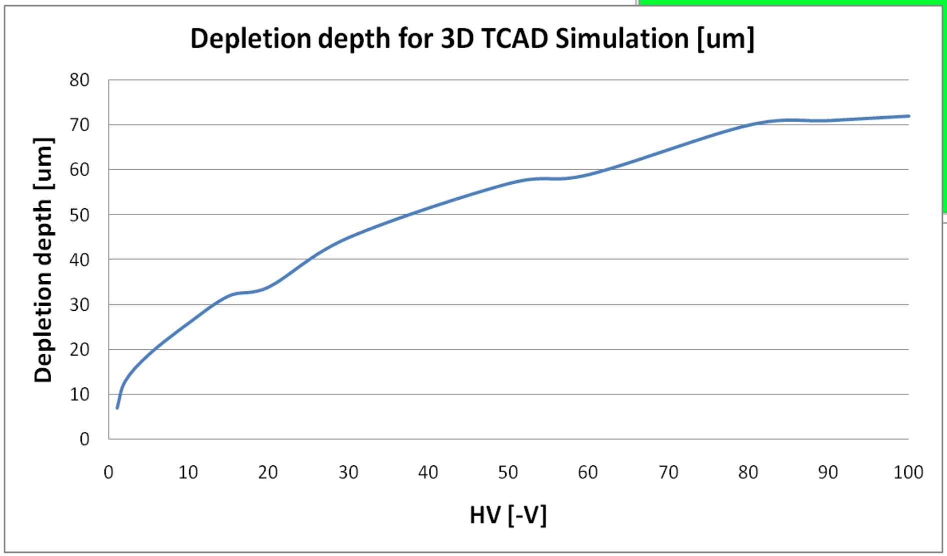
LF VerA depletion



Depletion vs. HV

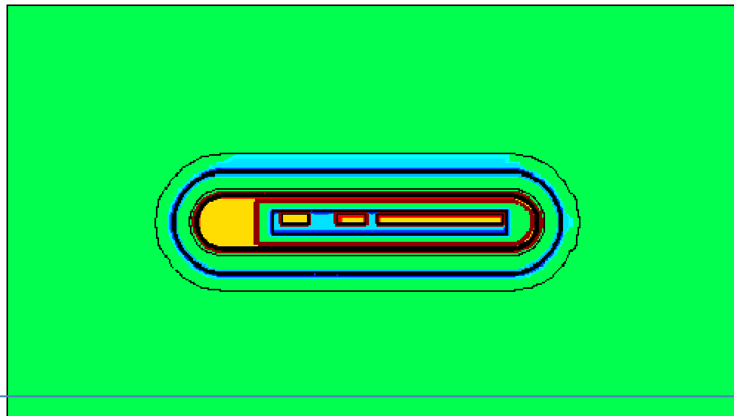




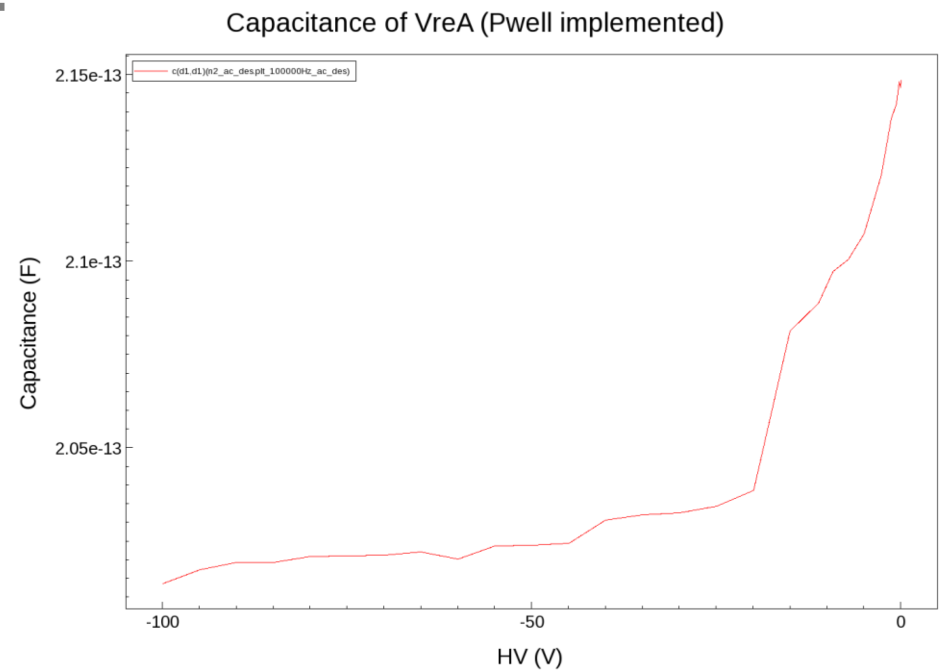


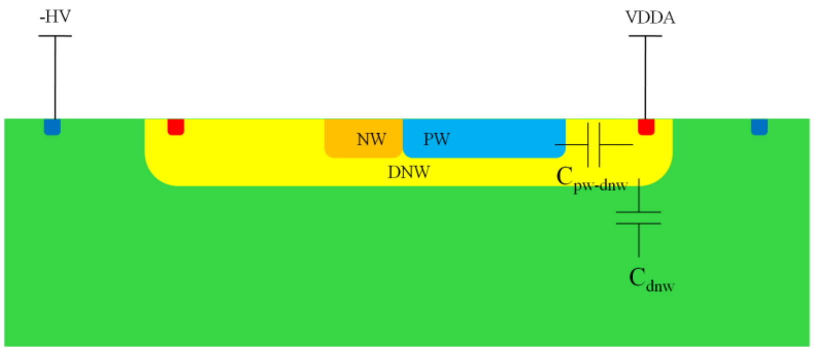
~70 µm of depletion depth can be obtained @HV=-100 V

LF VerA capacitance



Top view (PW and NW implemented)

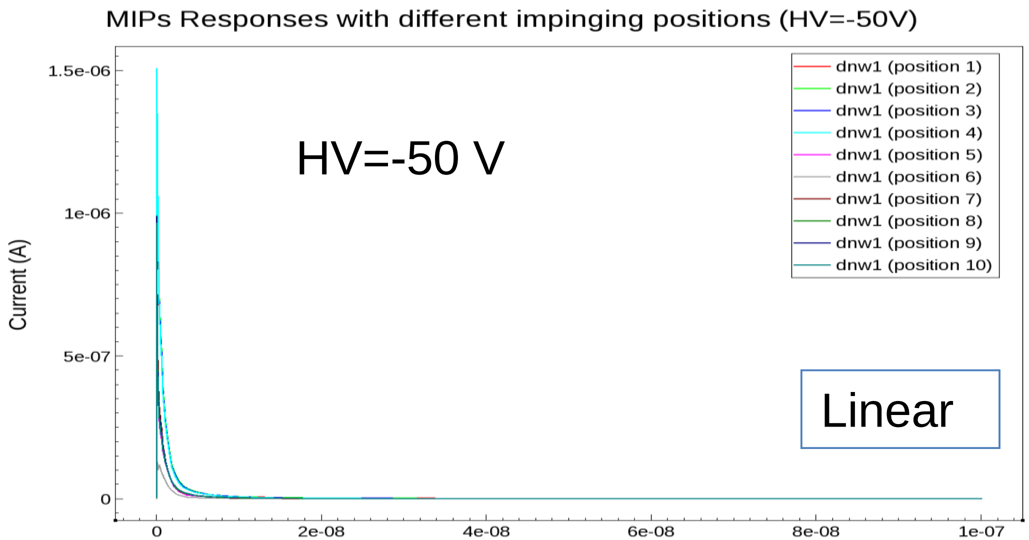


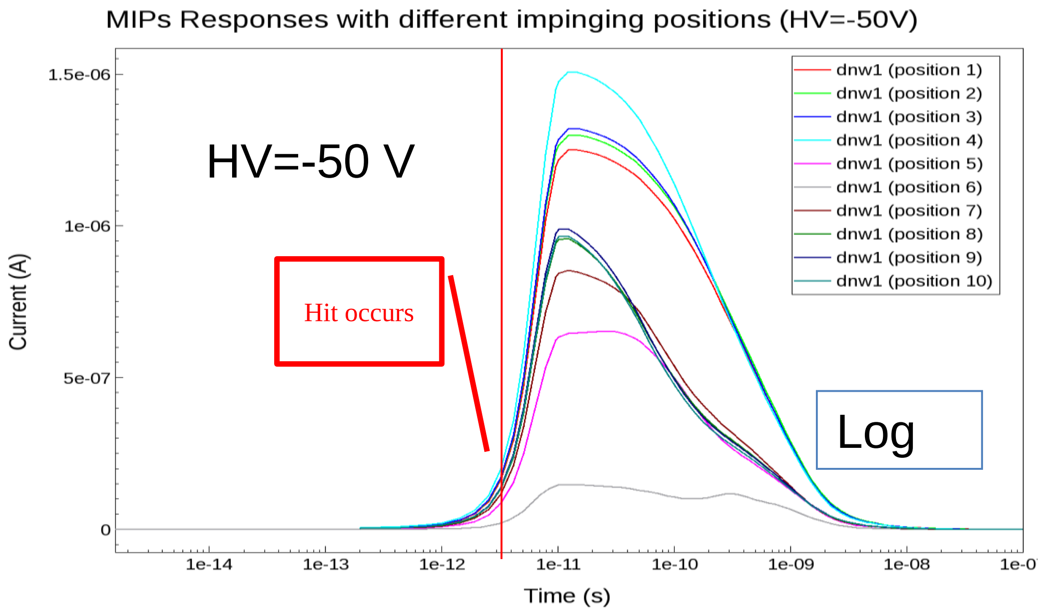


C_{dnw} is ~50 fF @ HV=-50 V
$C_{pw\text{-}dnw}$ is ~150 fF @ HV=-50 V
Total capacitance is ~200 fF @ HV=-50 V

The capacitances mainly come from the C_{dnw} (between the DNW and the substrate) and the $C_{pw\text{-}dnw}$ (between the PW/PSUB and the DNW)

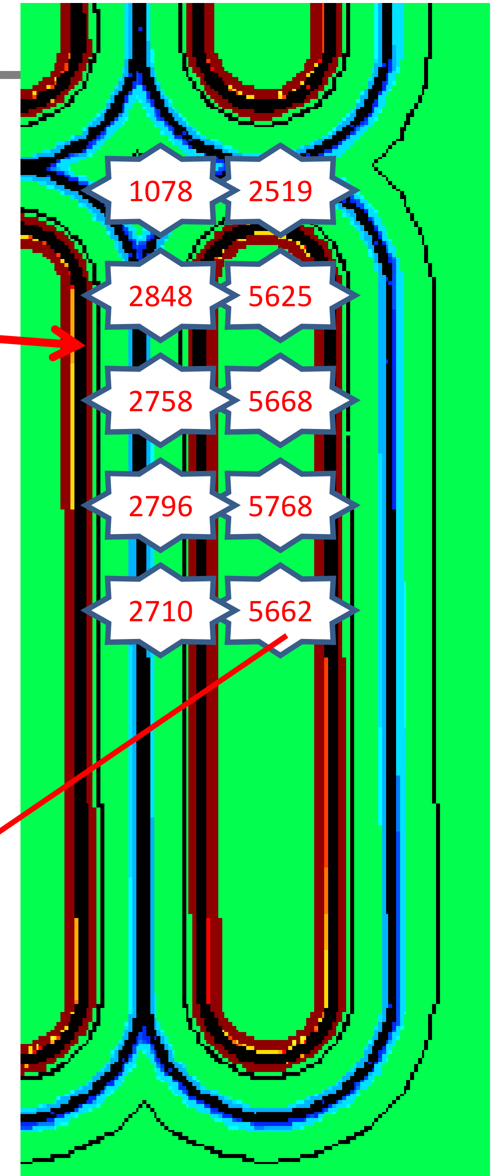
LFvA transient charge collection



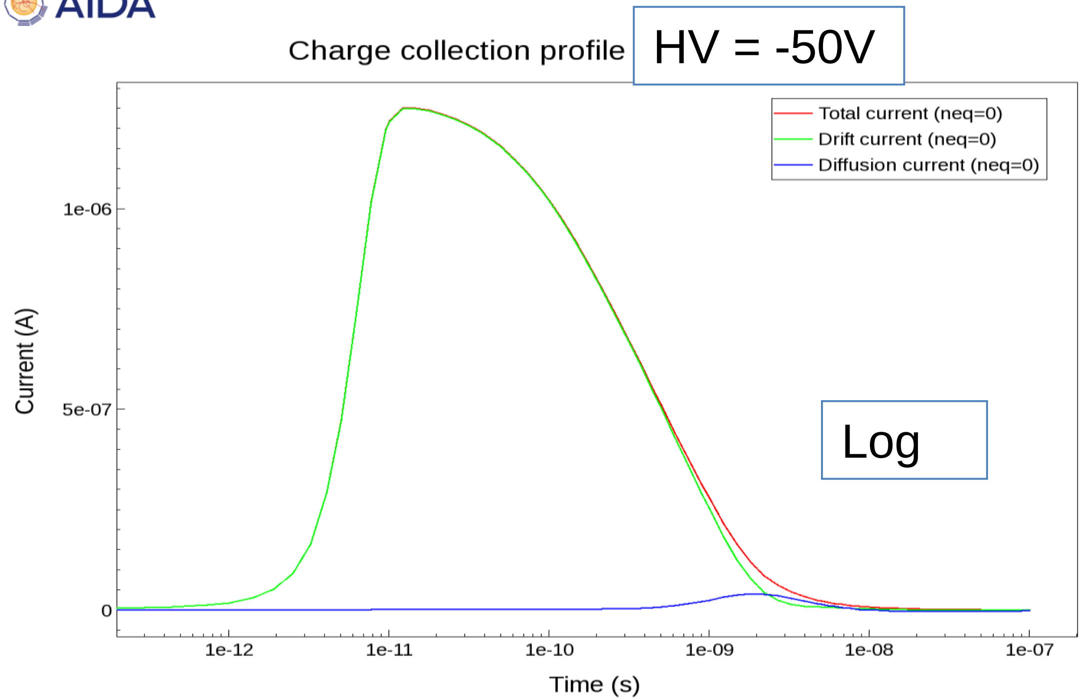


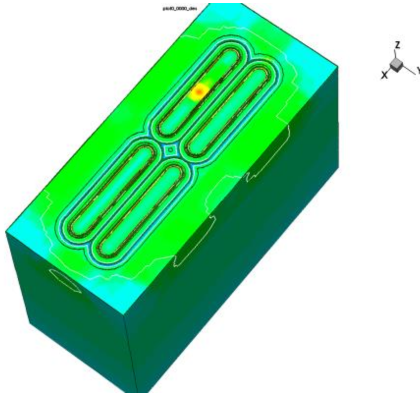
Collected charges within 5 ns.

6687 e- (HV=-100 V)



LFvA transient charge profile





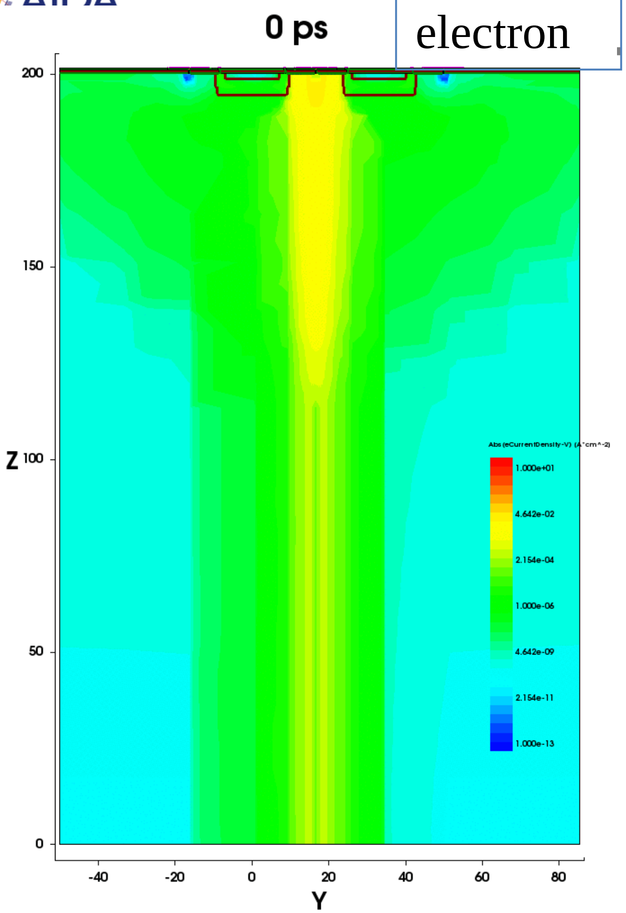
Fluence (neq.cm^{-2})	Drift(e-) @ -50V	Diffusion(e-) @ -50V
0	4812	850
1e14	4507	491
1e15	2536	188
1e16	1081	0

Enable the excess carrier generation in specific regions: depleted and un-depleted.

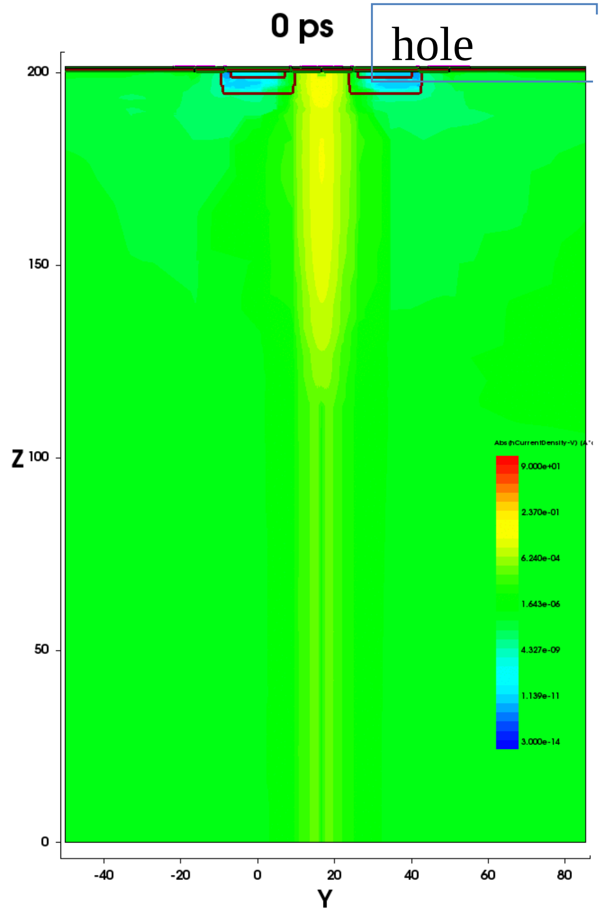
Before irradiation:
Q_{drift}=4812 e- (85%) peaking at ~100 ps.

$Q_{diffusion}$=850 e- (15%) peaking at ~2 ns.

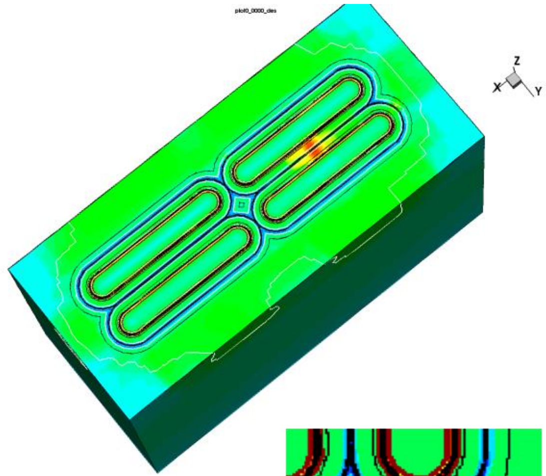
LFvA e/h current density (pos10)

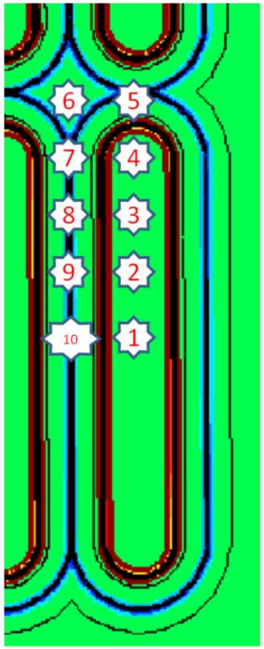


electron



hole





HV = -50 V

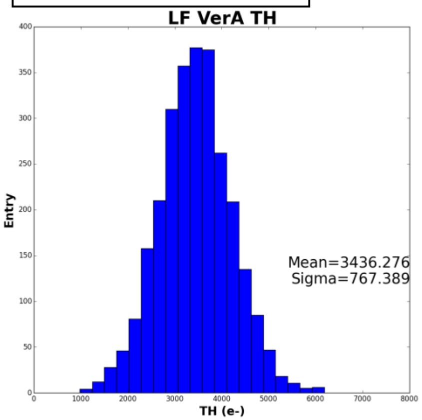
Electrons in depletion region drift towards DNW.

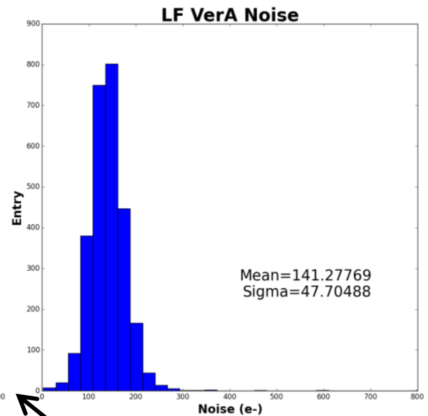
Holes in the upper side of depletion region drift towards p+.
Holes in the lower side of depletion region are swept out towards bottom.

LF VA/VB 2015 version

J. Liu / CPPM

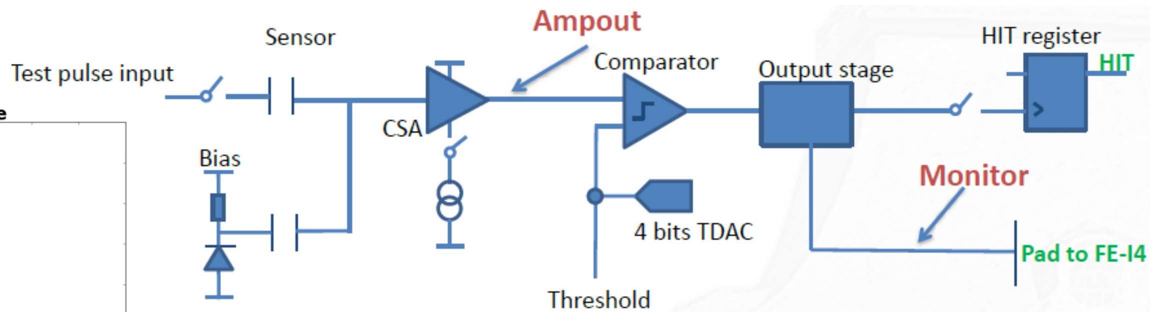
Pixel VA/VB





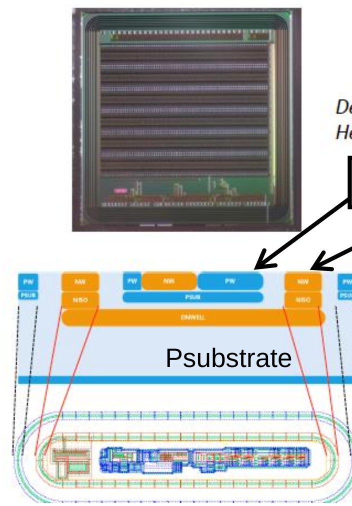
Threshold and noise LF VA after 100 MRads proton

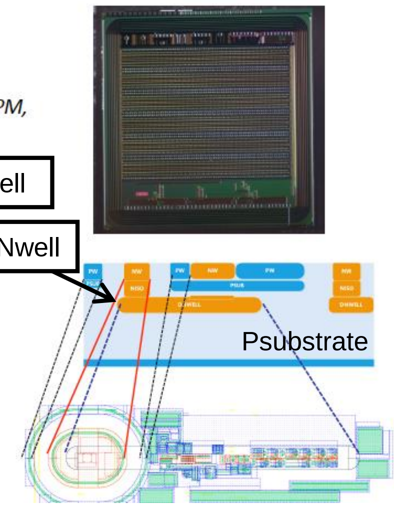
Pixel electrical parameter not much affected by 100 MRads irradiation



- CCPD LF VA
  - CMOS inside collection electrode
  - Test structures: NMOS and PMOS transistors
- CCPD LF VB
  - Smaller collection electrode
  - Test structure: diodes

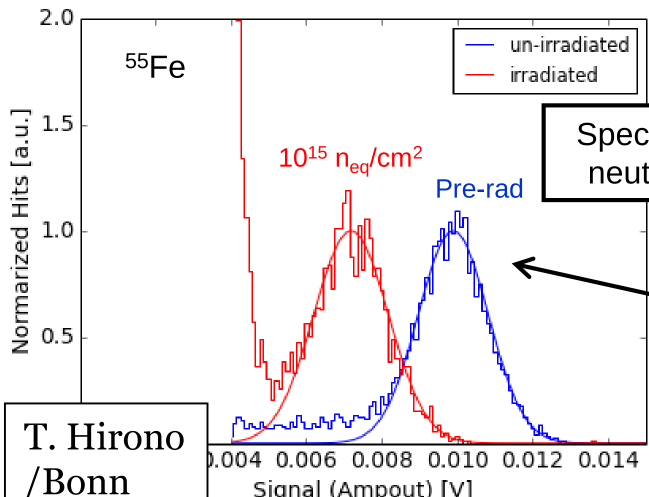
Design: Bonn, CPPM, Heidelberg





Blue= Pwell

Orange= Nwell



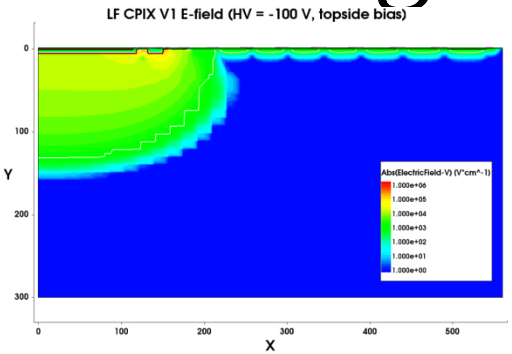
Spectrum ^{55}Fe after neutron irradiation

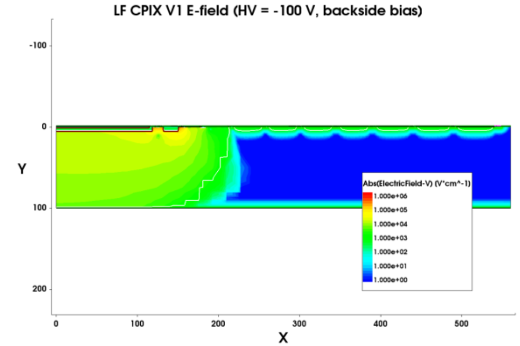
Electronics & sensor work after 10^{15} $n_{eq}.cm^{-2}$

T. Hirono /Bonn

Guard-ring for LF CPIX demo

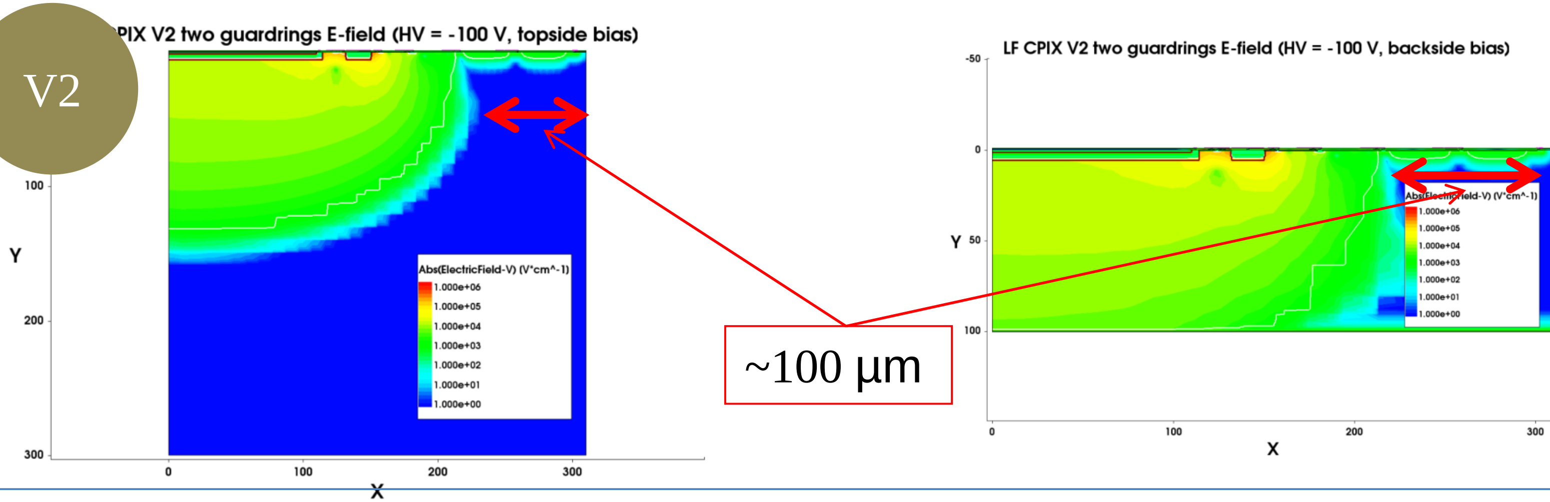
V1





Big un-depleted area between depleted edge and cutting edge → guard-ring reducing is possible → reduced dead region.

V2



Pwellring + 2 floating guard-rings + backbias + seal-ring.
The depleted region can not reach the chip edge even with removed 5 outer guard-rings.

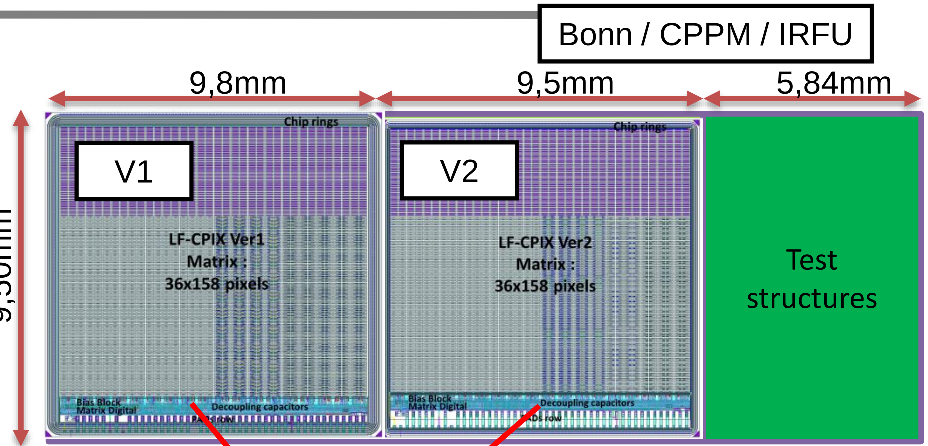
10×10 mm² demonstrator

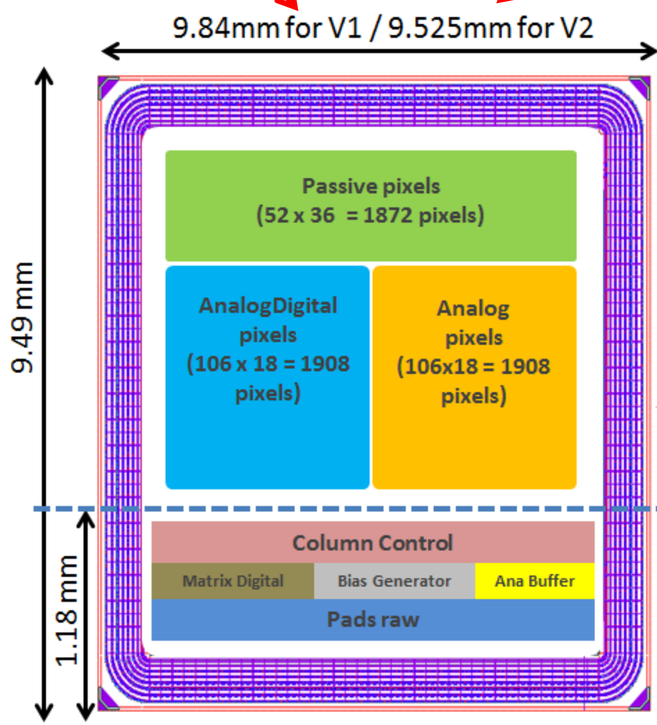
- Feb. 2016: MLM3.
- V2: V1 + new guard ring strategy.

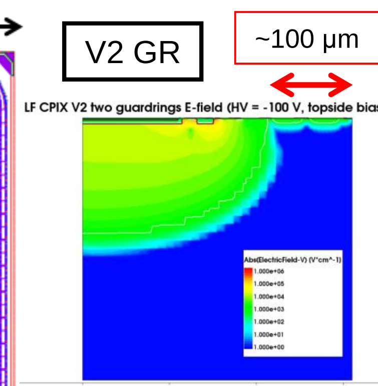
Bottom matrix: Col. ctrl, bias gene., analog buff., glob. config./SR readout

<u>Pixel Matrix :</u>

- Pixel 250µm×50µm (FEI4-like)
- All pixels have bond pad to FEI4
- <u>3 sub-matrices</u> :
  - **Passive**: only DNwell sense diode
  - **AnalogDigital**: à la LF VA, 4 flavors (different diode bias, diff. input transistors NMOS and PMOS).
  - **Analog**: preamp with complementary input CMOS, and 8 flavors (diode polarization, outputs “linear”, “saturated” or “digital”…).
  - Preamp out / hitOR available for all pix







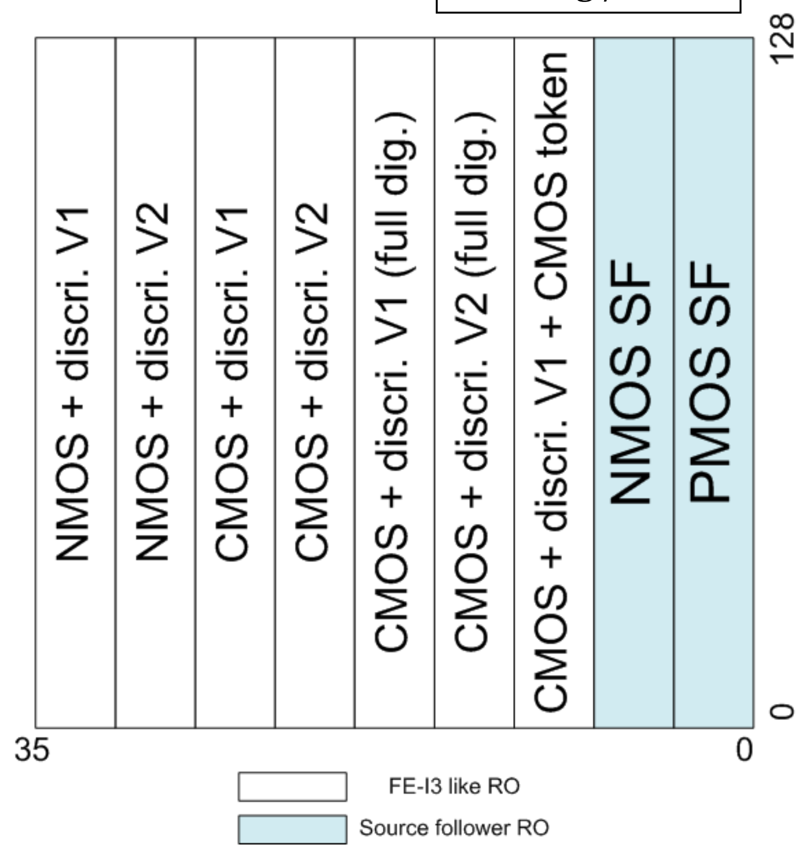
Jian Liu (CPPM/Shandong)

Expected ~ 2016 Q4

On-going: monolithic LF design

- Monopix design: Bonn/CPPM/IRFU
- 9 different flavors
  - Each has 4 columns
- 2 RO architectures
  - **FE-I3 like** pixels
    - NMOS/CMOS pre-amp.
    - Old/new discri.
    - Different power domain for discri.
    - CS /CMOS token transmission
  - **Pixel without RO logic**
    (logic at end of colum)
- Expected submission date: end June

T. Wang / Bonn



Performances using HV-CMOS

- Changes brought to Geant4-based simulation of current ATLAS pixel geometry.
- As a first try, to get faster results, no fundamental change to current 3+1 pixel layer geometry.
- HVCMOS could be exploited for outer layers, but we advocate here their use for the inner layer (current IBL) where they can have large impact on physics.

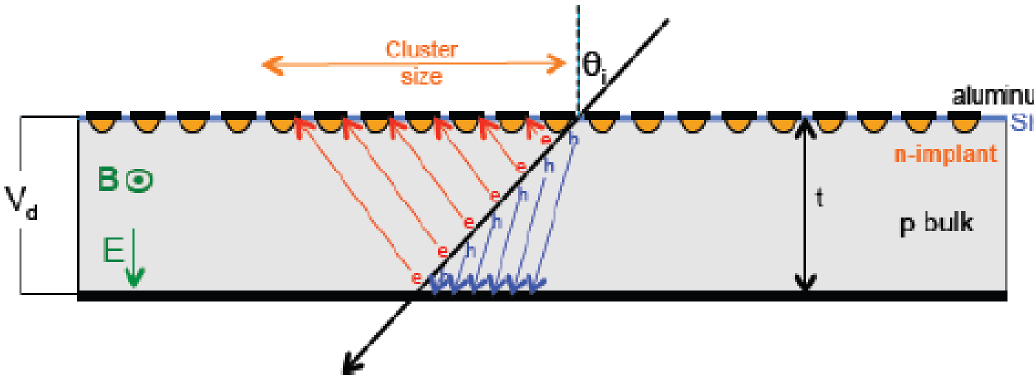
Alessandro Calandri / CPPM

Modifying the sensor thickness

Current digitization method is the drift model:

- carriers drift in the depleted sensor depth taking into account direction of electric field, the Lorentz angle and the diffusion
- Geant4 provides entry point, exit point and energy loss
  - drift path is divided into 50 segments and the total charge is uniformly spread within these segments
  - for each segment, the charge is divided into 10 sub-charges to ensure randomness of the diffusion process.
- The drift is performed between the entrance and the exit point following the Lorentz angle + a Gaussian smearing that accounts for the thermal diffusion
- The signal on each pixel is the sum of all sub-charges that reached that pixel

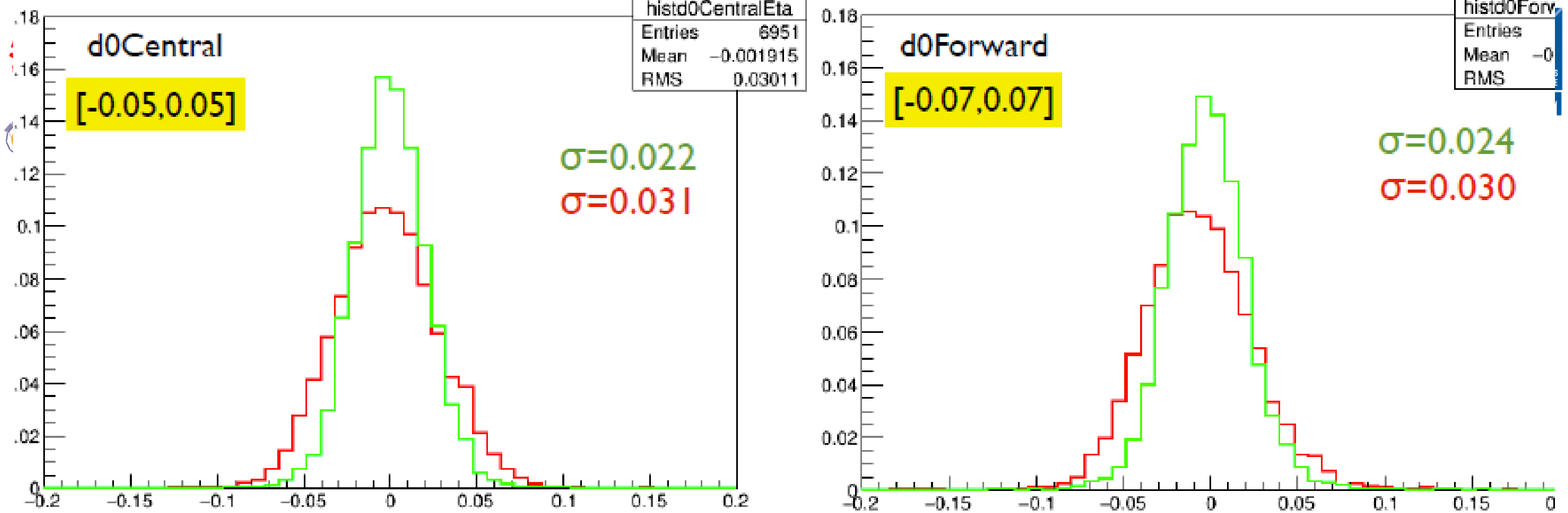
+ pitch reduction Rφ & z → next slides



- The ionization potential for the silicon is regarded as constant
- The Lorentz angle is computed from the conditions of the database (temperature, bias voltage applied on the sensors)

☑ IBLPlanarChargeTool and IBL3DChargeTool inside the package PixelDigitization can be modified to reduce the sensor thickness and perform the charge drift in a smaller depth

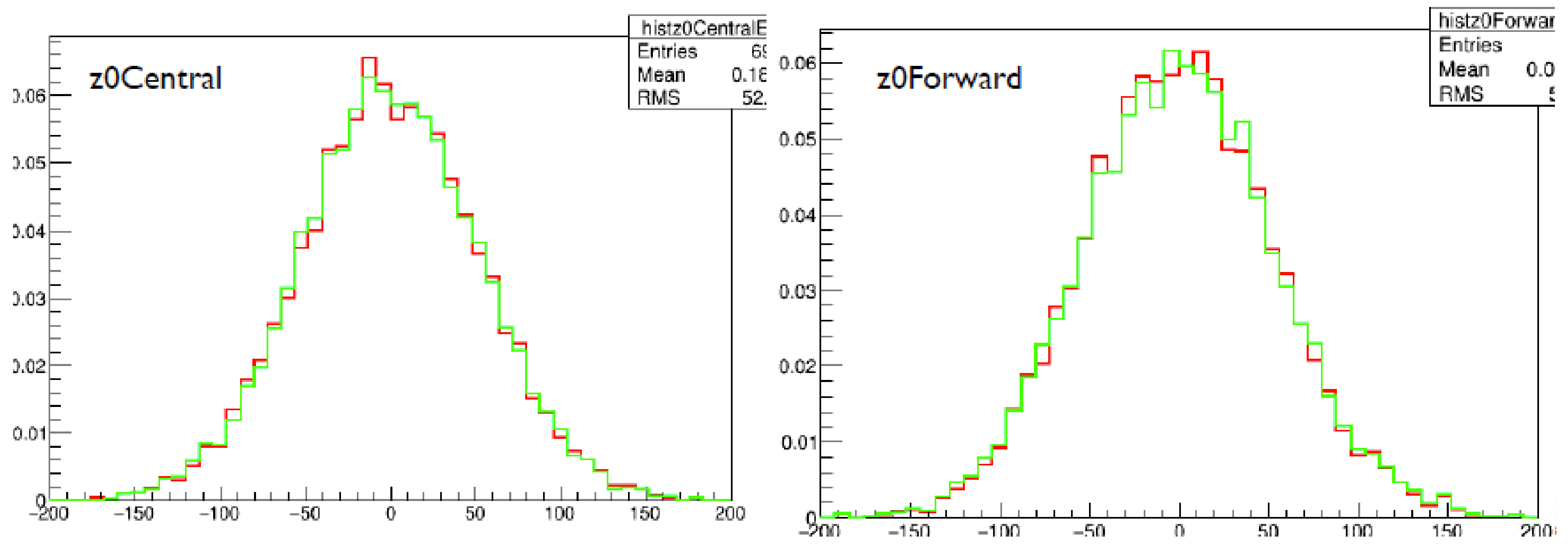
- for this study, I've just modified the depletion depth for planar sensors (IBLPlanarChargeTool)

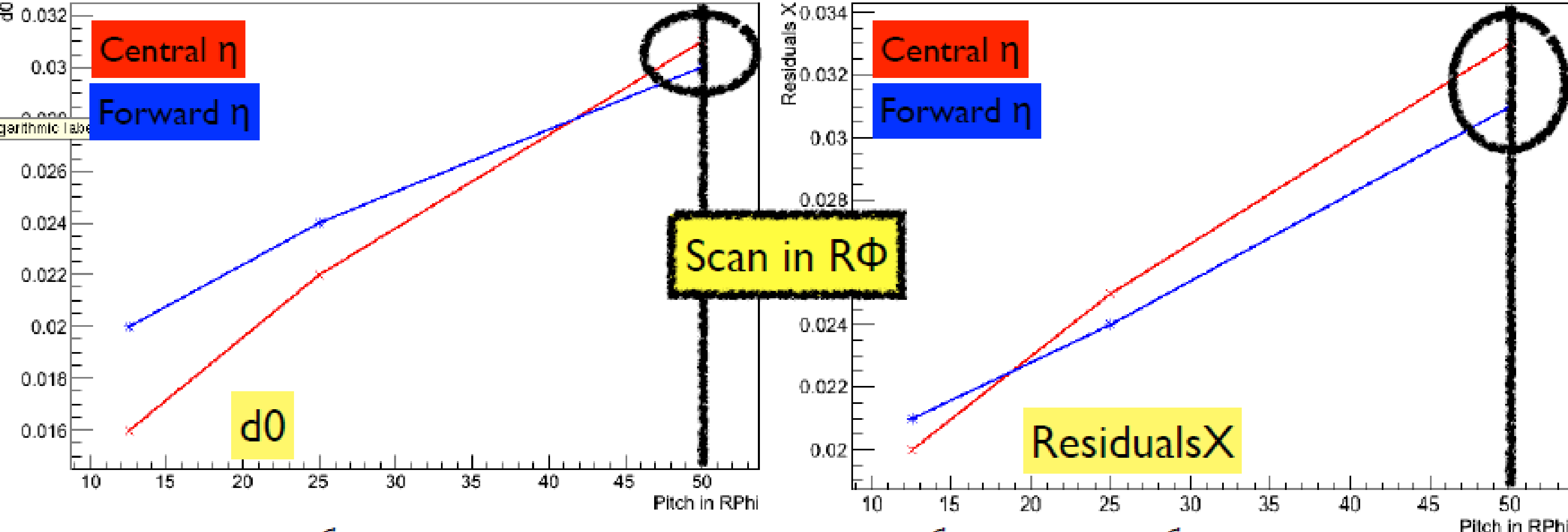


- Modified configuration: pitch in RΦ divided by 2 (50→25 micron)

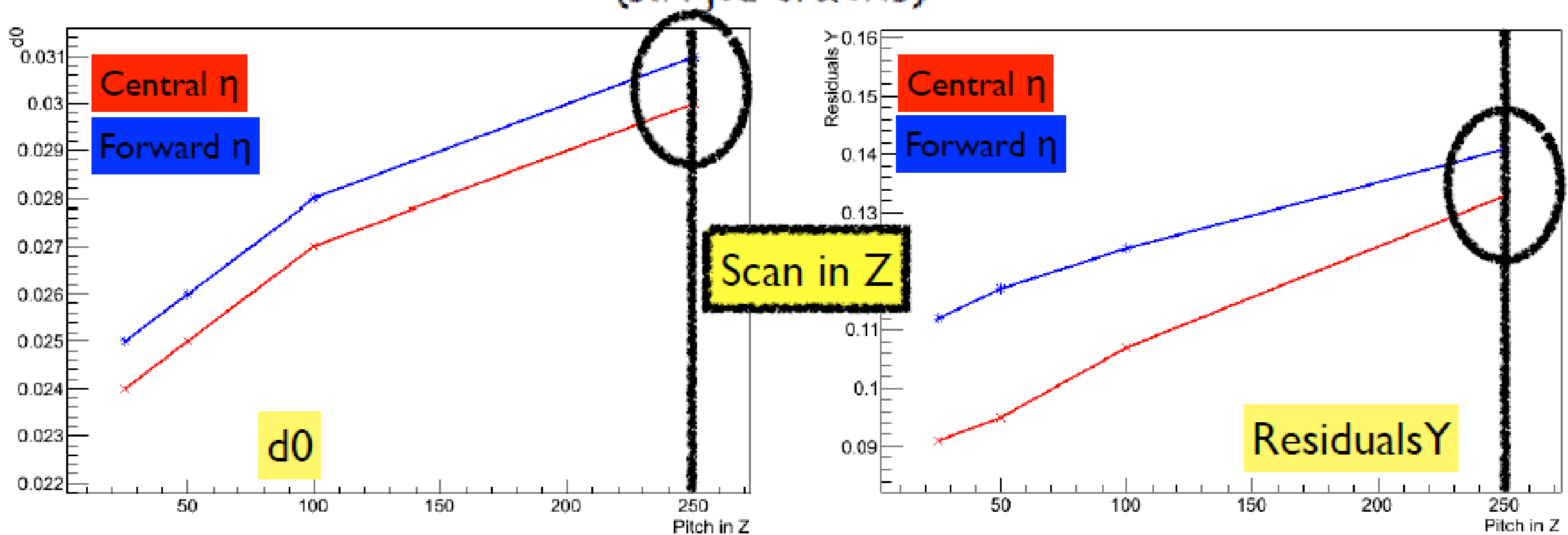
Default

Modified



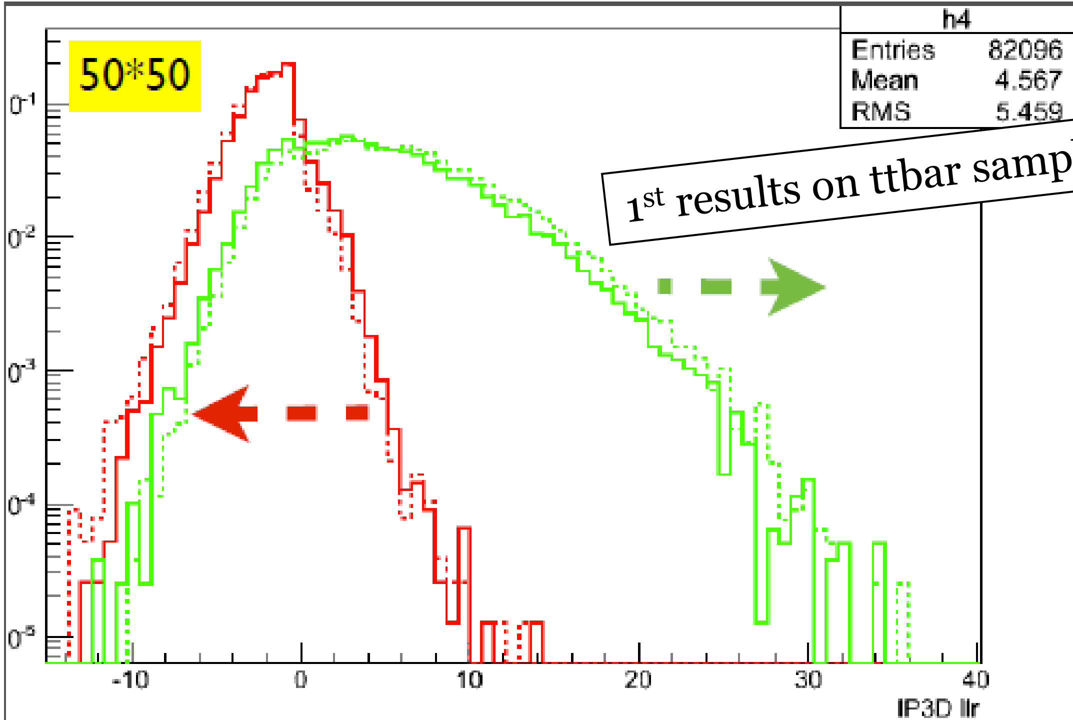


Resolution of tracking parameters as a function of the pitch size (single tracks)



IP3D log likelihood ratio

1st results on ttbar sample!



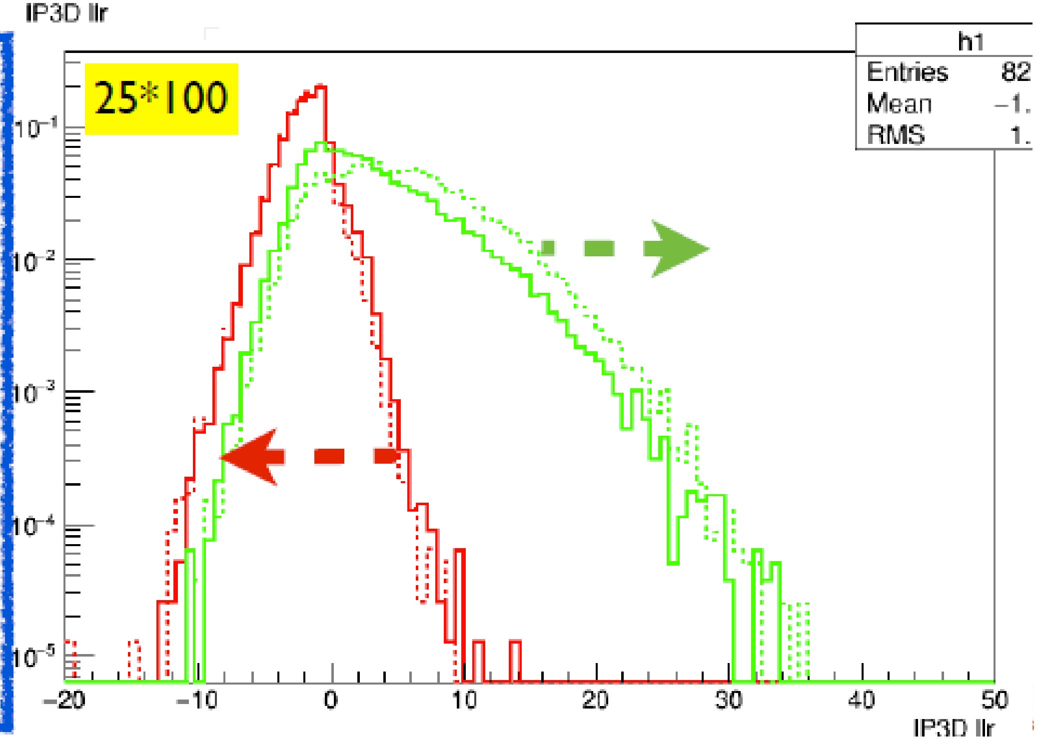
light nominal

light pitch Modified

b nominal

b pitch Modified

- Improvement in IP3D separation for modified pitch due to the gain in performance on the tagger input variables
  - will produce the ROC curve b-jet efficiency vs light/c rejection to check the gain for a given working point of the new approach b-tagging performance-wise
  - gain on final IP3D configuration can be easily translated in overall improvement on MV2 at the end of the b-tagging chain



Wrap-up

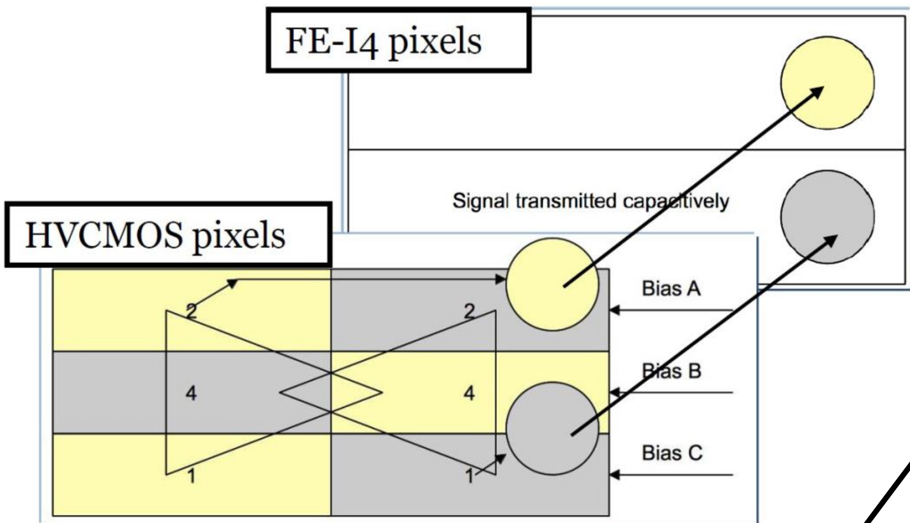
- TCAD simulations led to design in LF
- Characterization in lab, under radiation…
  - → CCPD LF Demonstrator submission in February.
    - → Should be back after the Summer.
  - → Monolithic demonstrator in LF.
- First tries towards assessing potential physics performance of technology at small radius.
  - – Scan pitch
    - Single track muons.
    - ttbar.

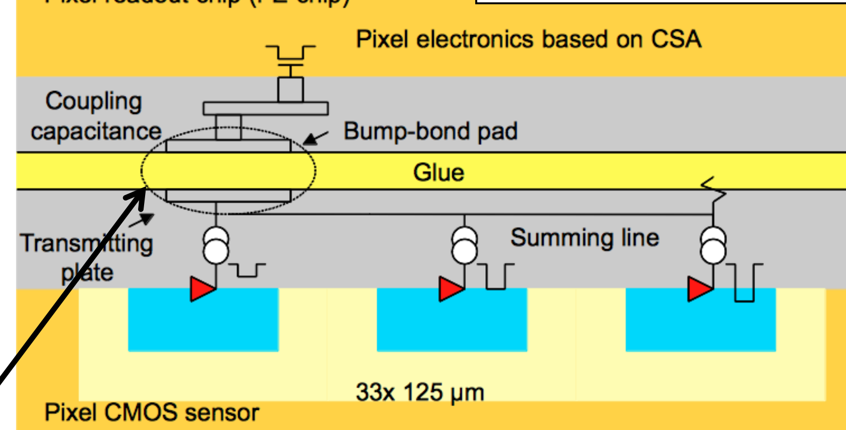
Backup

Readout -with larger pixels-

- Combine 3 pixels together to fit one FE-I4 pixel (50×250μm²), with HVCMOS pixels encoded by pulse height.

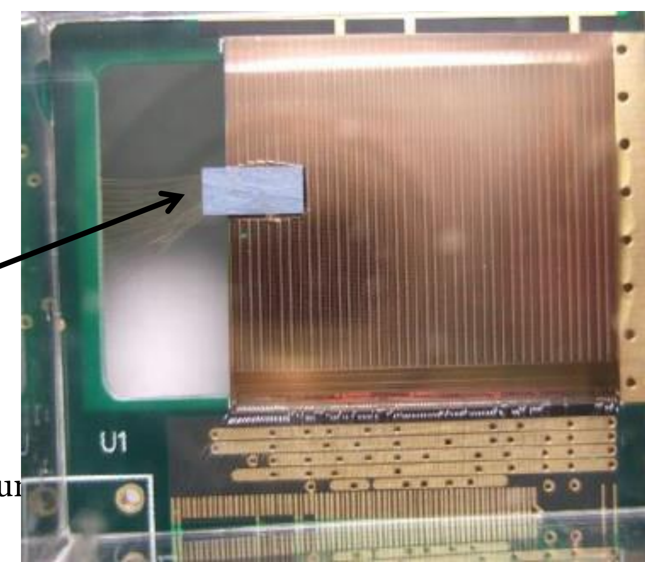
à la 3D electronics!





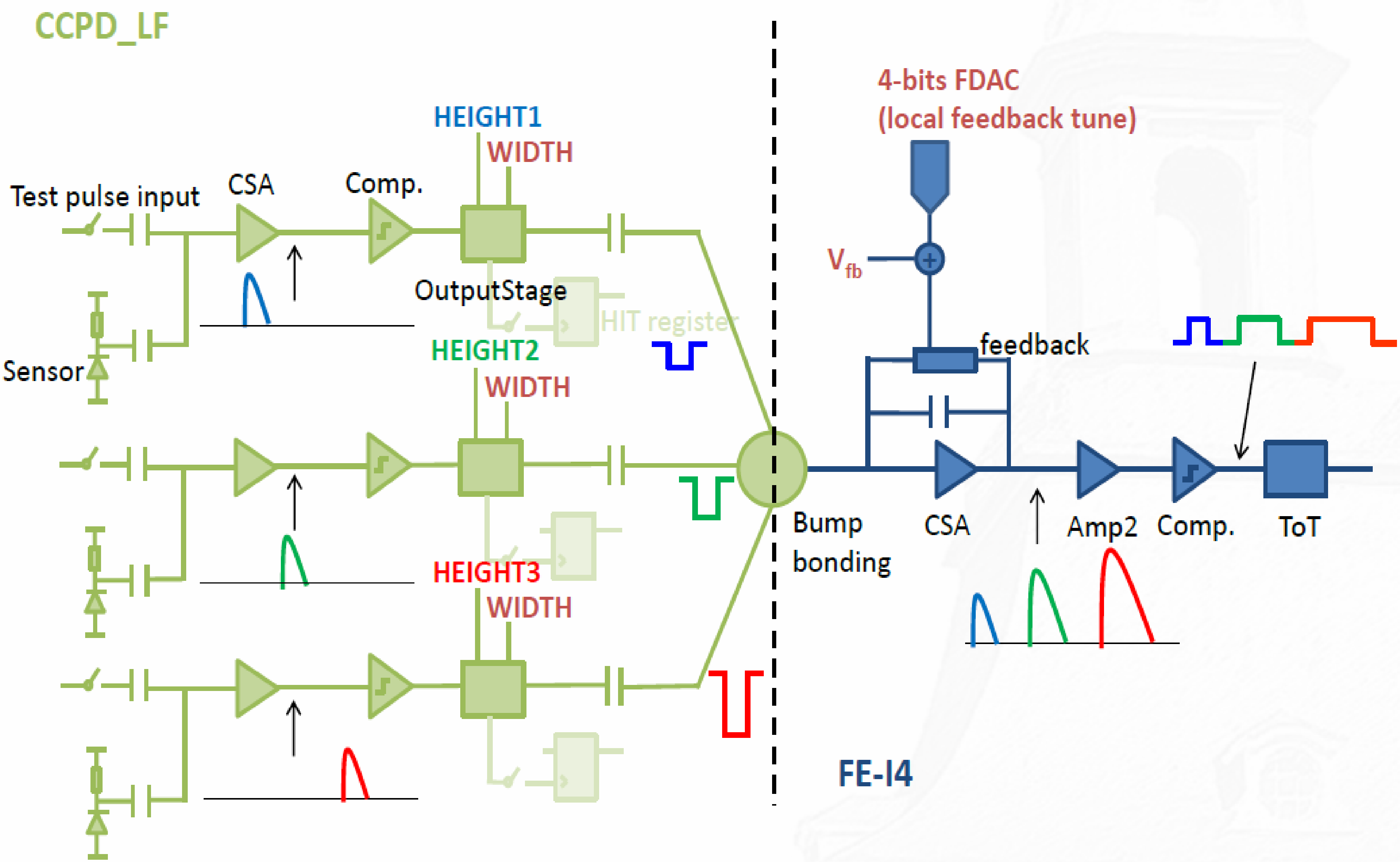
- Capacitive coupling OK: gluing!

(perspective to avoid bump-bonding?)



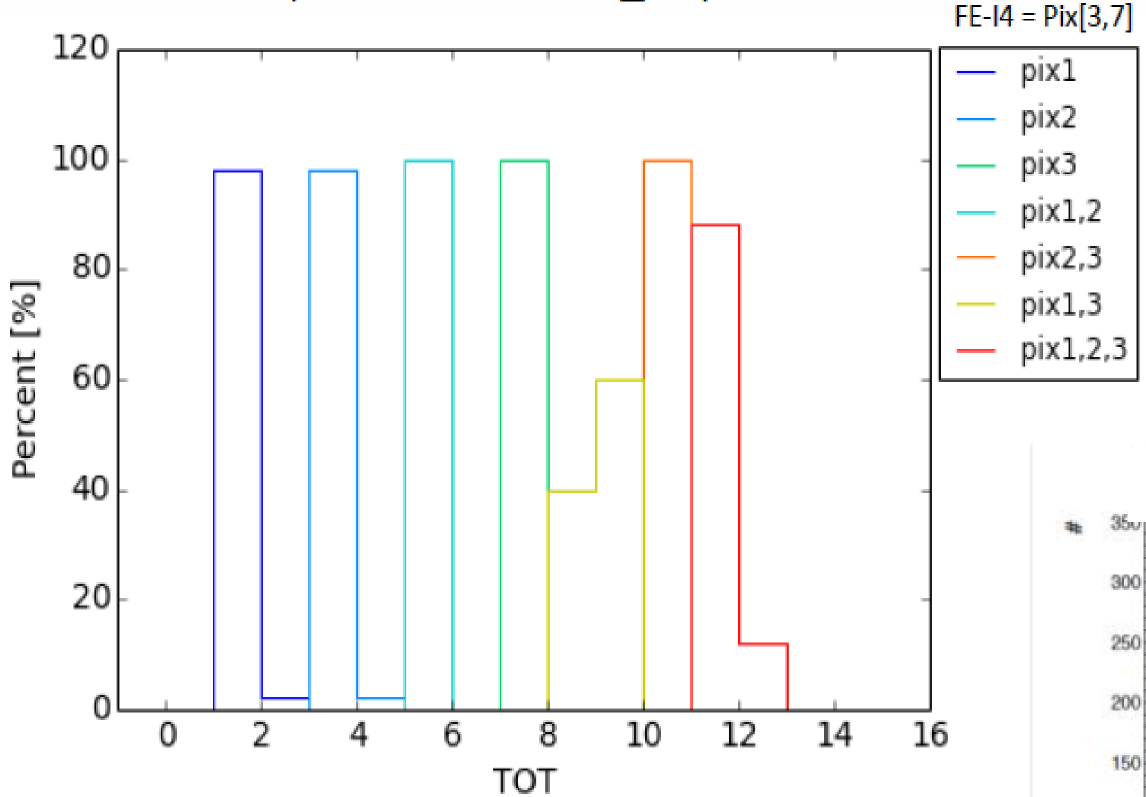
The tiny HV2FEI4p1 prototype glued on the large FE-I4

Readout of CCPD_LF and FEI4



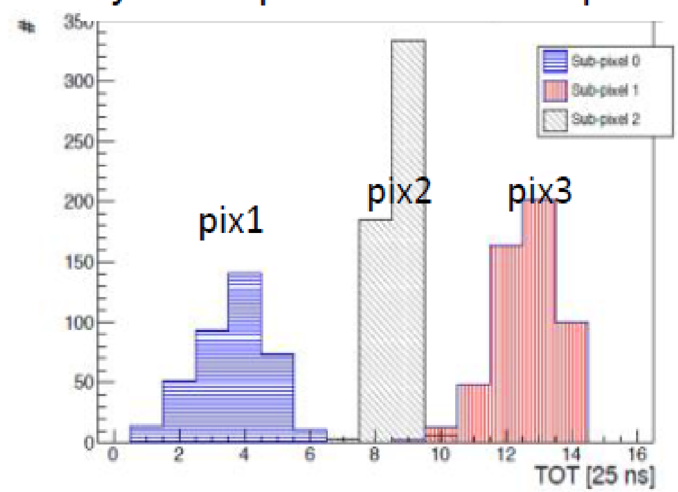
ToT dispersion of 1 “good” FE-I4 pixel (test pulse injection)

ToT response of 3 CCPD_LF pixels



- Subpixel encoding works in some pixels
- Dispersion of ToT can be tuned to be ~2ToT

cf. ToT response of 3 HV2FEI4 pixels

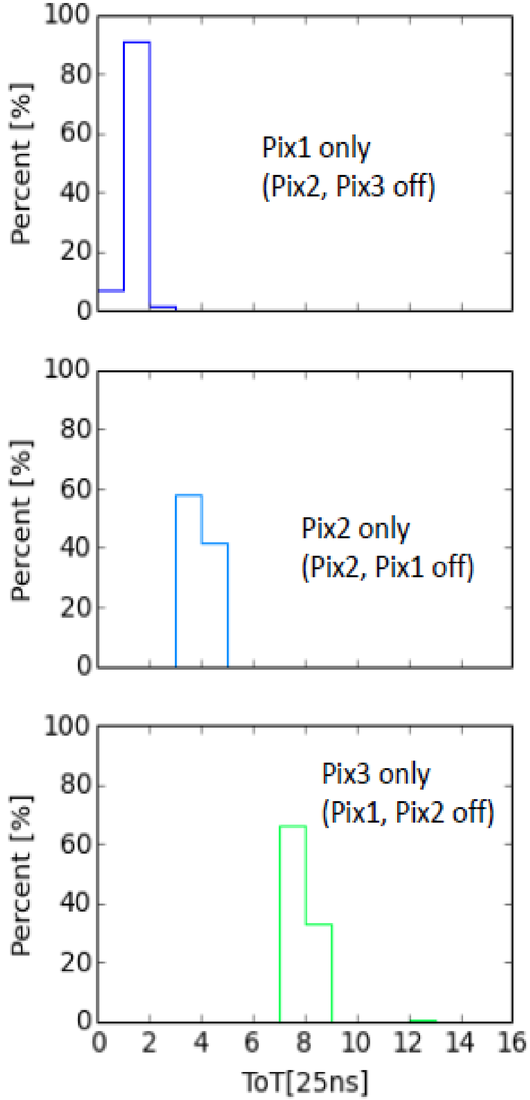


M. Backhause Thesis (2014)

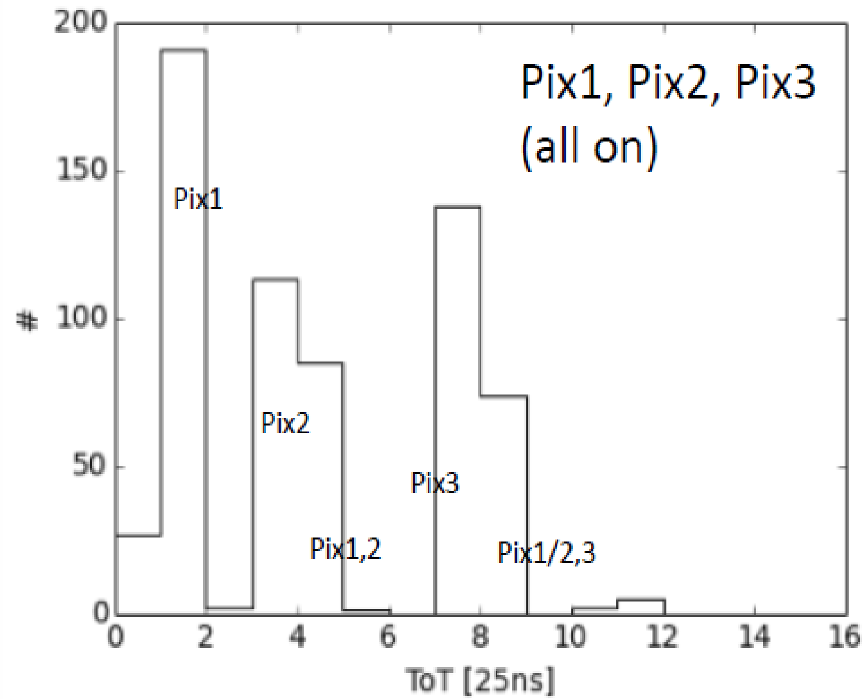
ToT value of a FE-I4 pixel (3.2GeV electron)

universitätbonn

ToT response of a single FEI4 pix



ToT response of a single FEI4 pix

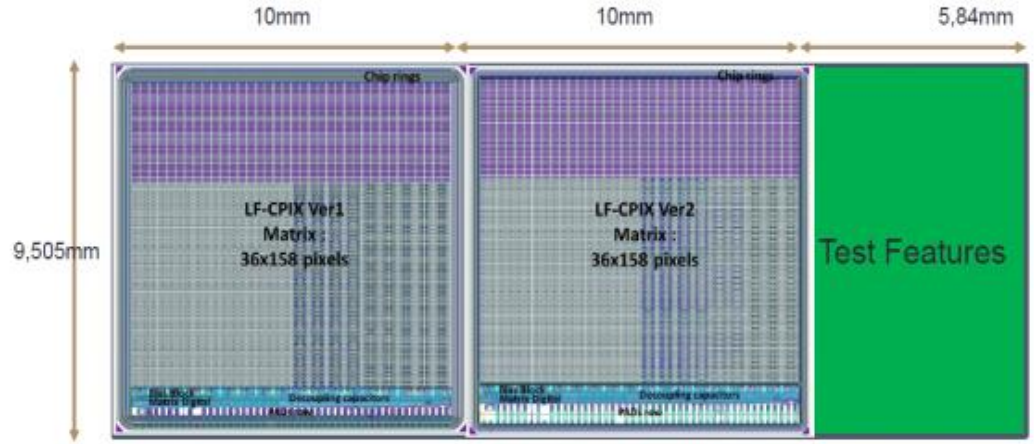


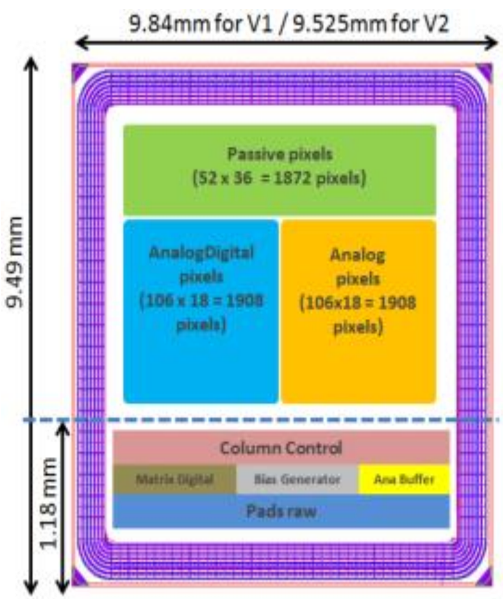
- Sub-pixel encoding works for real beam
- Detailed analysis is on-going

LF-CPIX Demonstrator

LF-CPIX : + Fully I

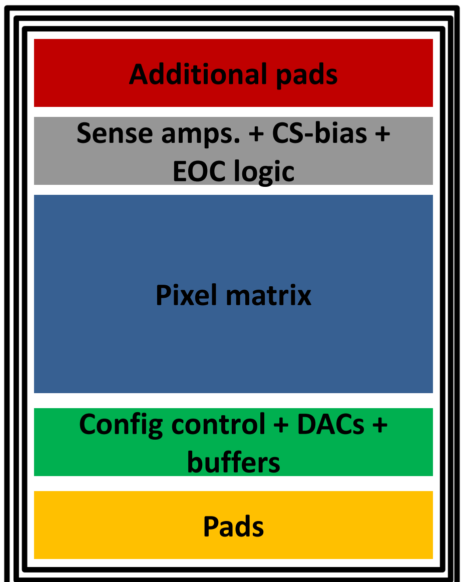
- 150nm CMOS (Avezzano, Italy)
- 2kΩcm p-type bulk
- Deep N-Well/P-Well available
- HV process
- CPPM + IRFU/CEA + Bonn

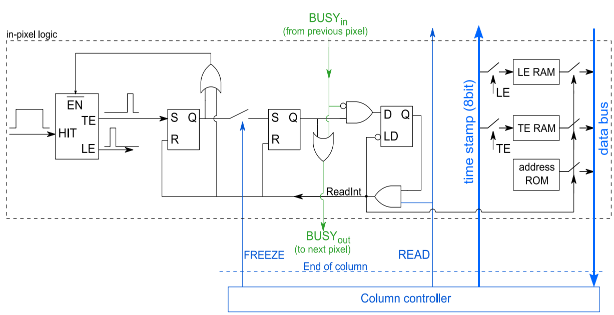




submitted 03/2016

LF-Monopix-01 Fully Monolithic



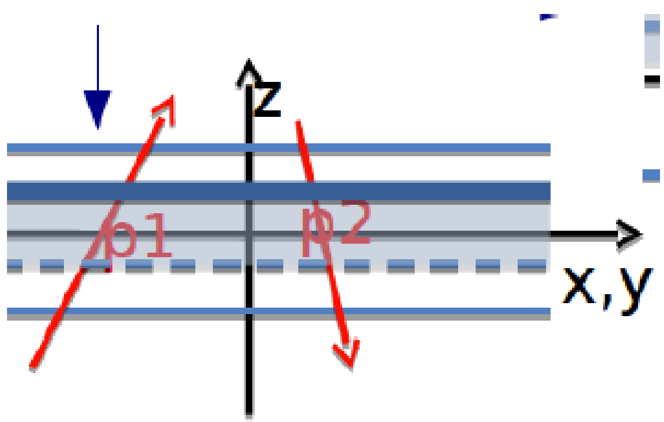


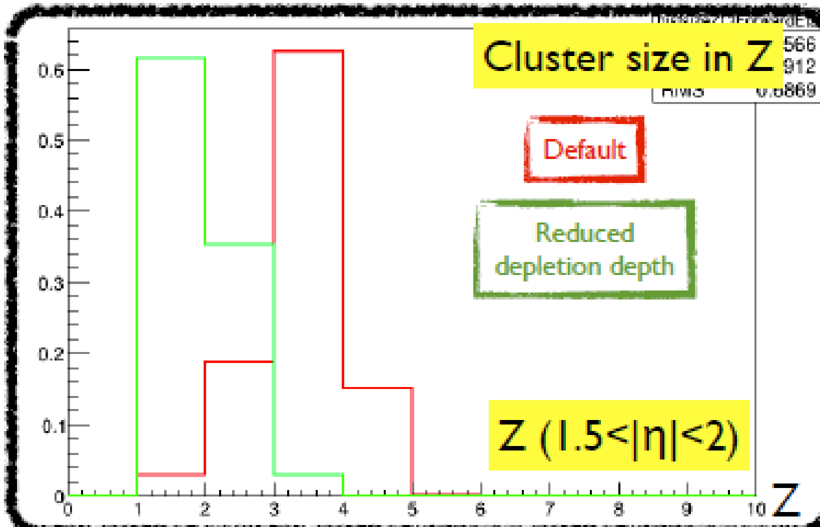
submission 05/2016

hemperek@uni-bonn.de

Modifying the sensor thickness (2)

- Depletion depth divided by 10 in the active region for IBL planar (200→20 μm) - symmetric wrt 0 in depth
- Relevant thresholds (the DB has been disabled in such a way that values can be modified by hand) for IBL divided by 10 accordingly (naively assuming linear scaling of thresholds vs sensor thickness in the charge drift) in PixelConditionService package (PixelCalibSvc), namely:
  - discrete threshold IBL: 1500→150, in-time threshold IBL: 1900→190, threshold noise: 200→20
- The current NN-clustering (flag in InDetJobProperties) switched-off for this study as the NN-based is not retrained for the new conditions, same for the clustering option in dense environment (TIDE)





- Lorentz angle correction in the RPhi plane properly taken into account when the depletion depth is modified:
  - LorentzCorrection in Phi→ tanLorentzPhi•depletionDepth (factor that gives the effective correction in the reconstruction frame)

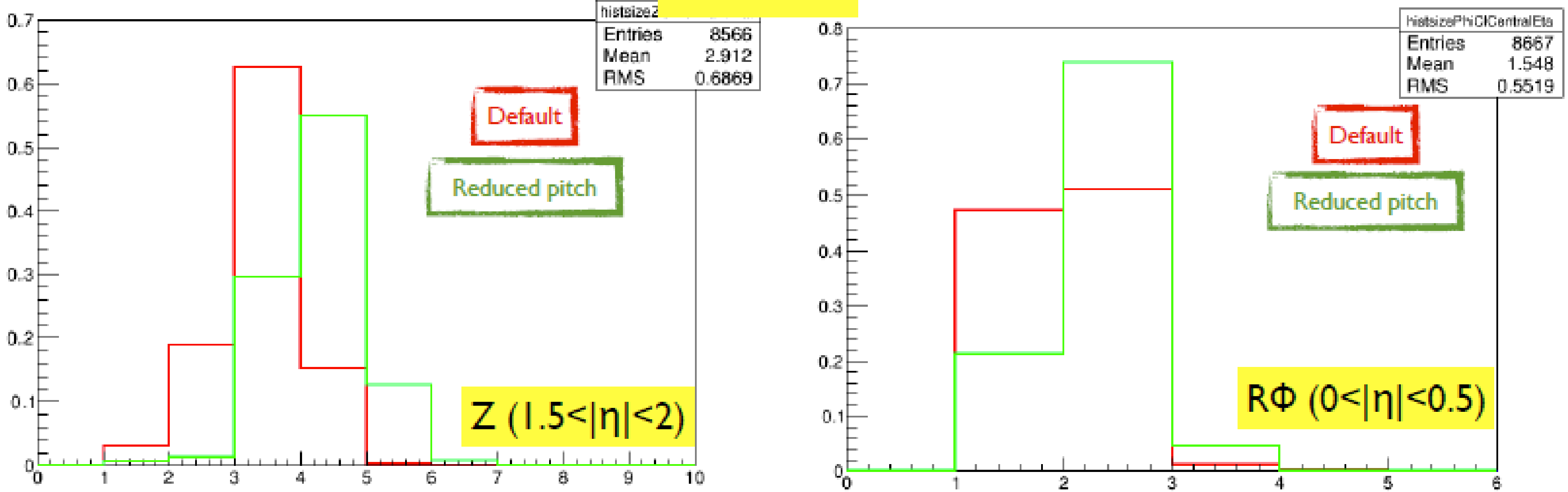
Modifying the pixel pitch in the IBL

- IBL pitch in RPhi/Z can be modified by overwriting the values stored in the DB with a txt file inside the InDetIBLExample package
  - values in the DB refer to the geometry tag I've used for this study, i.e. R2-2015-03-01-00
  - local dictionary (IDDictInnerDetector_readout.xml) modified to account for the new conditions (maxValues of the indices in Phi and Eta identifying the pixels varied according to the change in pitch)

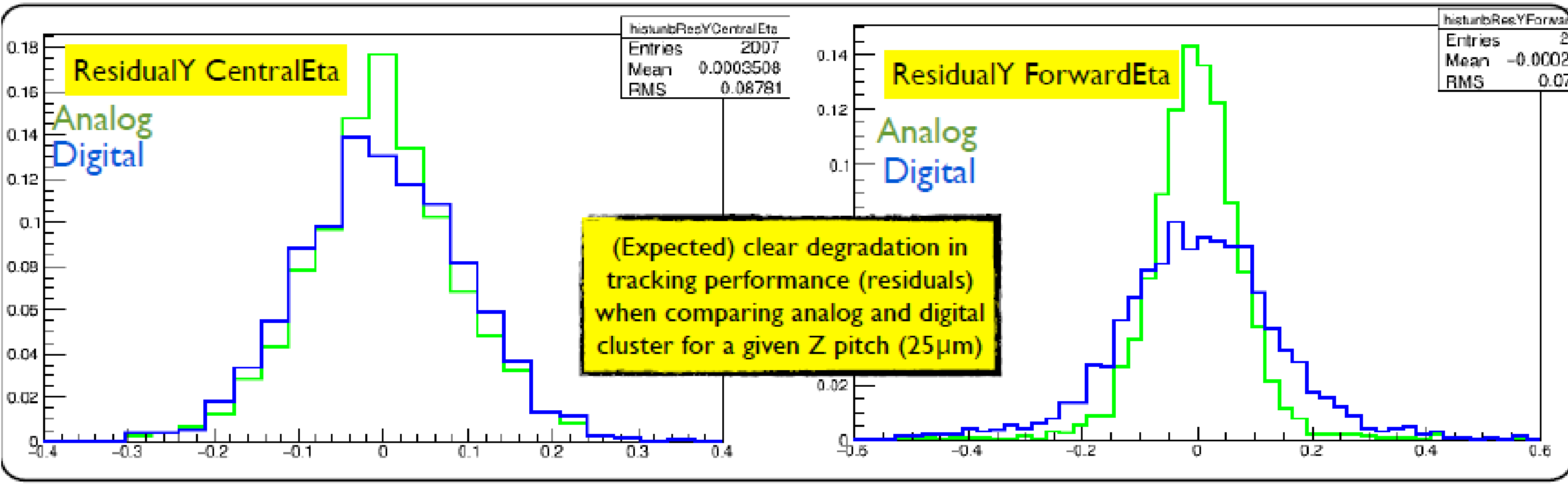
PITCHPHI	PITCHETA	PITCHETALONG	NCHIPSPHI
double	double	double	int
.05	.4	.6	2
.05	.25	.45	1
.05	.25	.25	1

- Default configuration: RΦ-Z: (50X250) μm
  - will show in the following slides a test on the tracking performance for a reduced pitch in RΦ (divided by 2, 50→25 μm) and Z (divided by 5, both for the normal pixels and the long ones, 250→50 μm, 450→90 μm)

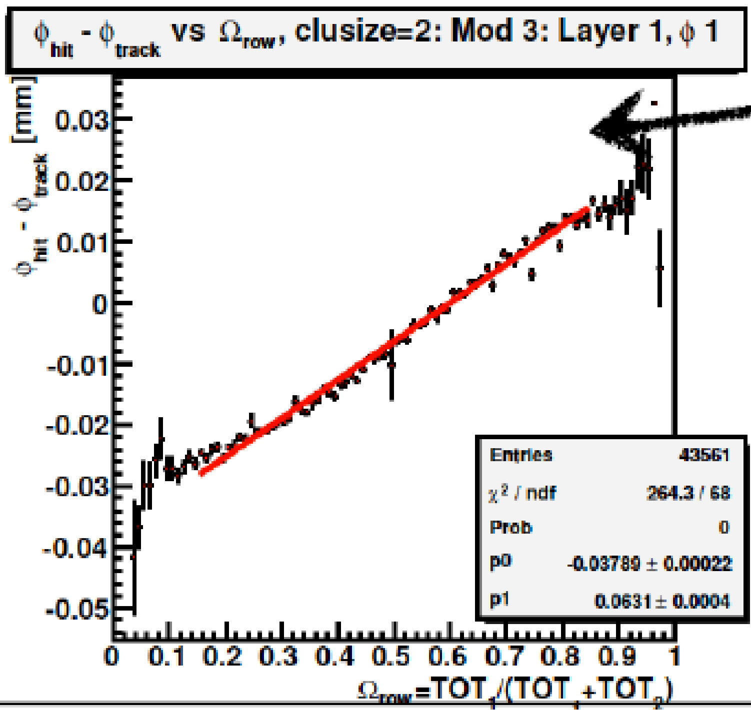
Cluster size



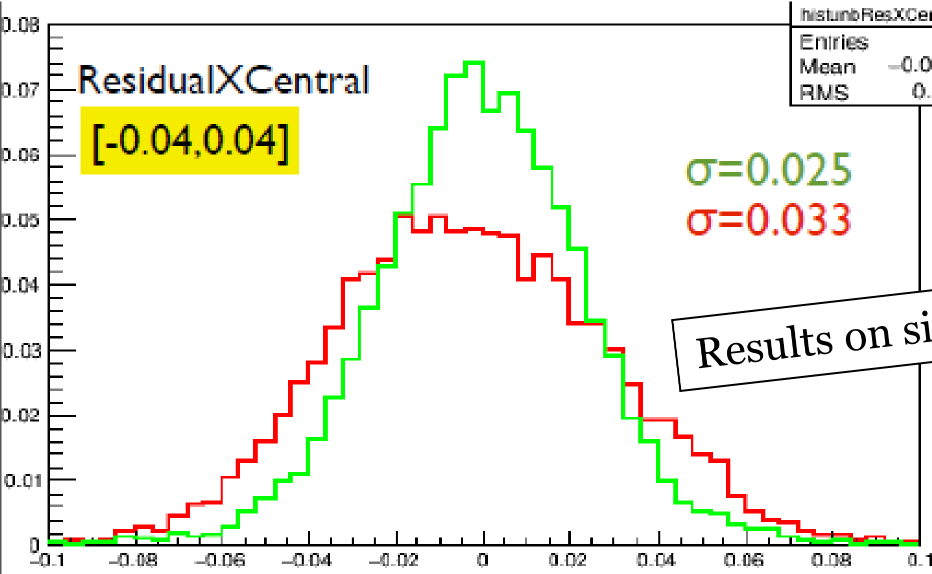
Pixel clustering algorithms (2)



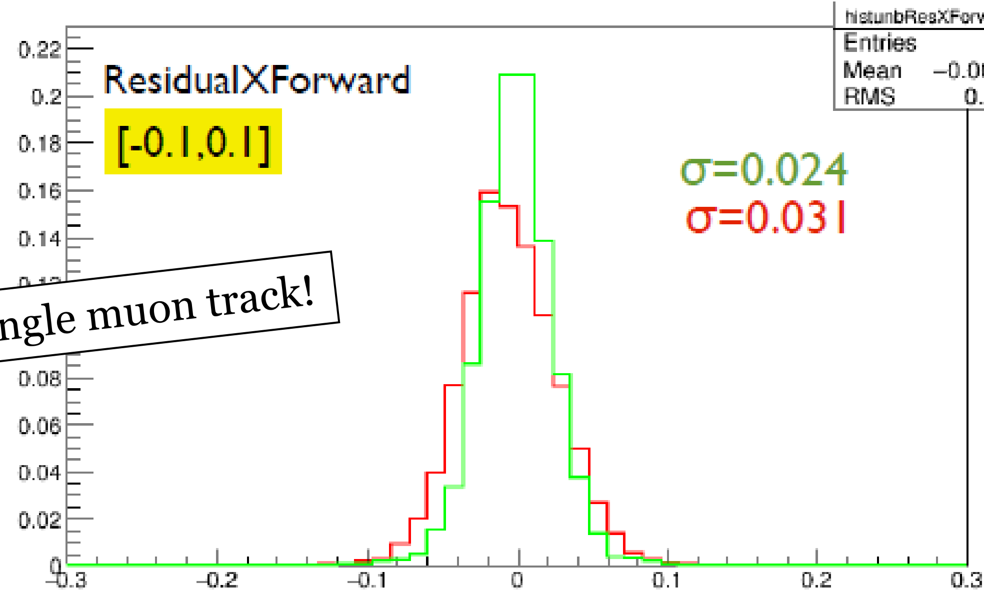
(Expected) clear degradation in tracking performance (residuals) when comparing analog and digital cluster for a given Z pitch (25µm)



- Example of the linear fit to extract the slope Δ in bins of cluster sizes in Phi and Z for the IBL
- Will have to reproduce the fit for each region and update the hard-coded file
- Results exploited by using digital clustering both for the default and modified case in order to remove clustering-related issues (no charge interpolation)
  - remarkable improvement in residuals/d0/pulls of the modified configuration (reduced pixel pitch in RPhi and Z) wrt to the nominal approach



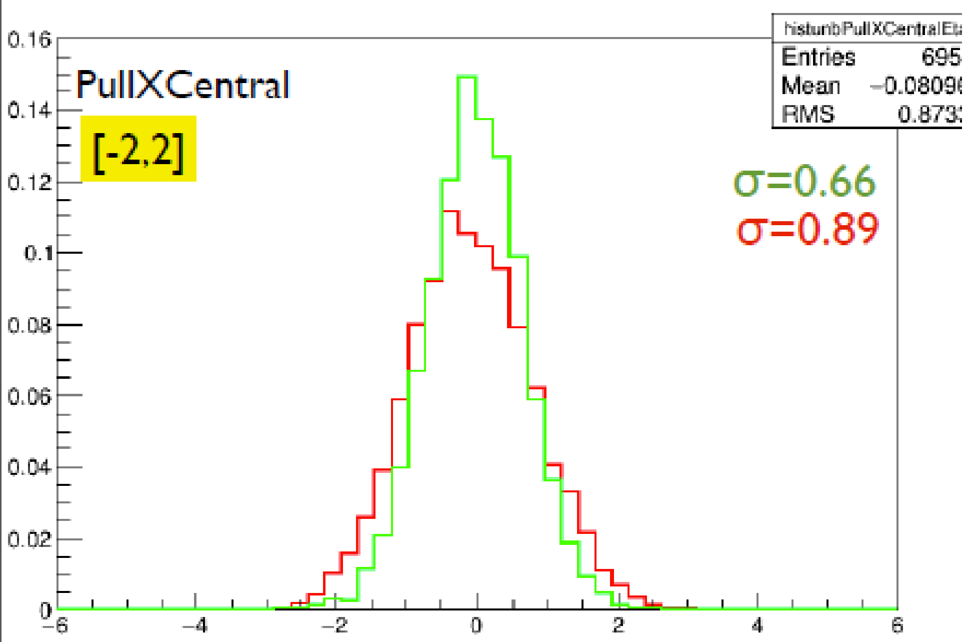
Results on single muon track!

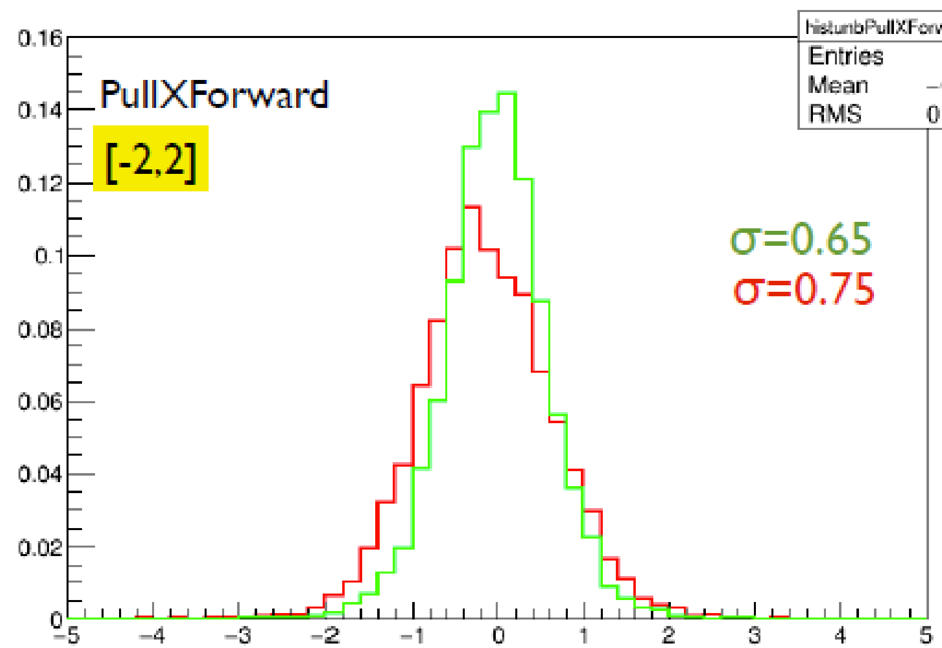


Default

- Modified configuration: pitch in RΦ divided by 2 (50→25 micron)

Modified

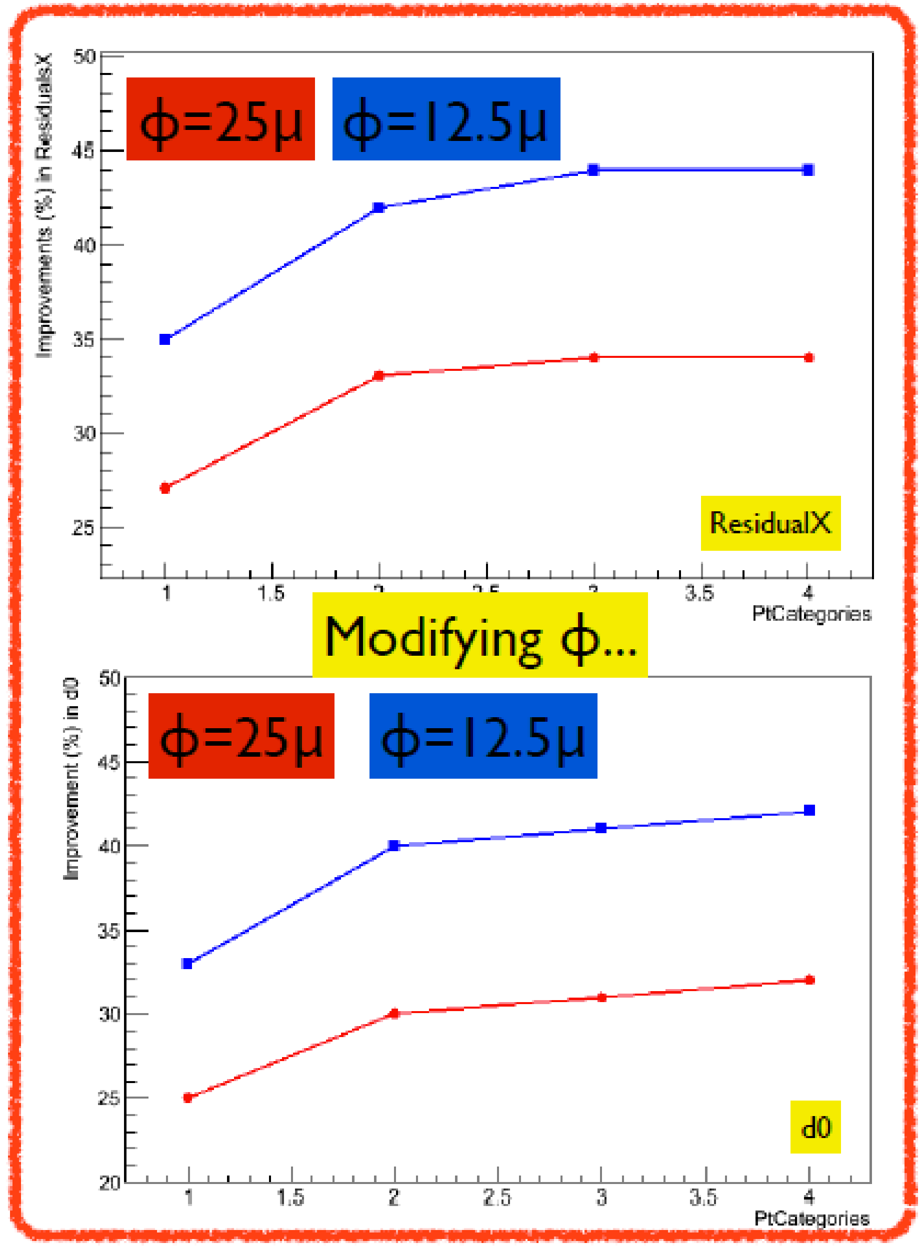


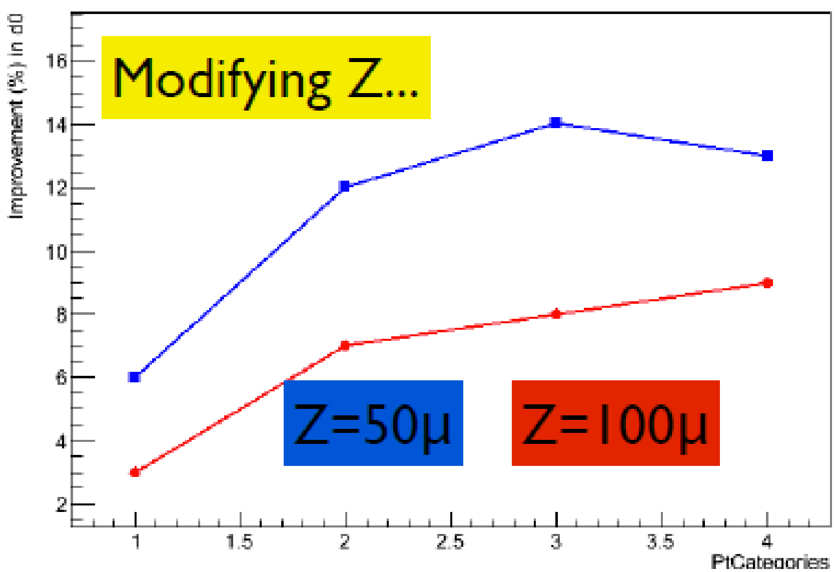


Results

- For low pt tracks (<20 GeV), the improvement in residuals and impact parameter is of the order of 35% (25%) when the pitch in Rϕ is divided by 4 (2). Same trend in Z (d0) although the absolute values of the typical gain are smaller
- Additional gain for tracks in the pt region 20-40 GeV (~5% improvement compared to the previous case)
- No significant changes in gain above 40 GeV (improvement, 40/30% in Rϕ and 8/15% in Z, wrt the nominal configuration is flat vs pt)
- No dependence (expected) in pt noted in the local Y residuals distributions

Pt cat: 0-20/20-40/40-60 /60-100 GeV





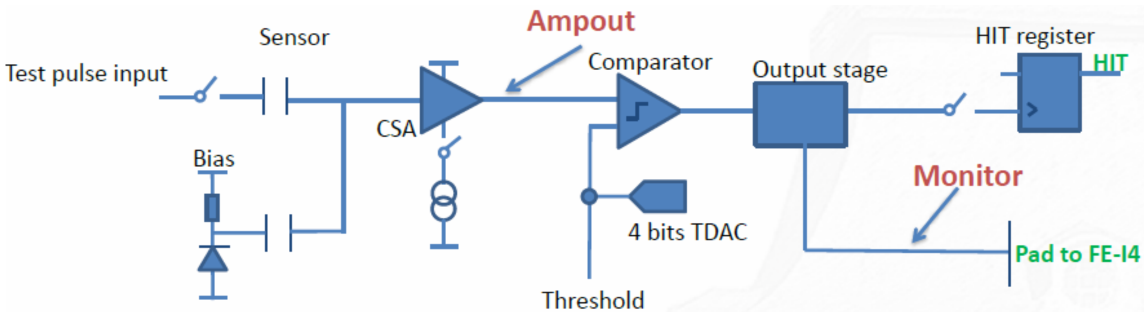
Wrapping up/ongoing activities

- Working on pixel simulation in light of possible usage of HV-CMOS technology for pixel ITK
  - fine pixel granularity and small depletion depth can result in better performance on the tracking and pattern recognition
  - using only 20μm (depletion depth) of 200μm sensor will result in large multiple scattering from the full depletion depth, hence results shown here can be regarded as lower bound of the realistic simulation for small CMOS depth
- Checks deployed on single track samples and ttbar with Run 2 geometry (only in the IBL planar region)
  - the depletion depth of the sensor is decreased by factor 10 (200→20 μm) and the relevant IBL-related thresholds have been varied accordingly
  - the pixel pitch (RΦ and Z) is decreased from its current value (250*50 μm) in order to simulate different sensor geometries for the HV-CMOS detectors
  - set of checks on the pixel clustering algorithm deployed in the analysis→results are shown for digital clustering: remarkable improvement in tracking performance (25-30%) due to the reduced pixel pitch

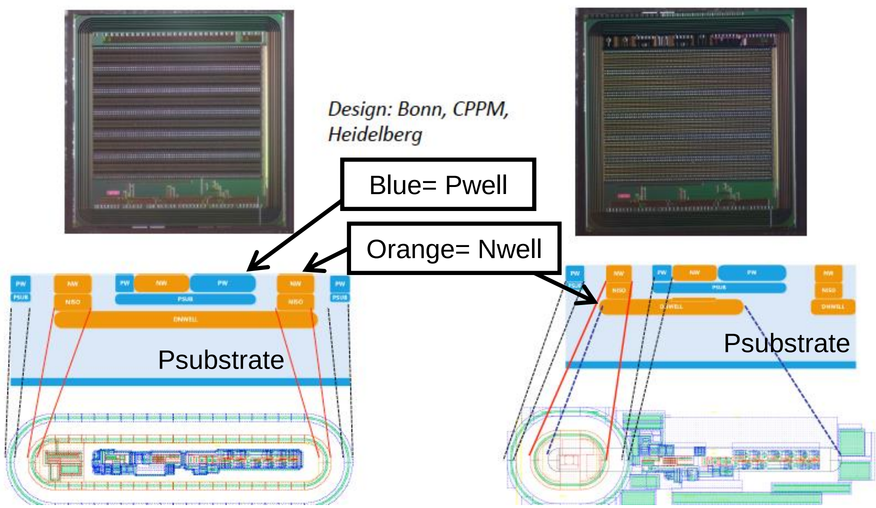
Ongoing activities and plans for the future

- Will complete the study on ttbar by gauging the improvement brought by the gain in resolution on Sd0/Sz0 on the IPTag performance
  - encouraging results found in the enhancement of b vs light log-likelihood ratio separation
- Will reproduce these studies (single tracks and ttbar) and assess the typical gain in the ITK framework by exploiting the different layouts that are currently being examined by the ATLAS ITK Simulation and Tracking group
- Plan to write a note summarizing and documenting these studies on HV-CMOS simulation once thoroughly completed

LF VA/VB 2015 version

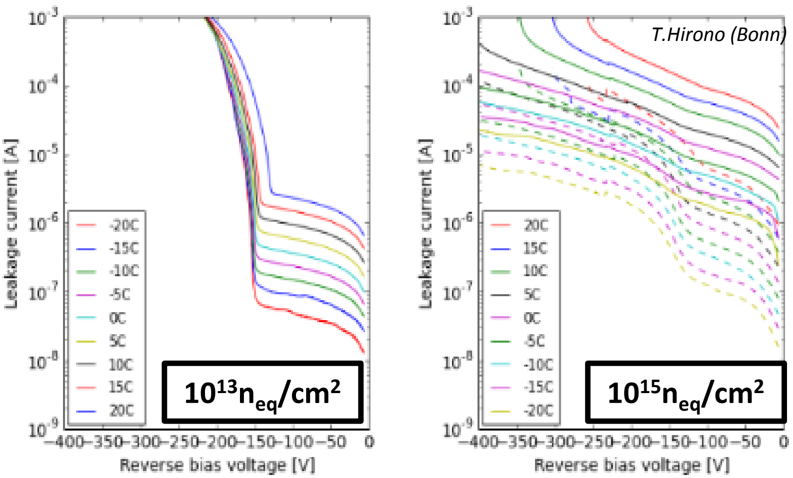


- **CCPD LF VA**
  - CMOS inside collection electrode
  - Test structures: NMOS and PMOS transistors
- **CCPD LF VB**
  - Smaller collection electrode
  - Test structure: diodes

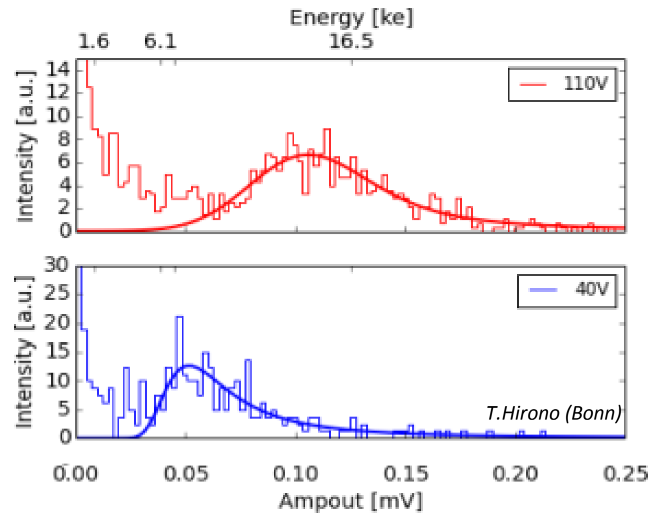


LFoundry (first submision results)

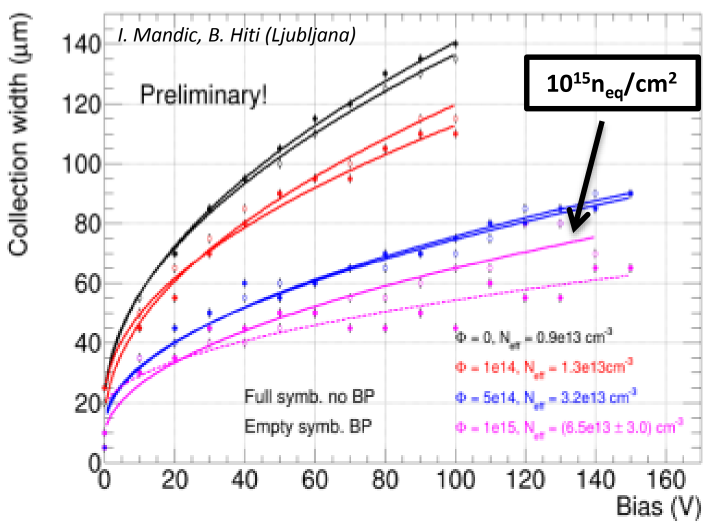
Sensor reverse current



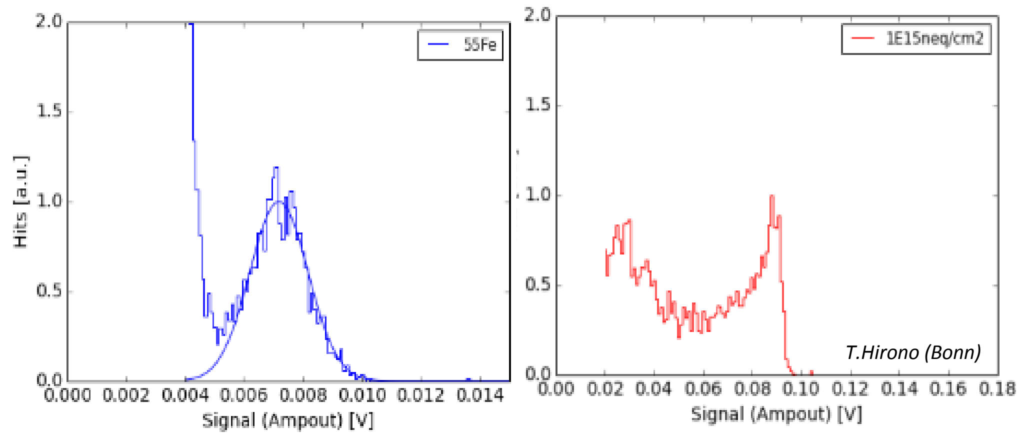
MIP (3.2 GeV) spectrum (before radiation)



Collection width (edge-TCT)

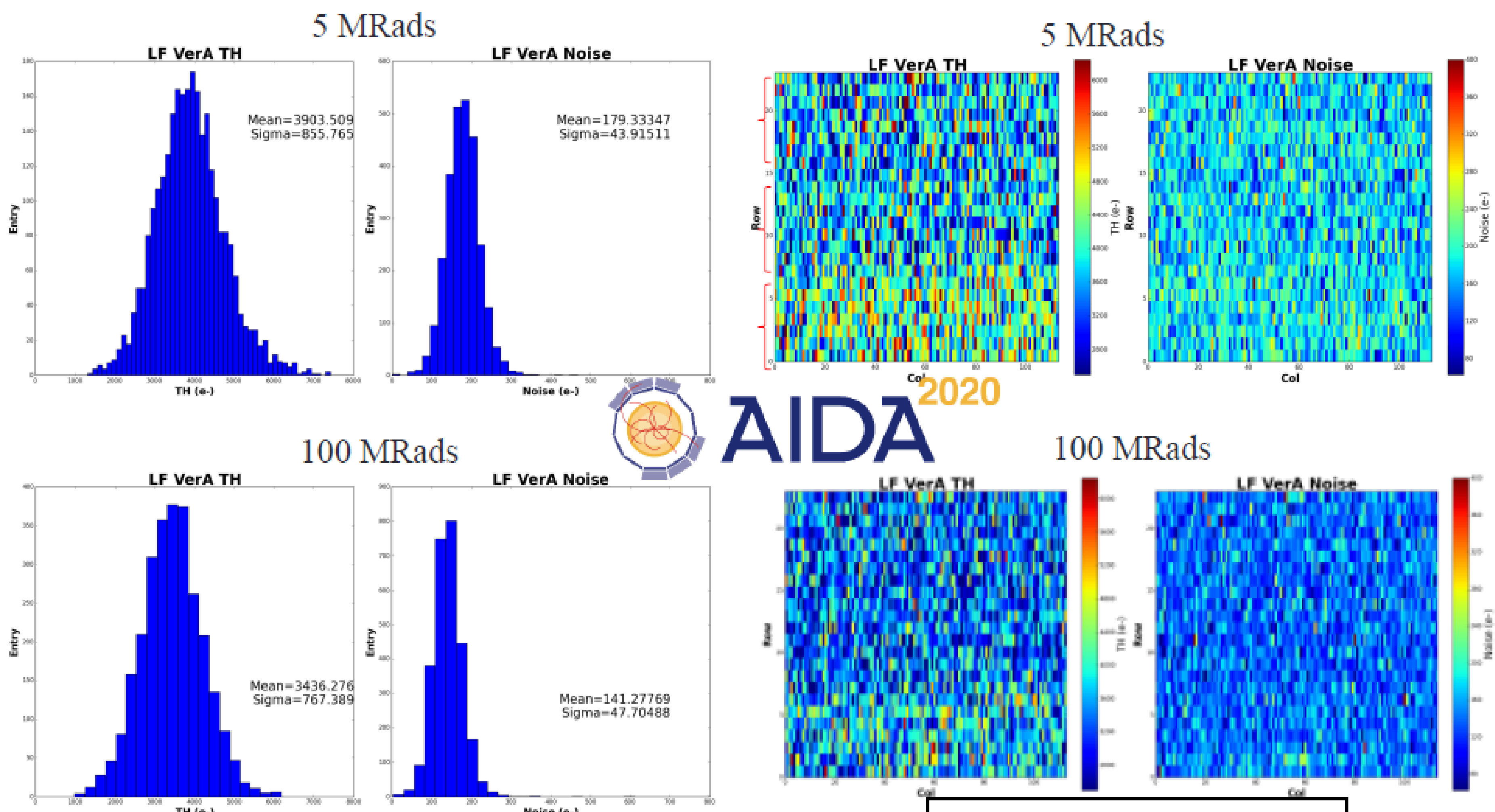


Sepctrum of ^{55}Fe and ^{241}Am after $10^{15}n_{eq}/cm^2$



hemperek@uni-bonn.de

CCPD-LF irradiated to 100Mrads protons beam



Jian Liu (CPPM/Shandong)

The pixels electrical parameters not really affected by the protons irradiation (10-20% variations)