ATLAS Silicon Strip Electronics

(Electronics for the ATLAS ITk Strip Detector)

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A.A. Grillo

SCIPP – UCSC

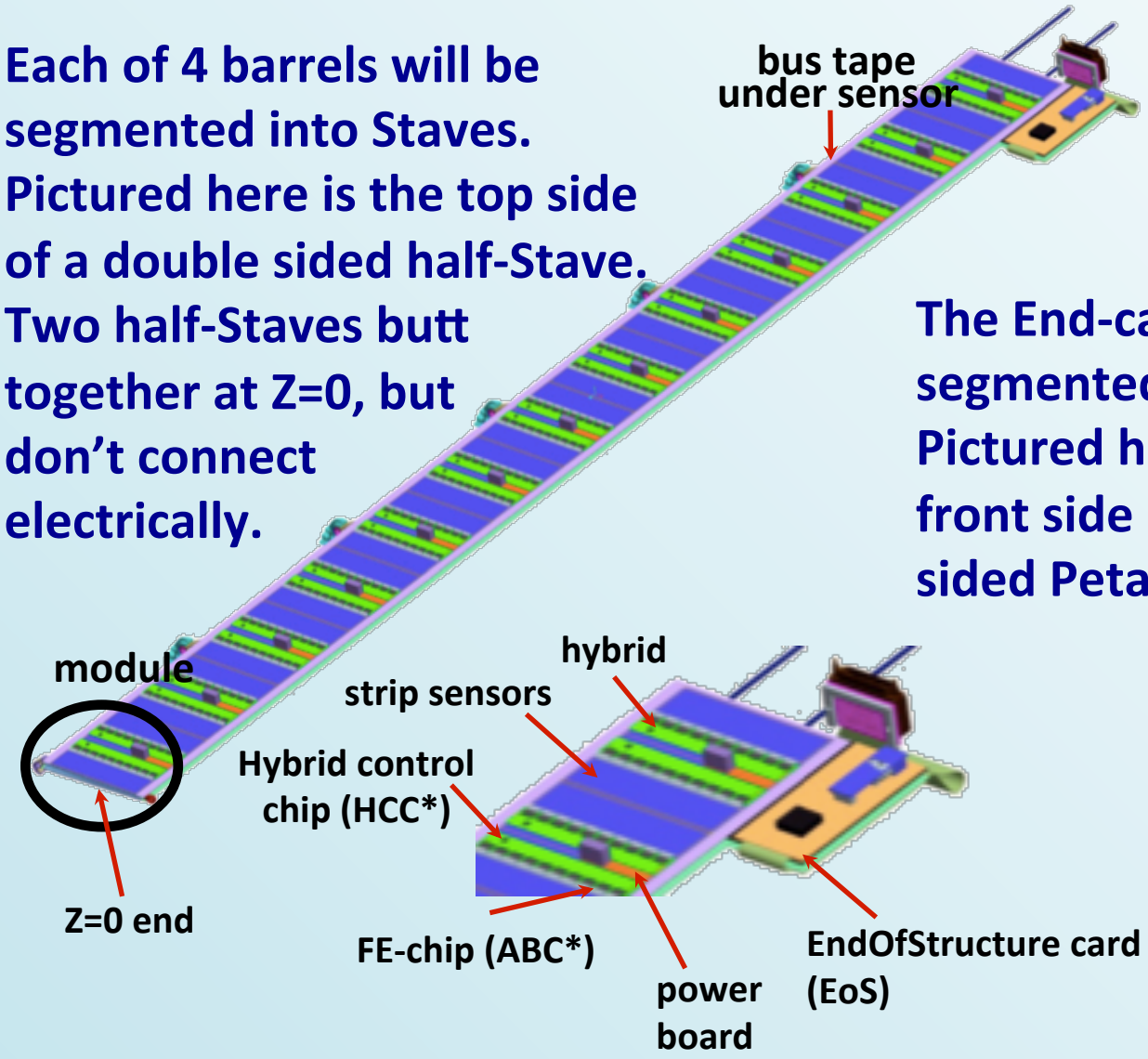
For the ITk Strip Community

ATLAS ITk

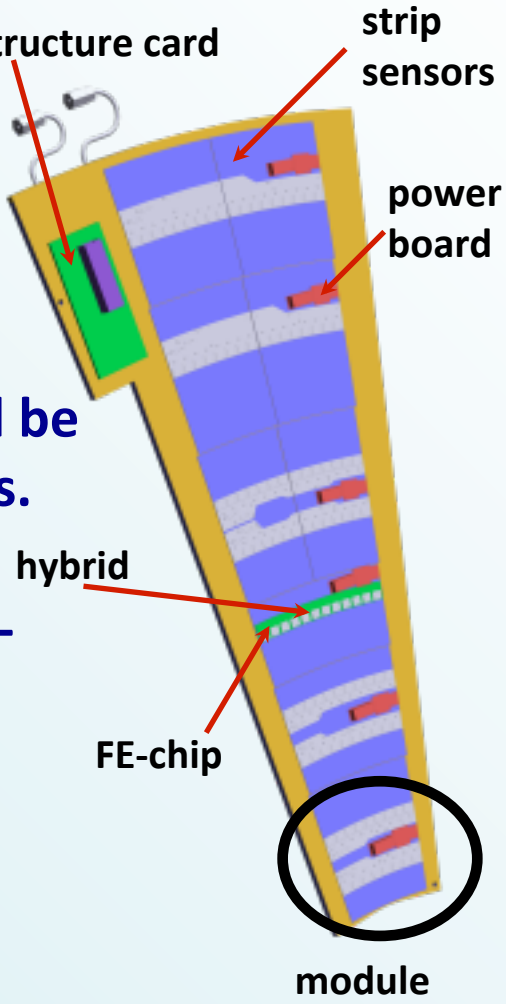
- The Phase II Upgrade of the ATLAS Inner Detector is now named the ITk (Inner Tracker).
- As Steve has already presented, it will be an all silicon detector made up of a Pixel detector at small radii and a strip detector at somewhat larger radii.
- This talk will focus on the electronics for the strip detector – there will be a following talk covering the pixel detector electronics.
- And since Peter already covered powering possibilities for the tracker yesterday, I will just glance over that and focus mainly on readout and control.

Staves & Petals: Basic Integration Units

Each of 4 barrels will be segmented into Staves. Pictured here is the top side of a double sided half-Stave. Two half-Staves butt together at Z=0, but don't connect electrically.



The End-cap disks will be segmented into petals. Pictured here is the front side of a double-sided Petal.

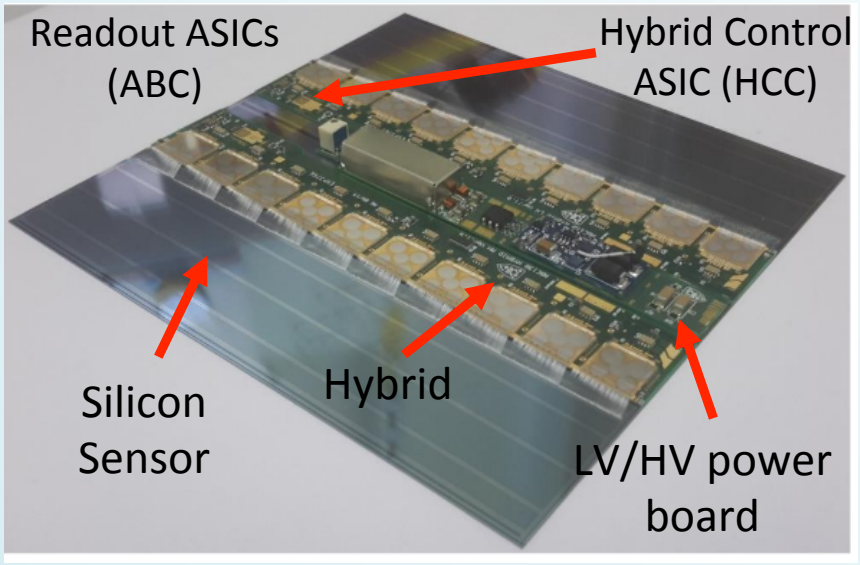


A Very Large Increase in Size and Complexity

- **Comparing the new ITk tracker to the existing ATLAS SCT:**

The New ATLAS ITk Strip Tracker						The Existing ATLAS SCT Tracker		
Number of Full Length Double-Sided Staves	Number of Barrel Modules	Number of Double-Sided Petals	Number of End-Cap Modules	Number of Readout Channels		Number of SCT Barrel Modules	Number of SCT End-Cap Modules	Number of Readout Channels
196	10,976	384	6,912	60M		2,112	1,976	6.3M

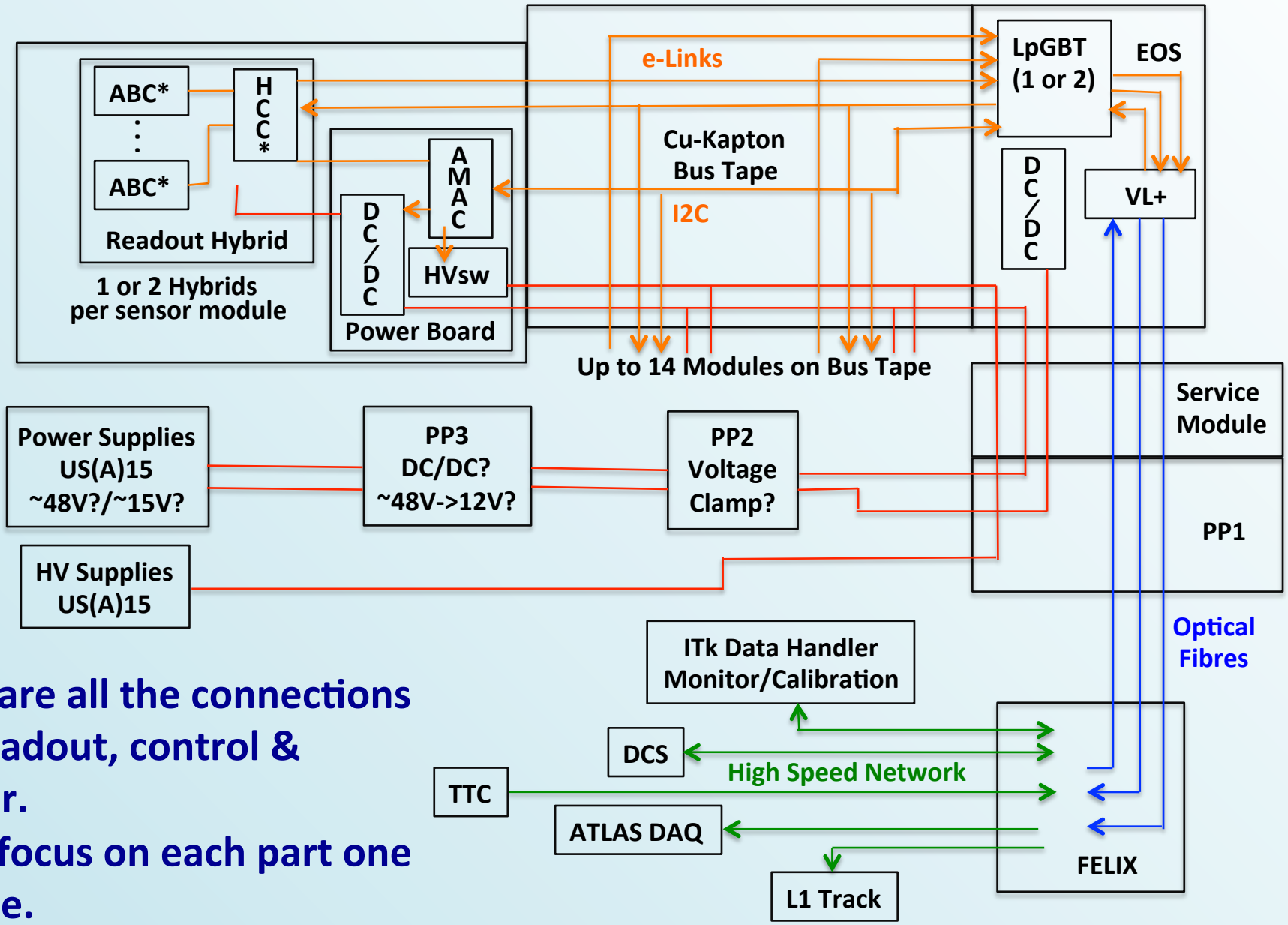
- **A factor of 4 more modules to build and a factor of 10 more channels to operate.**
- **Barrel Modules are built on sensors 9.8 cm x 9.8 cm in size.**
  - **The inner two barrels have 4 rows of 2.4 cm long strips serviced by 2 readout hybrids.**
  - **The outer two barrels have 2 rows of 4.8 cm long strips serviced by one hybrid.**
- **End-cap modules use trapezoidal shaped sensors of varying size to fit the wedged shape petal.**
  - **The longest End-cap strip is 5.4 cm long.**



Barrel Module with Short Strips

Stave or Petal Connections

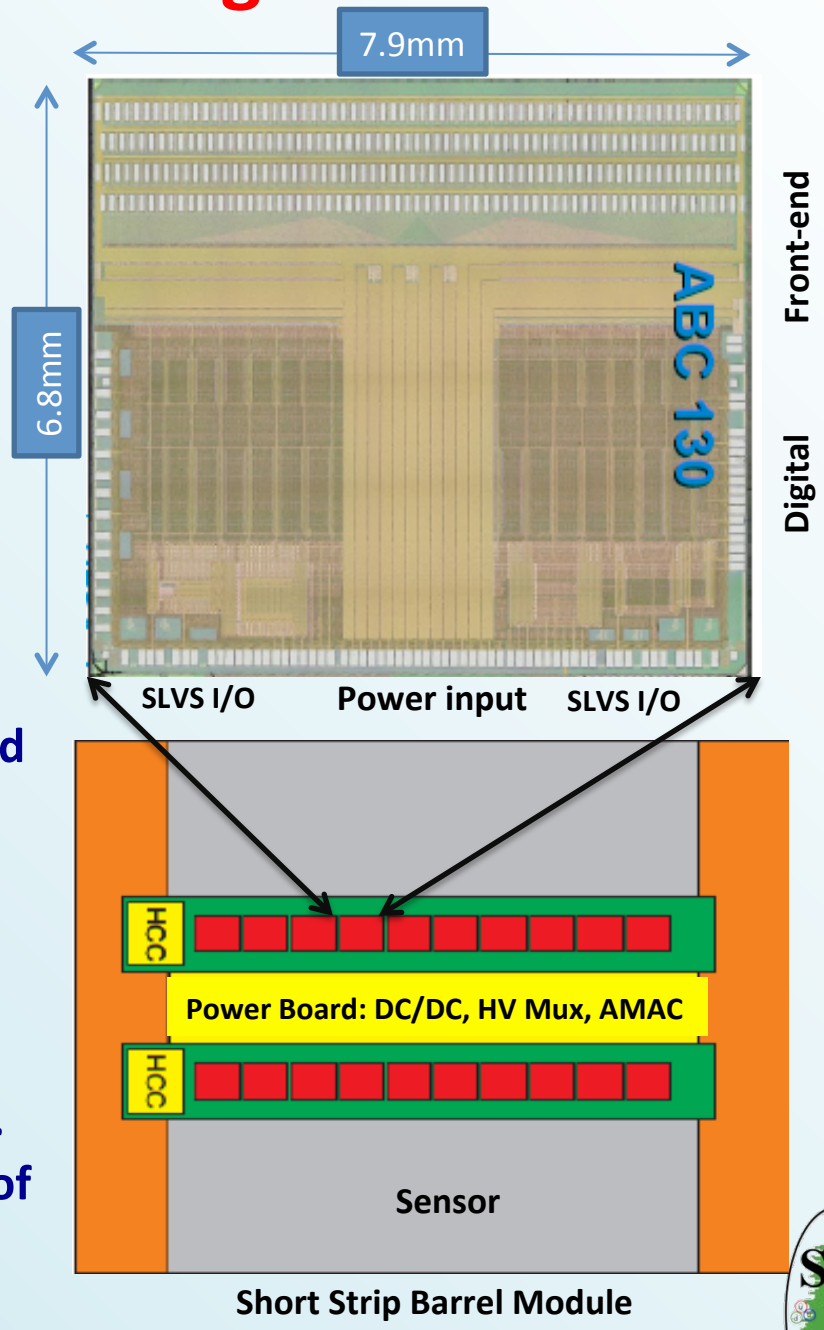
One of Two Sides



- Here are all the connections for readout, control & power.
- I will focus on each part one by one.

Module is the Basic Building Block

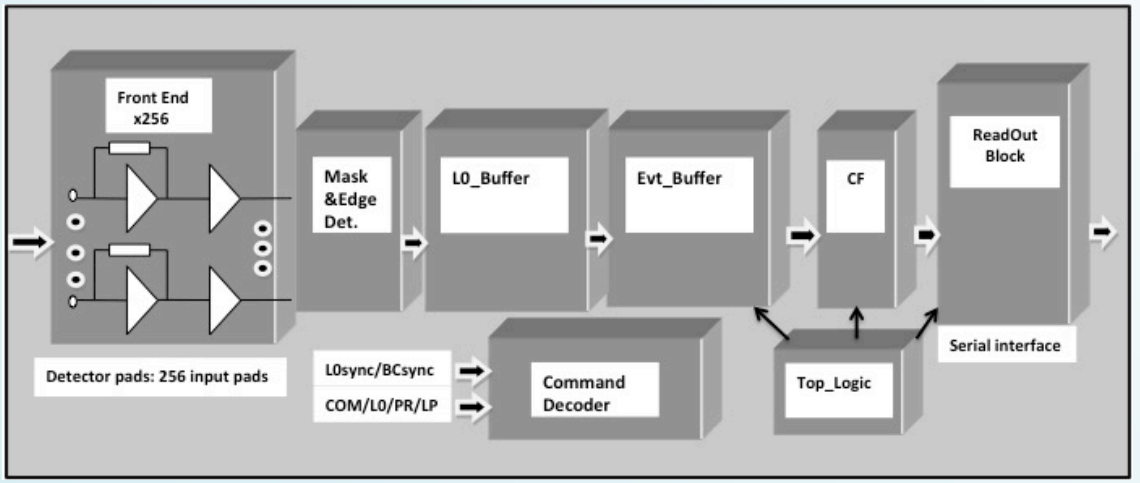
- This diagram depicts a short strip barrel module with a blow-up of an ABC130 front-end ASIC.
- Each of the two readout hybrids contains 10 ABCs and one HCC module controller ASIC.
- Sitting between the two readout hybrids is a power board.
- A long strip barrel module would have one hybrid and one power board.
- The power board includes a DC/DC converter to supply 1.5V, an HV switch for sensor bias and an AMAC (Autonomous Monitor & Control) ASIC.
- AMAC is powered independent of the DC/DC converter, monitors temperature, voltage, etc. and controls an HV switch and power to hybrid(s).
- Bidirectional communication with AMAC is provided via I2C bus from the SCA block of the LpGBT at end of stave or petal.
- LV to the hybrid and HV to the sensor can be controlled by the AMAC based upon correct temperature and operating voltages and currents.
- The End-cap modules differ in the size and shape of the sensor and in the number of ABC ASICs.



Short Strip Barrel Module

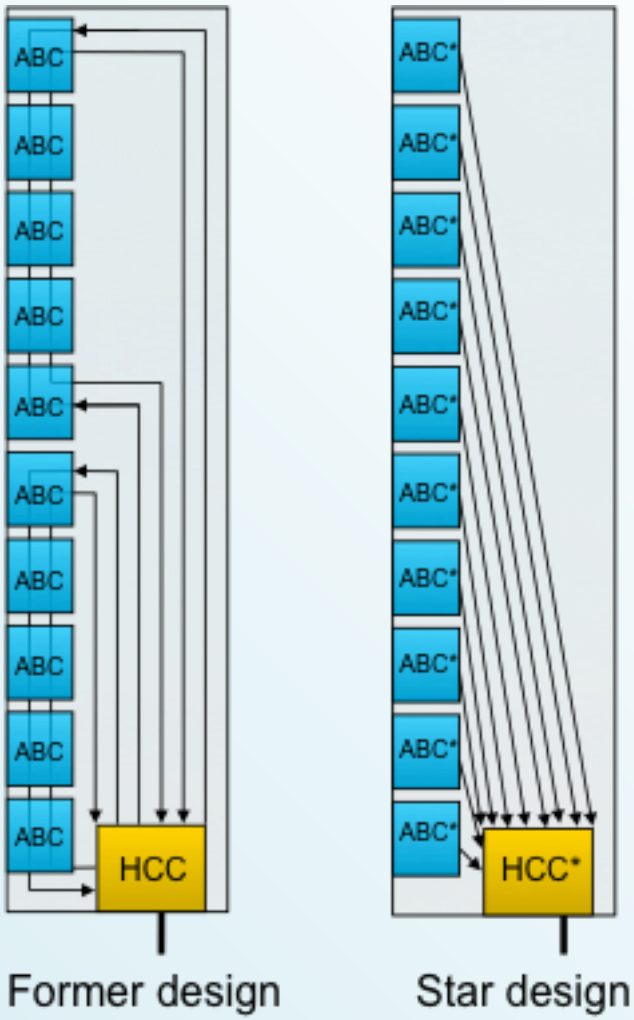
ABC* - Standard Binary Readout

- The ABC* front-end readout ASIC uses the same binary readout employed by the present ATLAS SCT tracker readout. (The ABC130 is an earlier prototype of the ABC* - See the next slide.)
- It includes amplifier, discriminator, pipeline for 256 channels and a buffer and a cluster algorithm to compress data for output.
- It is being designed to support more than one trigger mode:
  - L0 – Capture & readout everything.
  - L0/L1 – Capture data at L0, send requested data at L1.
  - L0/R3/L1– Capture data at L0, send requested ROI data with priority, send remaining requested data on L1.
- The HCC* manages these three trigger modes and sends the appropriate signals to the ABC* depending upon what mode is in operation.
- It is built on the GF130nm technology.

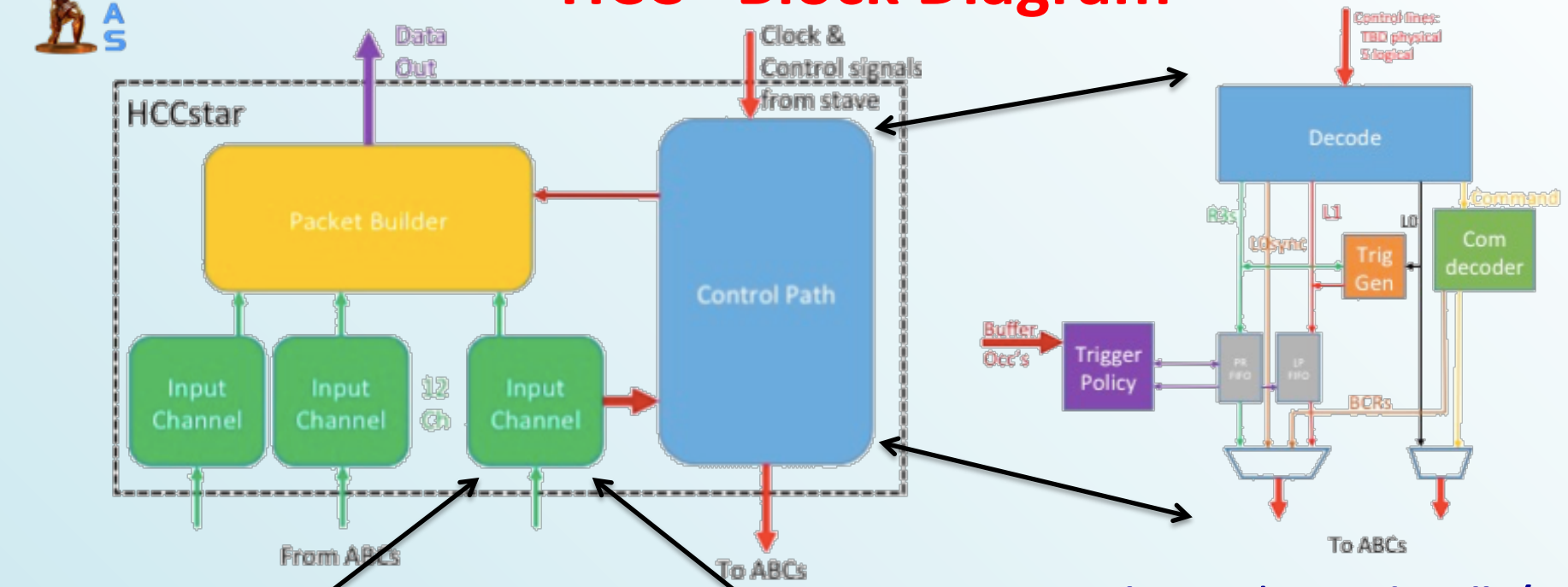


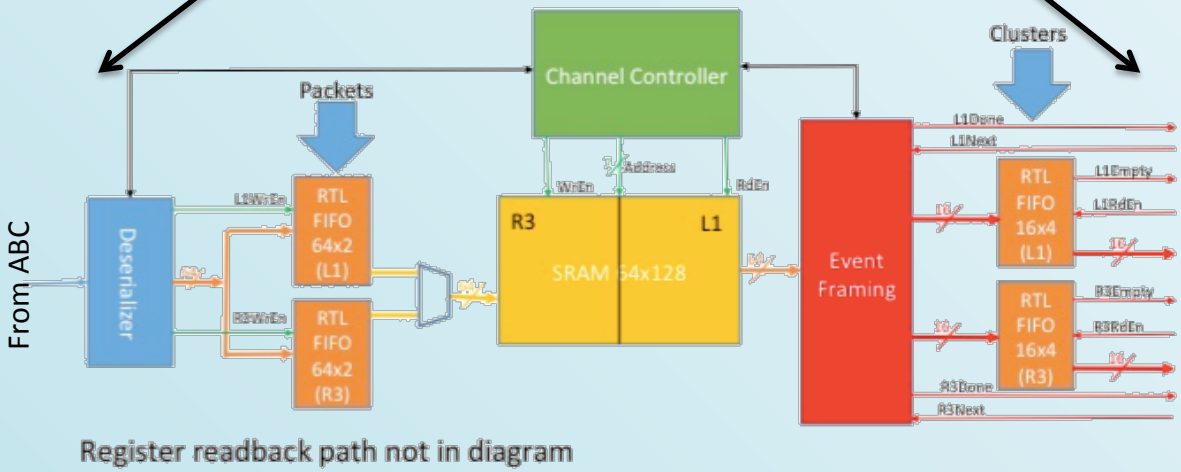
“Hold the Press” – New Design

- After the first ABC ASICs (named ABC130) were designed and fabricated on the IBM 130nm technology, the ATLAS L0 trigger rate requirement was increased to 1 MHz.
- We determined that the readout architecture could not support this 1 MHz rate and, therefore, a design change was required.
- The fundamental change was the interface from ABCs to the HCC as shown here.
- Serial transfer of data to the HCC was changed to direct communication from all ABCs to the HCC – hence the new ABC* and HCC*.
- The “star” configuration removed a bottleneck in data transfer to the HCC, which had considerable bandwidth still available.
- While both ASICs required changes, the HCC* required nearly a complete redesign as it must now essentially build events in parallel from fragments coming from all the ABC*s.



HCC* Block Diagram





Register readback path not in diagram

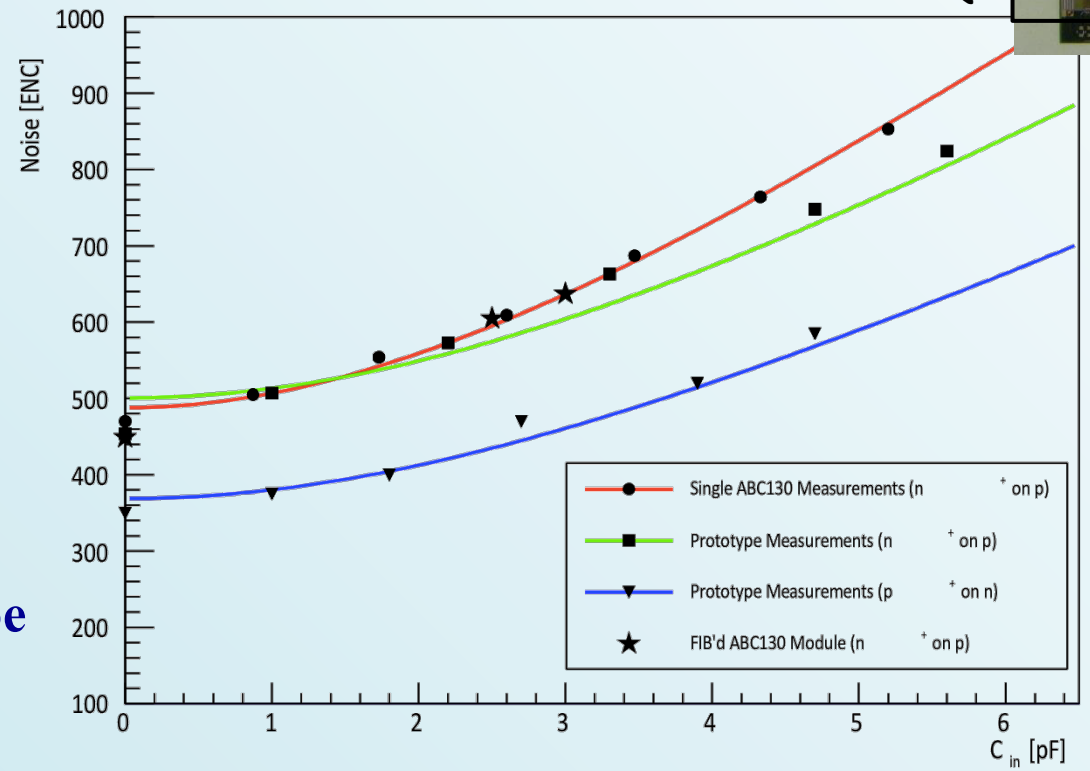
- The HCC* provides all I/O control for itself and the multi-ABC* readout system.
- Trigger types and commands for configuration, calibration, etc. are received and passed onto ABC*s as needed.
- Data from all ABC*s is grouped by event and then sent out.
- It is also built on the GF130 nm technology.

L0-Tag

- Events are typically identified by an event counter (L0ID or L1ID) and a bunch crossing counter (BC).
- In the present SCT, these counters are held in the ROD and the lower order bits of the counters are also kept in the on-detector ASICs.
- The RODs then cross check on-detector values included in each event data packet.
- These on-detector counters are prone to errors due to missed or extra triggers transmitted or to SEUs in the counters.
- Once a counter is in error, all following events appear as events out of order until the counter is reset.
- ITk will employ a new scheme – L0-Tag.
- Each L0 trigger will be accompanied by a tag; that tag will be sent back as part of the event data; off-detector electronics will check for matching tags.
- Errors will still occur for the same reasons, but each error should result in at most two lost or corrupted events rather than a long series of lost events.
- The off-detector electronics then will have responsibility to manage the counter identifiers.

Prototype Testing

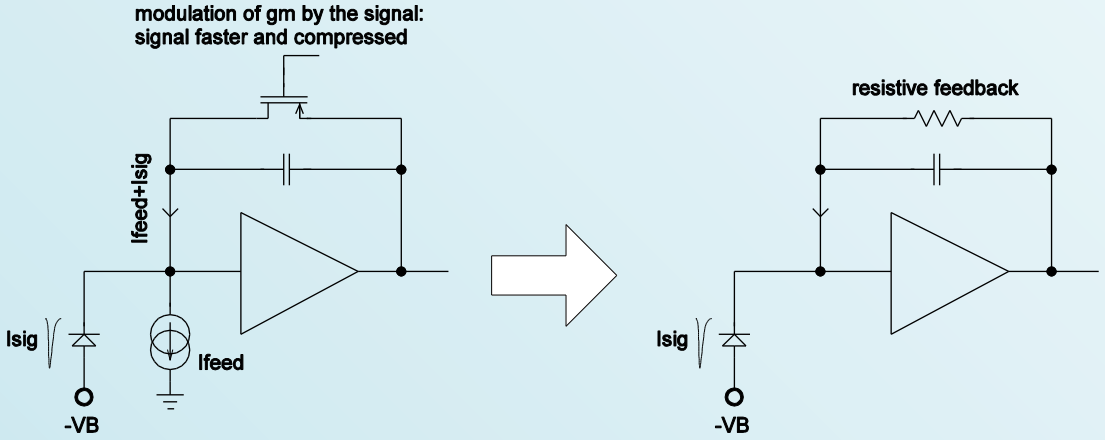
- The ABC* and HCC* are still in design.
- The ABC130 & HCC130 are being used for testing and to exercise module assembly and test.
- Noise performance of the prototype front-end chip and the full ABC130 front-end was compared.
- The prototype front-end allows comparison of performance of negative & positive signals.
- The first fab'd ABC130s had a digital error requiring a FIB repair.
- A second fab of ABC130s fixed the error.
- The "FIB'd ABC130" module ran all 10 ASICs but read out only 5 that were FIB'd.
- ENC for the FIB'd module agrees well with the prototype front-end chip and the single ABC130 chip.

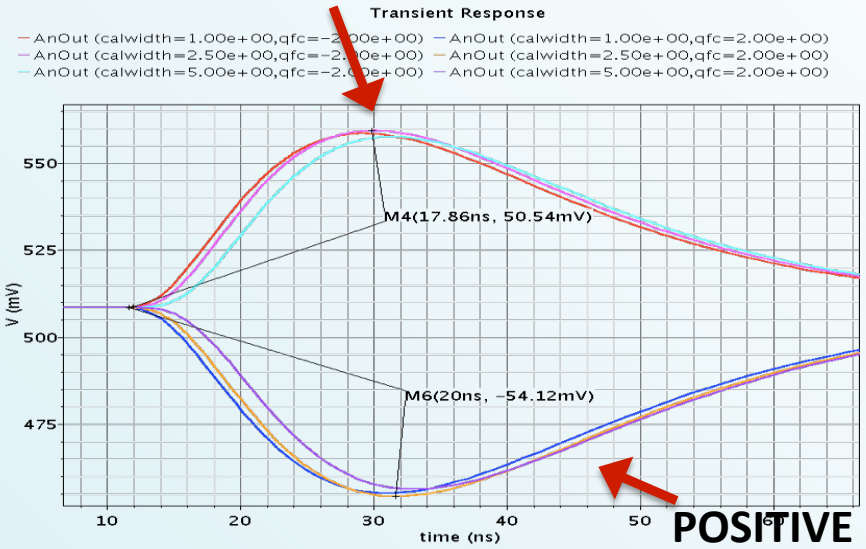


Performance Difference with Signal Polarity

- **Noise performance is worse after sensor polarity swap: effect of signal compression.**

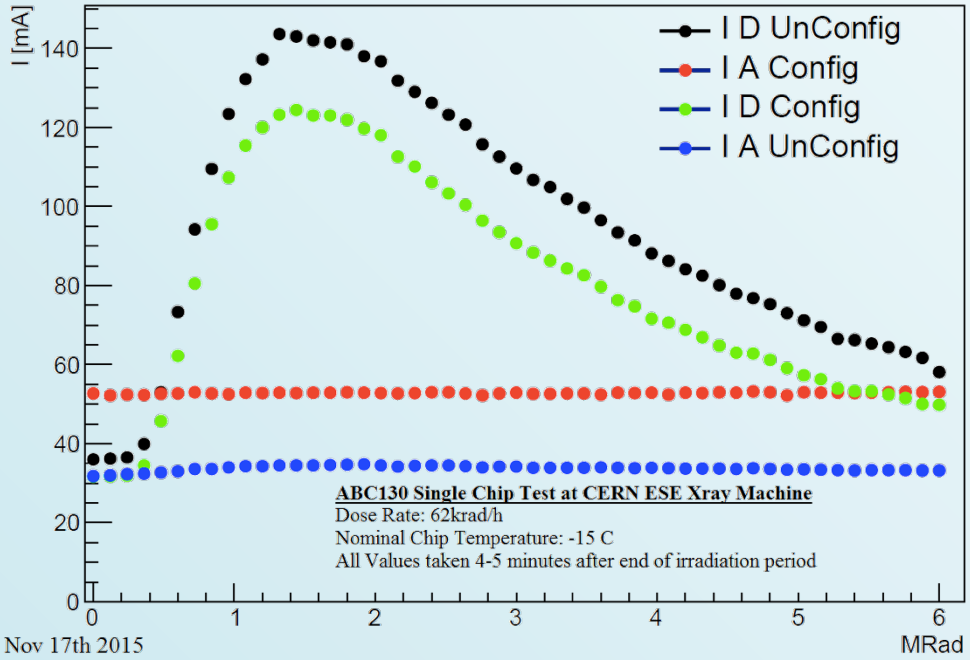
NEGATIVE (faster, lower in amplitude, more noisy)

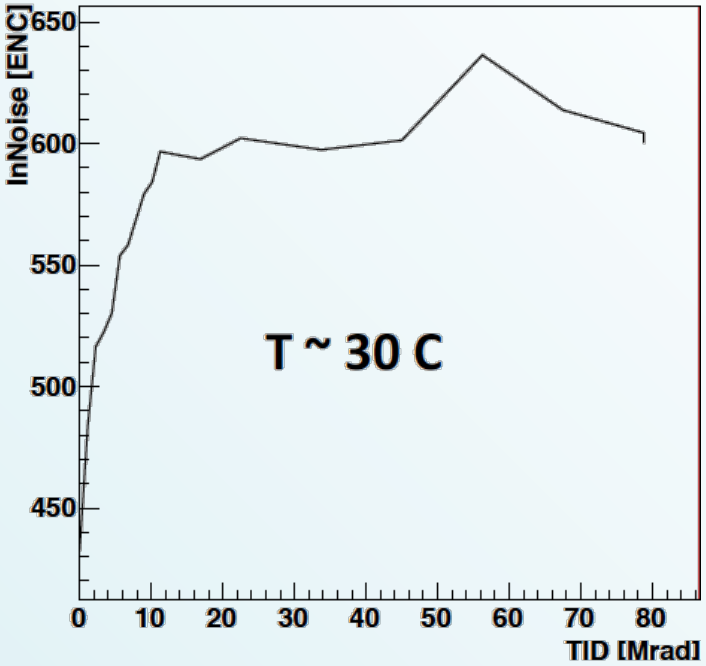




- **Effect of compression for negative signals (modulation of feedback transistor gm) simulated at the 8-10% level, in reality (prototype measurements) as high as 20%.**
- **This can be resolved by changing to a resistive feedback.**

Post Irradiation Testing

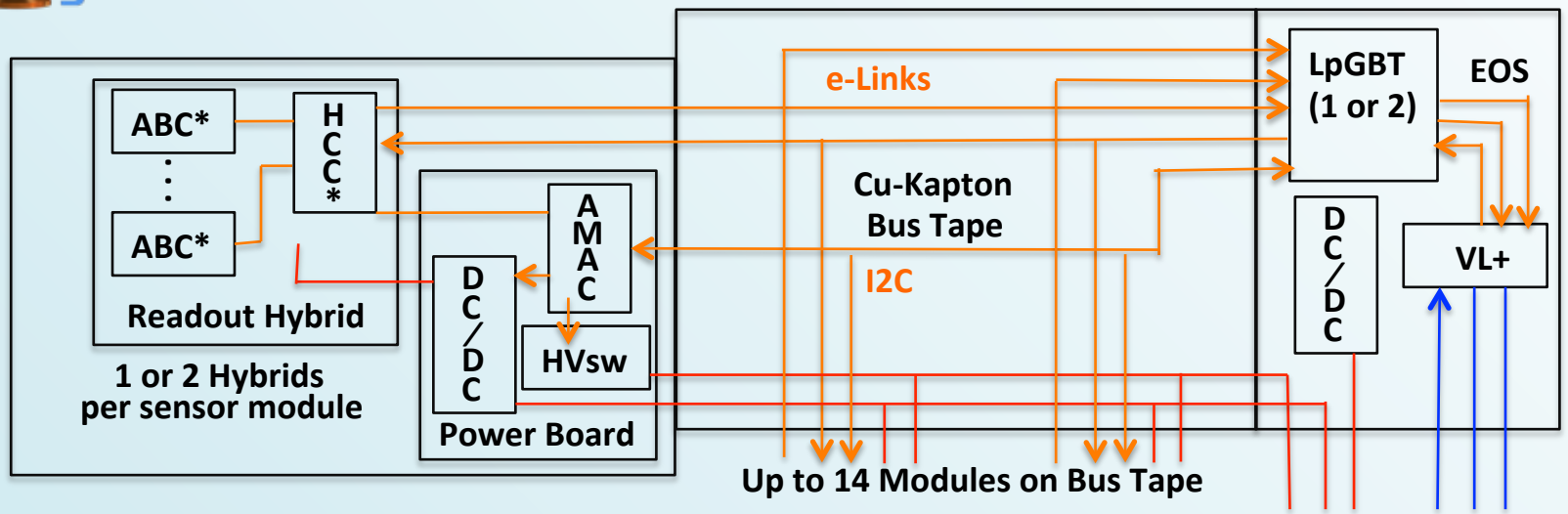




- Digital current rise with TID observed in ABC130.
- Known effect: see e.g. F. Faccio and G. Cervelli, IEEE Trans. 52.6 (2005) 2413.
- Digital current (D) peaks, then recovers. Function of dose rate and temperature. No effect in analogue current (A). ABC tested configured & unconfigured.
- Tests underway at expected operating temperature and dose rate at HL-LHC.

- Unexpected noise increase observed after ionizing radiation:
  - Possible reason: 1/f noise.
  - Simulated pre-rad contribution of the 1/f noise to ENC was at the level of 3%.
  - Radiation effects on 1/f noise under study.
- Some reports for similar technology (130nm ST) show substantial increase of 1/f noise for regular NMOS devices and no change for the enclosed structures (influence of STI isolation?)
- For new ABC front-end, all critical (for noise) NMOS devices will be in enclosed geometry.

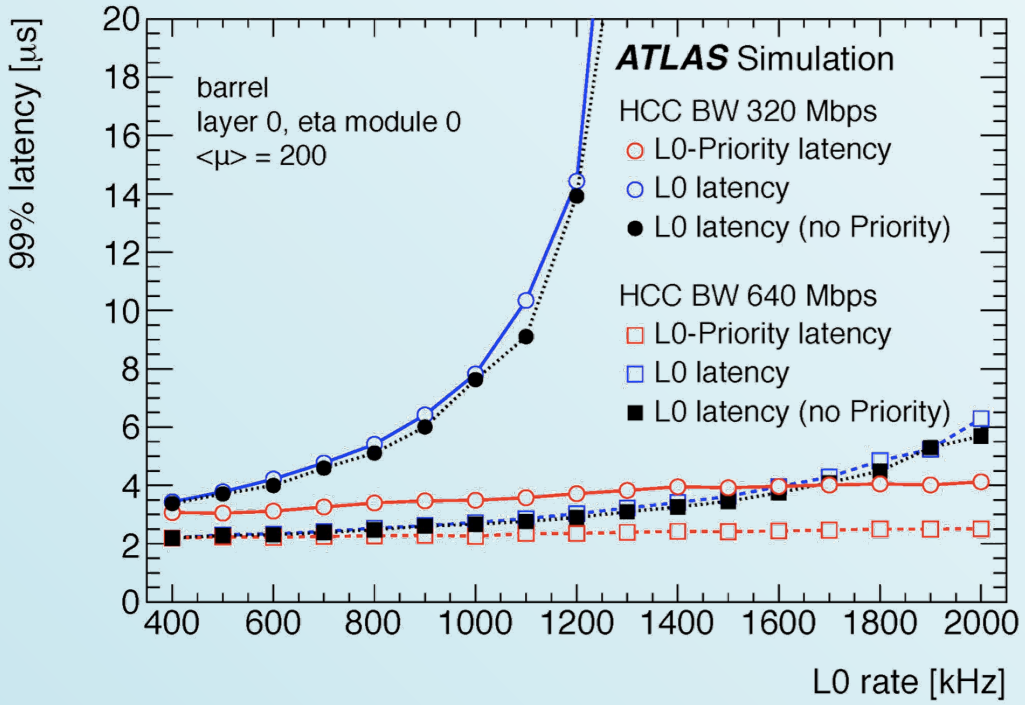
Cu-Kapton Bus Tape

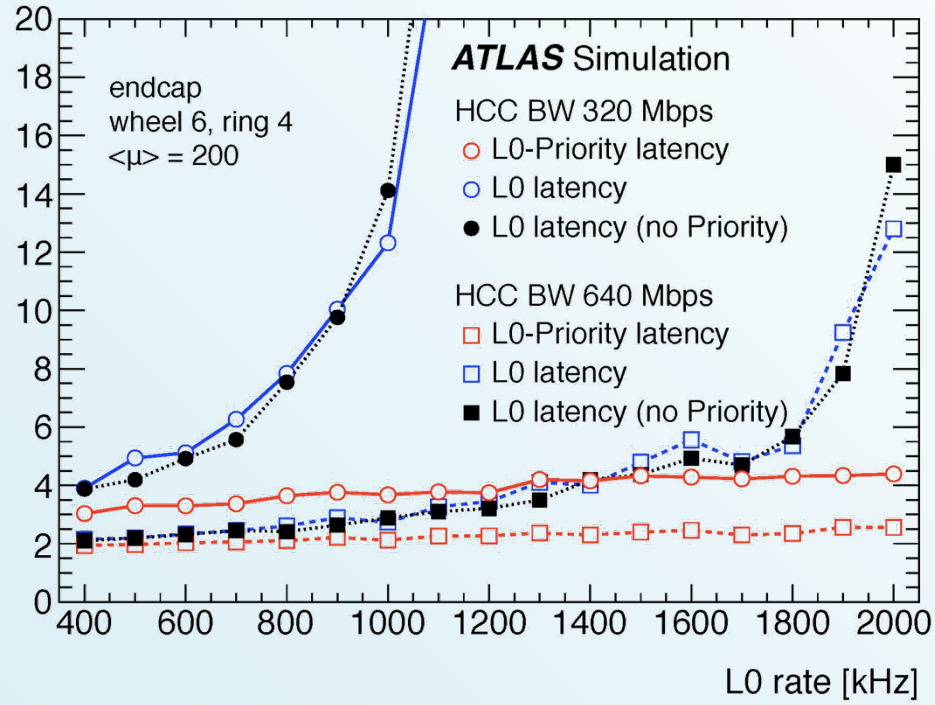


- A Cu-Kapton bus tape provides all the electrical connections between the modules and the EOS card on both Staves & Petals.
- Triggers, commands and clocks are carried from LpGBT to hybrid HCC*s via 3 multi-drop lines, two e-links at 160 Mbps and a clock at 40 MHz.
- Data is carried from HCC*s to LpGBTs via point-to-point e-links at 640 Mbps.
- Each half-stave has 14 modules on the top and on the bottom side.
- Petals have 9 modules on each side of varying size to fit its tapered shape.

Managing the 1 MHz L0 Rate

- The change to the "star" hybrid architecture was not the only concern with the increase to 1 MHz L0 rate.
- We need to meet the latency requirement, especially to feed data to L1-Track.
- Here are simulations of our readout time at two different output bandwidths.

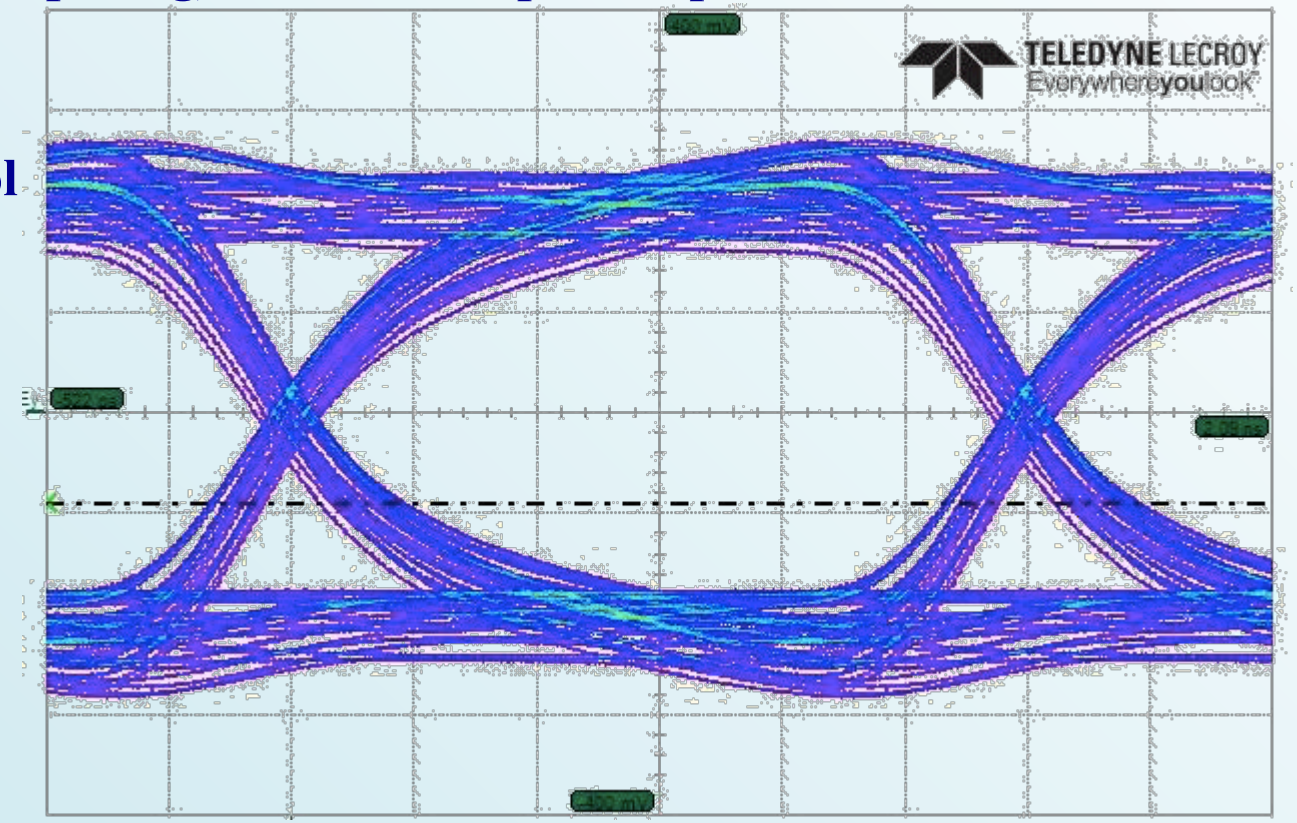




The simulated latency for all data from 99% of all requests to arrive at the end of stave/petal for the highest occupancy Barrel and End-Cap layer module of the ITK as a function of the L0 rate for the scenario where all L0 events are read out from the detector. Detector occupancies commensurate with a mean occupancy of 200 separate pileup interactions per bunch crossing have been used.

Electrical Transmission on Cu-Kapton Tape

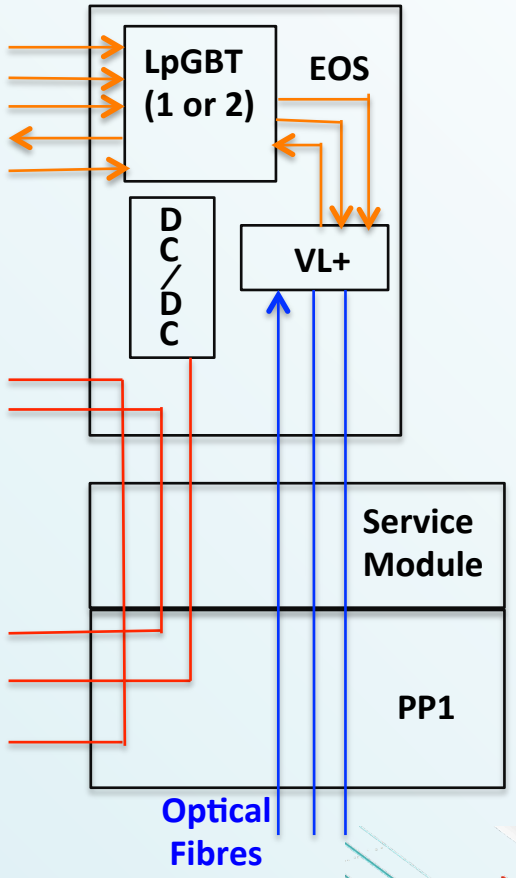
- 640 Mbps is faster than we originally intended to run the bus tape e-links.
- Preliminary data indicates that 640 is manageable.
- Parametric measurements of "S" parameters with various shield and conductor configurations (e.g. relative spacing) has led to improved performance.
- More extensive testing of tapes with improved shield & better impedance control are being prepared.
- These tests will include parametric measurements of "S" parameters, signal attenuation, and bit-error-rate testing of transmission using a balanced code and pre-emphasis.

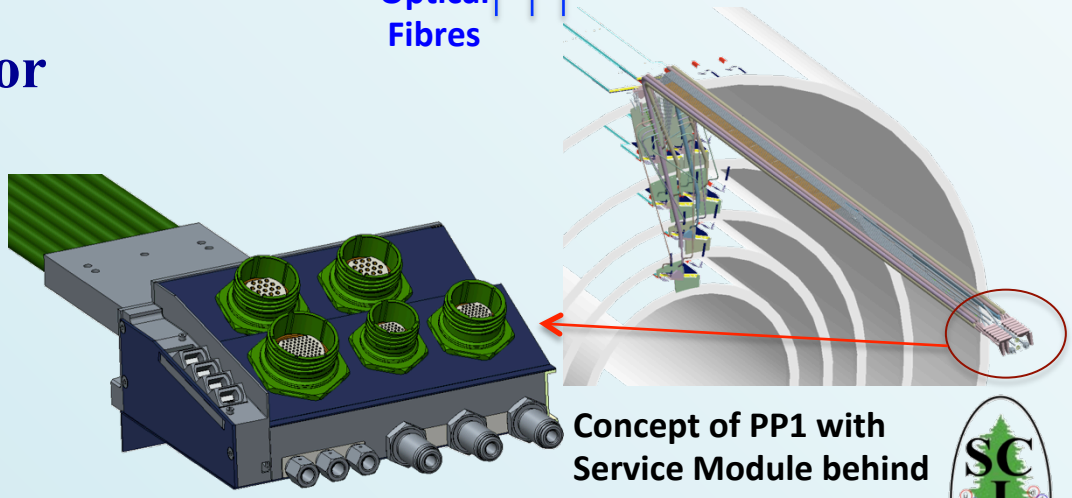


640 Mbps Eye Diagram Simulated Using "S" Parameters Measured on the Bus Tape with Improved Shielding

End of Structure (EOS card) & PP1

- Each side of a petal and each side of a half-stave has an EOS card.
- Petals with 14 HCC*s (Some modules have 2 hybrids and 2 HCC*s.) and outer barrel half-staves with 14 HCC*s require 1 LpGBT – Inner barrel half-staves with 28 HCC*s require 2 LpGBTs, each with a complementary number of VL+s.
- A DC/DC converter steps down the voltage for the EOS ASICs.
- PP1 provides the connection point for harnesses from the outside and the Service Module will provide an orderly method to tie the PP1 connections to the EOS cards.

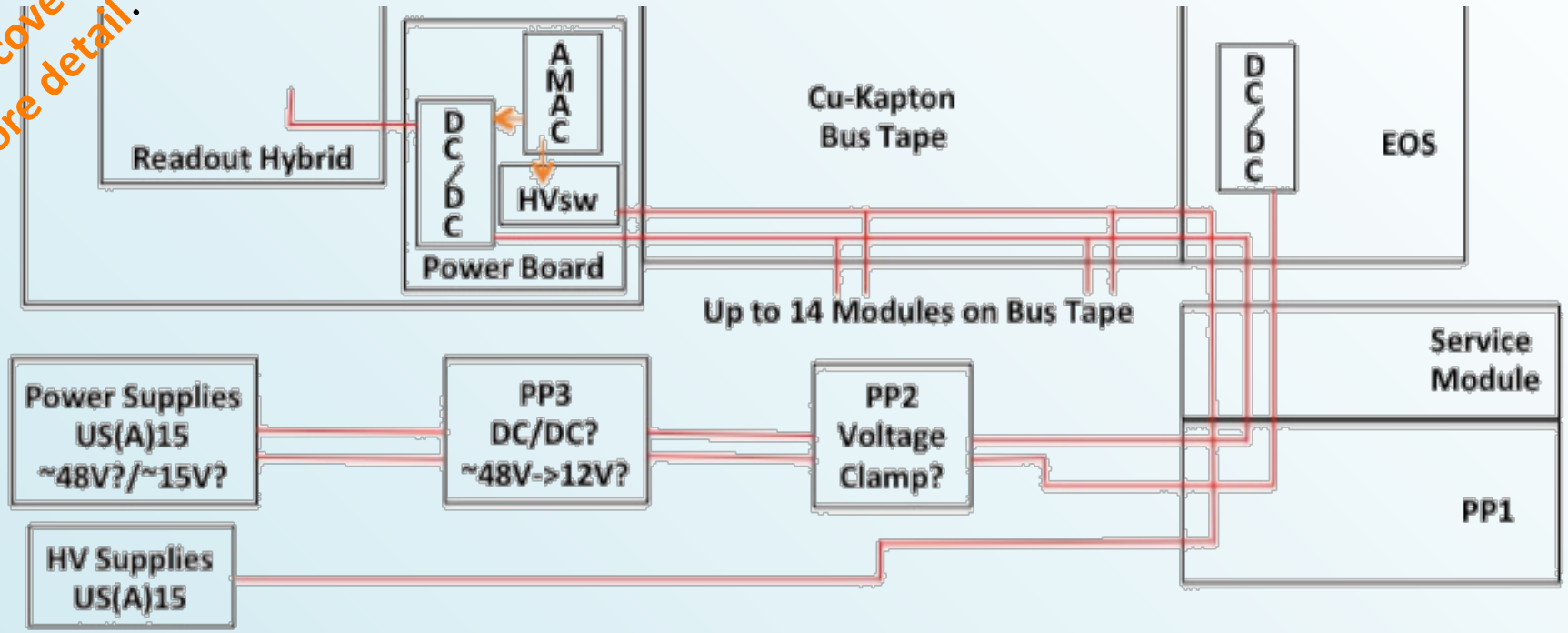




Concept of PP1 with Service Module behind

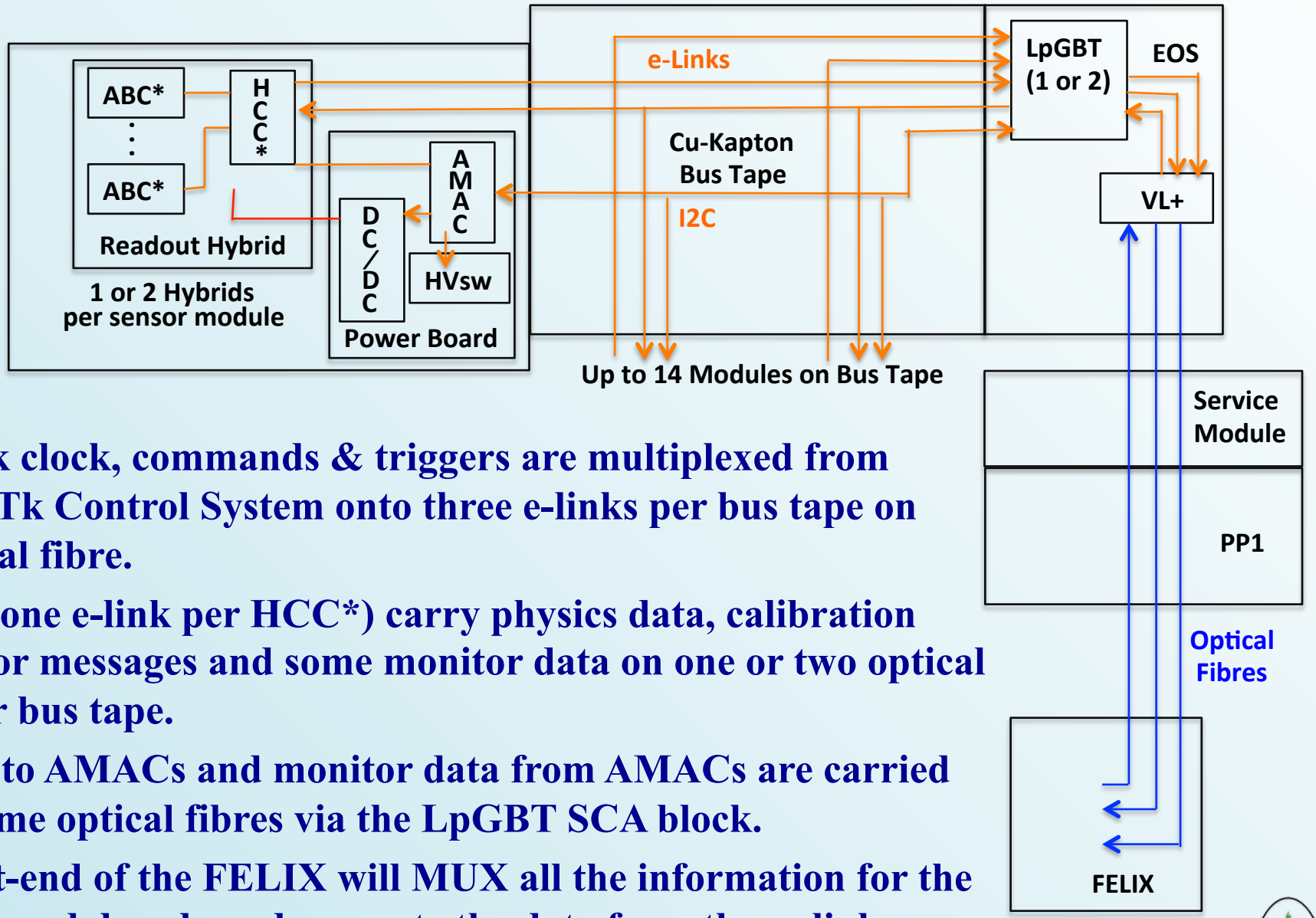
Powering Options

Peter Phillips covered this in much more detail.



- LV and HV are to be supplied from the service caverns.
- Two LV options are being considered:
  - A) A step down at ~PP3 to 10V-12V to be supplied to the DC/DC converters at EOS and modules.
  - B) Source at 15V with ~3V drop along full length of cable run.
  - Amount of copper needs to be considered.
  - A voltage clamp at PP2 may be required to prevent over voltage at DC/DC converters should current draw drop by a large amount.
- HV to be provided per stave/petal with HV switches to disable bad modules.

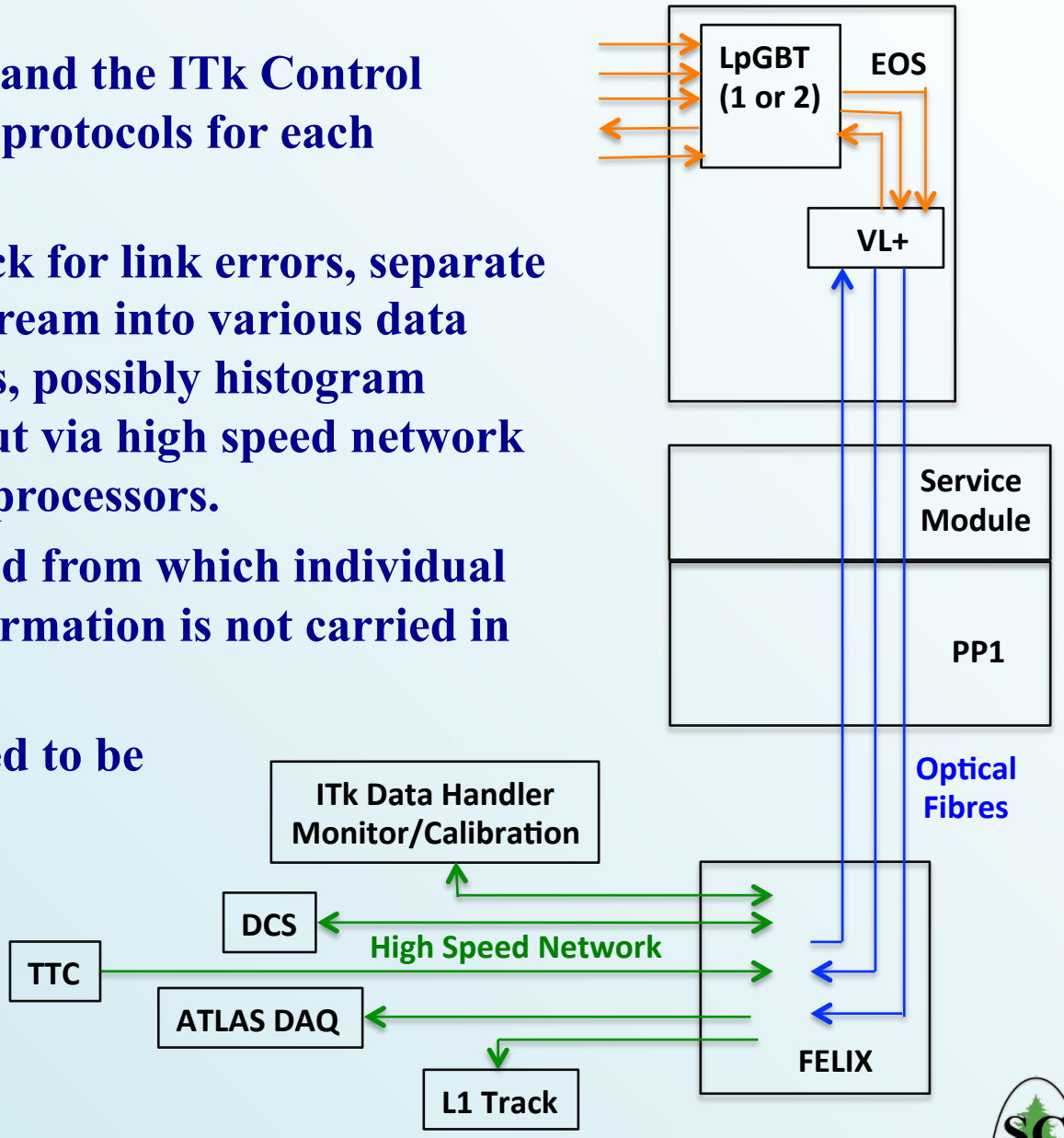
Optical Links between Detector & FELIX



- Downlink clock, commands & triggers are multiplexed from TTC & ITk Control System onto three e-links per bus tape on one optical fibre.
- Uplinks (one e-link per HCC*) carry physics data, calibration data, error messages and some monitor data on one or two optical fibres per bus tape.
- Controls to AMACs and monitor data from AMACs are carried on the same optical fibres via the LpGBT SCA block.
- The front-end of the FELIX will MUX all the information for the downlink and decode and separate the data from the uplinks.

Off-detector Control & Processing

- FELIX will take input from TTC and the ITk Control system to build ITk Strip specific protocols for each downlink.
- FELIX will take uplink data, check for link errors, separate data from the continuous input stream into various data types, decode ITk specific headers, possibly histogram certain data and then ship data out via high speed network link to the appropriate back-end processors.
- Output data will need to be labeled from which individual uplink (e-link) it came as this information is not carried in the original data packets.
- All back-end processors are planed to be processor farms.



Environmental Monitoring

- **The Pixel and Strip detectors have their own tie to ATLAS DCS to provide on-detector monitors and control:**
  - **Pixels will have a wired system, likely tying to an industrial bus (CANBus?).**
  - **Strips will make use of the SCA block on the LpGBTs, communicating through the opto-links.**
- **In addition ITk will employ system wide environmental monitoring.**
- **This system will monitor temperature and humidity inside the ITk with an independent channel into ATLAS DCS.**
- **It will always be available even when DAQ is not operating but certainly whenever any power is applied to the ITK.**

Interlock System

- An interlock will also exist to guarantee the safety of the detector and in some cases personnel safety.
- Examples include:
  - A signal from the cooling system that it is operational.
    - This may be divided into sectors of the detector allowing one to be on while others are not.
  - Temperature sensors independent of the Pixel and Strip monitoring will assure that the cooling system is operational before power to the detector will be enabled.
    - Again, this may be divided into sectors.
  - Power to the laser drivers will not be enabled if cabinets with optical receivers are open.
  - Some of the Pixel and Strip monitors may also be fed to the Interlock System via DCS.
- The hardware matrix for this system is yet to be designed.

Power Up Sequence

- **Powering on the detector must follow a strict set of steps in order assure that it is first safe to apply power to each part of the detector.**
- **The steps now envisioned are:**
  - **All interlocks must be cleared, at least for the sector to be powered on.**
  - **Power to the EOS cards applied and communication with the EOS LpGBT systems initiated and validated as operationally valid.**
  - **Communication with each AMAC ASIC on each module is established and its local monitors (e.g. hybrid temperature) are validated.**
  - **HV to the stave or petal applied. (HV Switches on modules are still off.)**
  - **HV Switches may now be closed and sensor leakage currents measured.**
  - **LV to the stave or petal bus applied. (DC/DC converters on modules still disabled.)**
  - **Readout hybrids may now be powered via the AMAC chips – hybrid voltages and currents validated.**
  - **Configuration of all readout hybrid ASICs is loaded.**
- **At this point, the detector, or sector of the detector, should be operational. Calibration may be the next operational step.**

Summary

- The overall readout and control architecture is well defined, but ...
  - The increased L0 trigger rate to 1 MHz caused major revisions in the last year.
  - The increased digital currents post-rad and the larger noise post-rad requires more investigation, now ongoing.
  - Off-detector electronics has yet to see the start of detailed design but requirements have been well documented.
    - This work presently is focused on module and stave/petal testing.
- We have the previous prototype ASICs for advancing module assembly and testing procedures to prepare for construction.
- There is still much work to complete the revised on-detector ASICs.
- As noted in the previous talk, there are still options to consider in the powering chain.
- Common ITk Interlock System still requires detailed design.