

CMS GEM Electronics

Electronics Systems for GEMs in CMS

System 2, for prototypes

V2 System

VFAT2 , GEBv2 , OHv2

Slice Test

System 3, for GE11

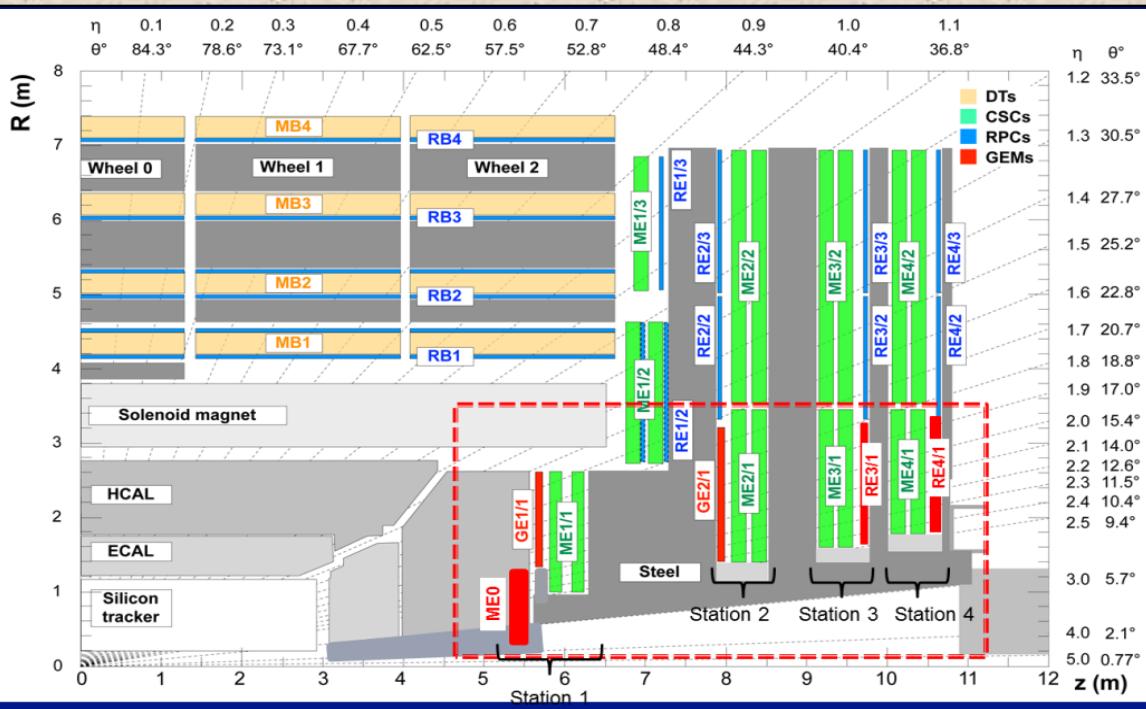
V3 system

GEBv3 , OHv3

VFAT3 design status

GE11 Schedule

The CMS Muon System

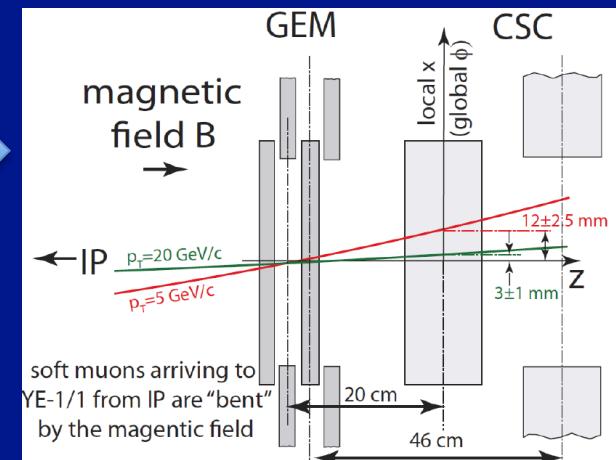


New Muon Systems :

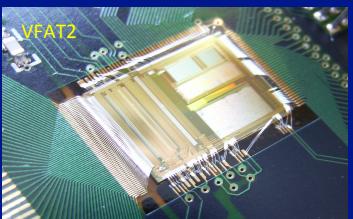
GE1/1 & GE2/1 GEM detectors

GE1/1 (LS2) and GE2/1 (LS3) to add redundancy and provide separation of high and low pT Muons needed for trigger efficiency at high particle rate.

MEO : Extending eta coverage up to eta=3 or more with 6 layers of GEM detectors



CMS GEM Electronics System



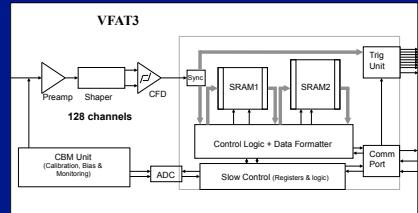
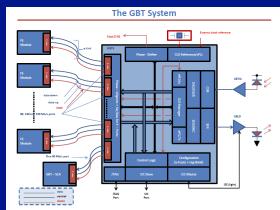
GEM Electronic Board
(GEB)



Opto-Hybrid (OH)

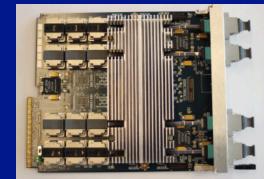


GBT

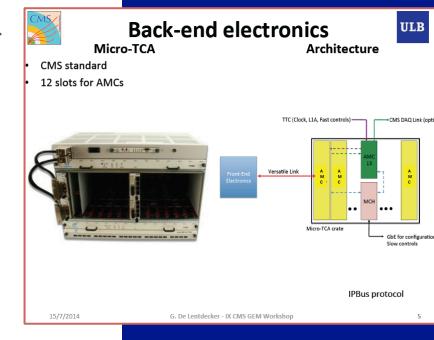
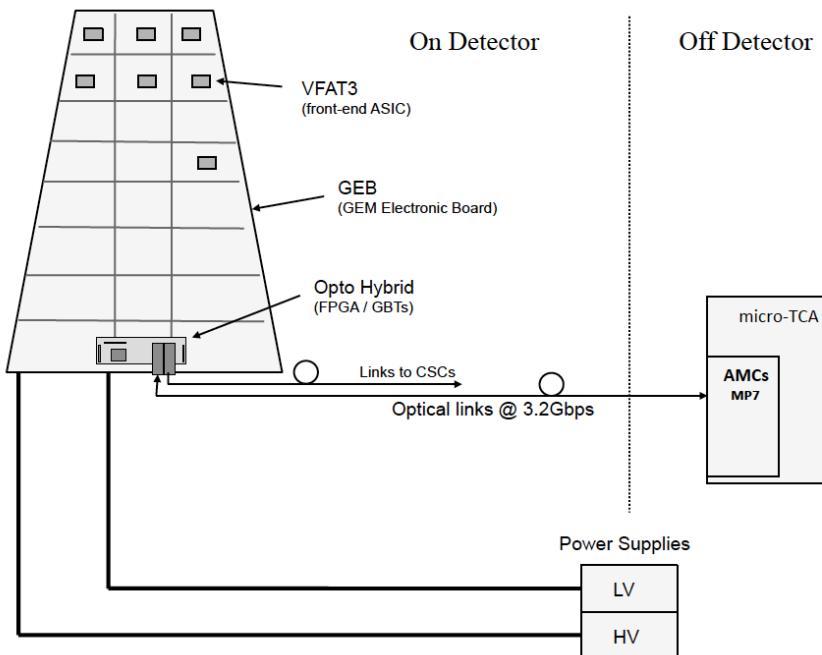


VFAT3 front-end ASIC development

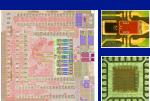
MP7/FC7



μ TCA
AMC13, MCH



Versatile Link



Use of many common developments such as GBT,
Versatile Link, μ TCA backend

Installation in CMS in 2019-20

- LS2 : GE1/1 Installation
- LS3: GE2/1 and MEO

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V3 system

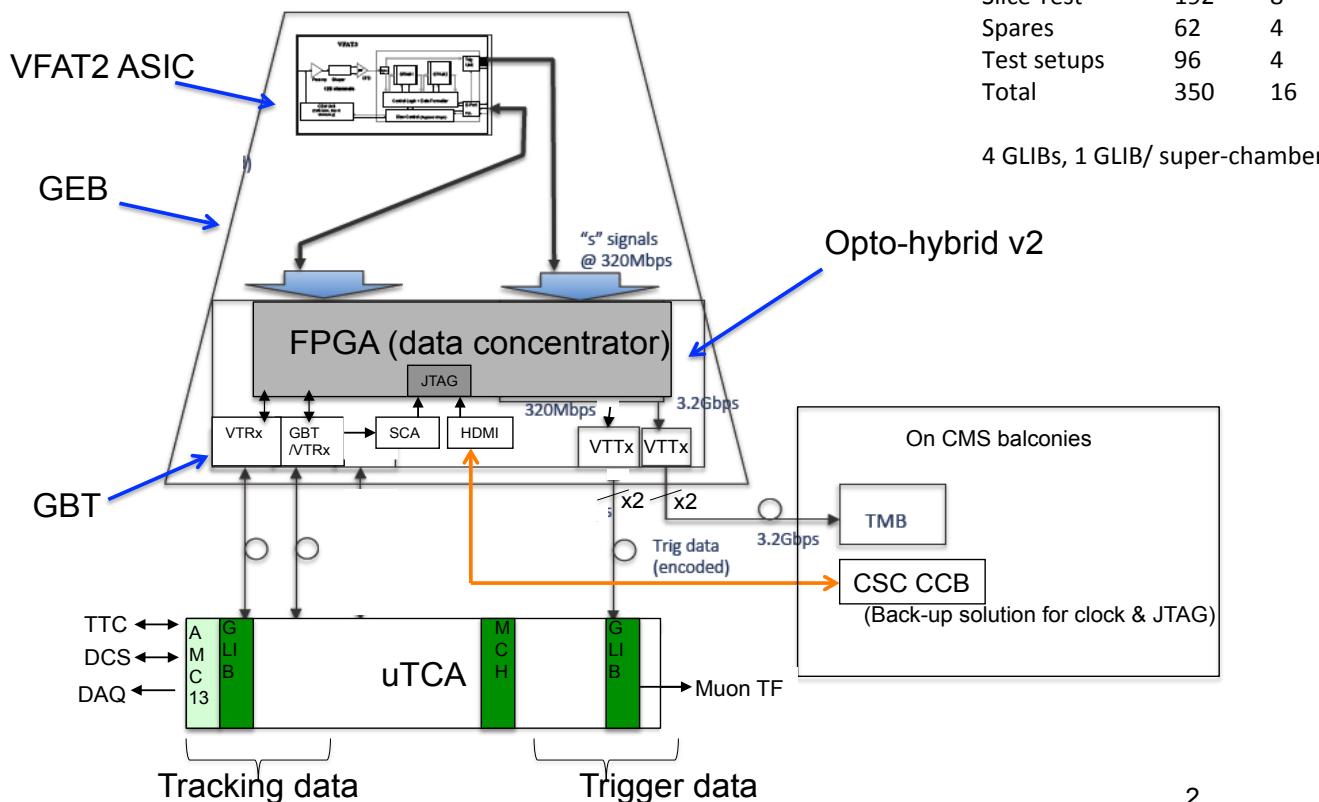
GEBv3 , OHv3

VFAT3 design status

GE11 Schedule

System v2

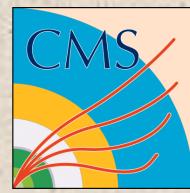
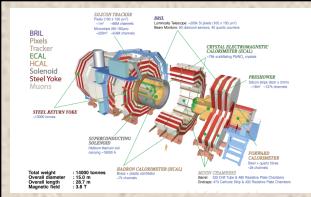
Slice Test system



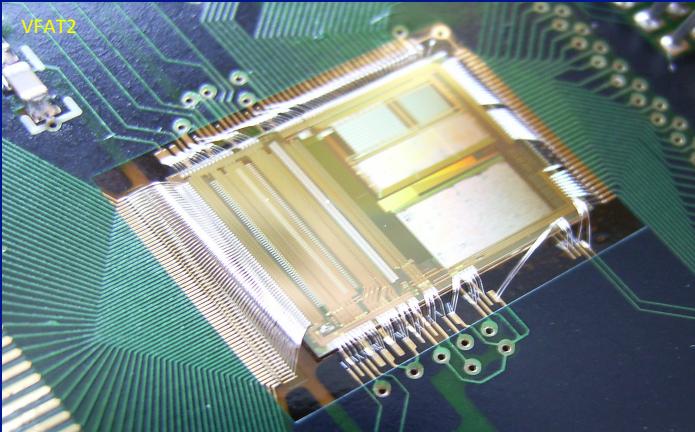
4 super-chambers (10 degrees each)
8 chambers (2/super chamber)
24 VFAT2 / chamber
1 OptoHybridv2 / chamber
1GBT, 1SCA, 2VTRx, 2VTTx / chamber

	VFAT2	GBT	SCA	VTRx	VTTx
Slice Test	192	8	8	16	16
Spares	62	4	4	8	8
Test setups	96	4	4	8	8
Total	350	16	16	32	32

4 GLIBs, 1 GLIB/ super-chamber



VFAT2 & v2 hybrids



VFAT2 hybrids: Production of 350 VFAT2 V2B hybrids

Currently undergoing production, component mounting, chip bonding and production testing.

Prototyping the v2 system



GE1/1 inside the cooling box



CERN 904

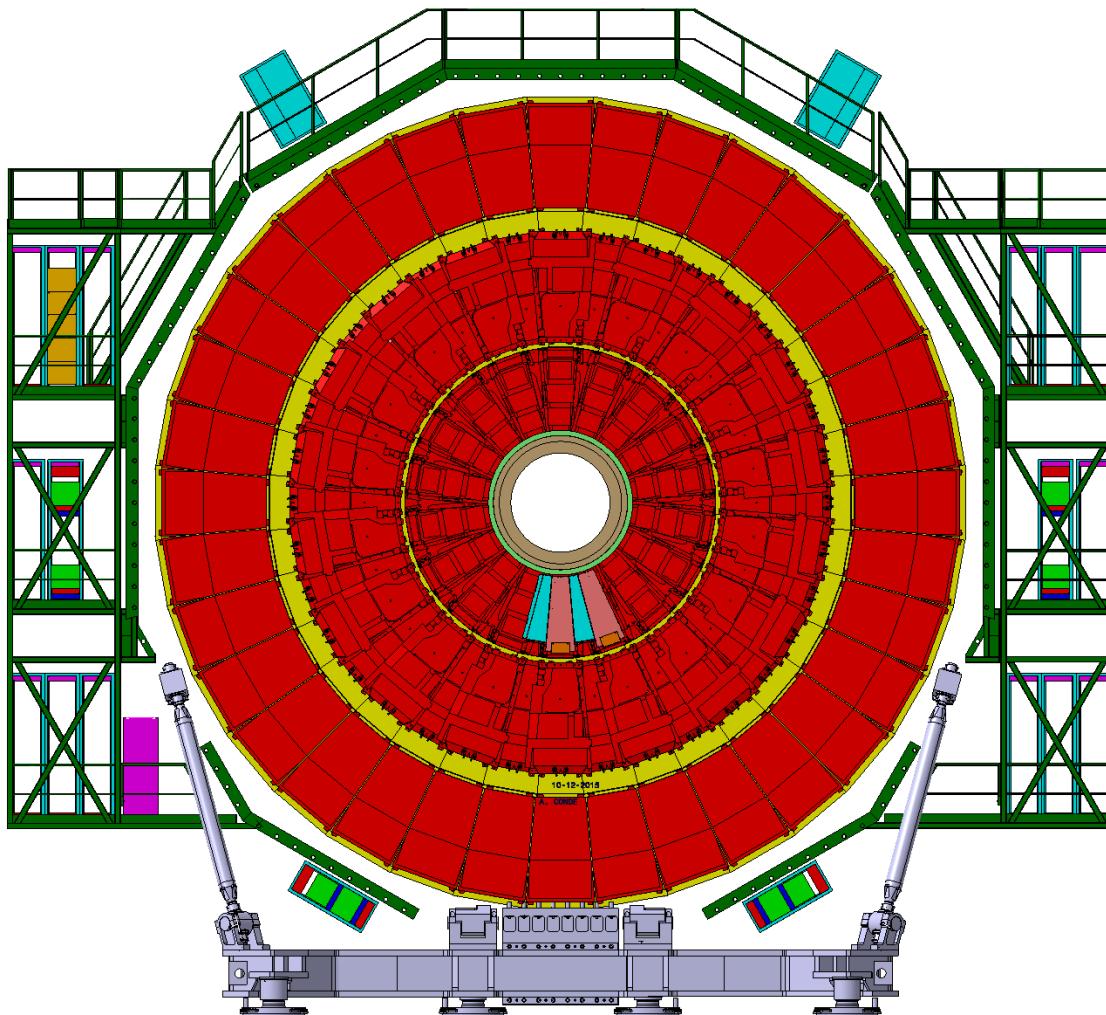
Set-up used for
firmware and on-
line software
development.

- CERN
- Lappeeranta University of Technology
- Peking University
- Rice University,
- Texas A&M
- ULB Brussels
- UCLA
- UCDavis
- Wayne State University

ME1/1

GE1/1 Setup for VFAT
and GEB tests.

Slice Test



CMS GEM Electronics

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VFAT2 , GEBv2 , OHv2

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GEBv3 , OHv3

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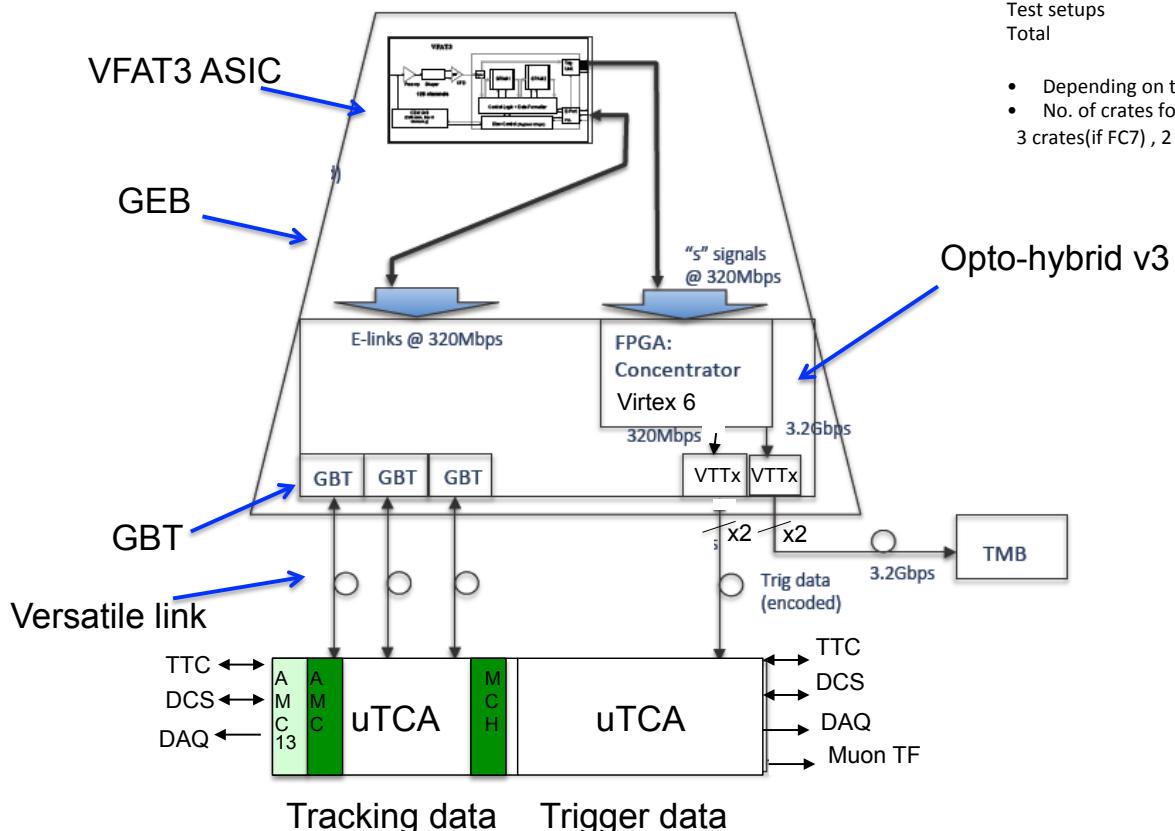
System v3

GE1/1 system

72 super-chambers (10 degrees each), 2 end caps
 144 chambers (2/super chamber)
 24 VFAT3 / chamber
 1 OptoHybridv2 / chamber
 3 GBT, 1SCA, 3VTRx, 2VTTx / chamber

	VFAT3	GBT	SCA	VTRx	VTTx	FC7
GE11	3456	432	144	432	288	36 /76*
Spares	400	50	20	50	30	4/8*
Test setups	480	60	20	60	40	10
Total	4336	542	184	542	358	50/90*

- Depending on the no. of GBT links/FC7(CTP7orMP7)
- No. of crates for the full system could be reduced to:
 3 crates(if FC7) , 2 crates(if CTP7) , 1 crate(if MP7)

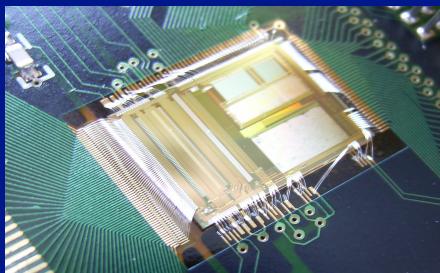


Front-end ASIC Development

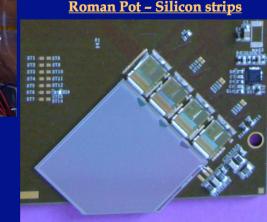
VFAT2 to VFAT3

VFAT2
Initially design for TOTEM

Current front-end readout
for CMS GEM R&D



TOTEM's 3 different detector technologies



T2
GEMs

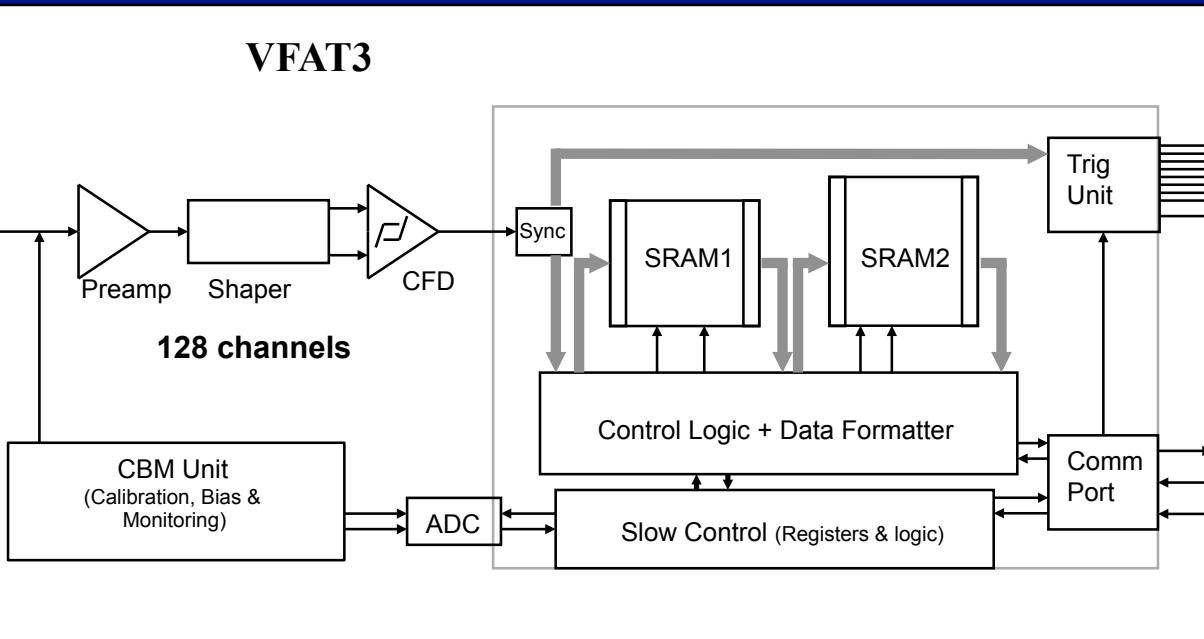
VFAT2 is used with all 3
detector technologies

Roman Pot - Silicon strips

VFAT3 – New VFAT ASIC for GE1/1

VFAT3

128 channels



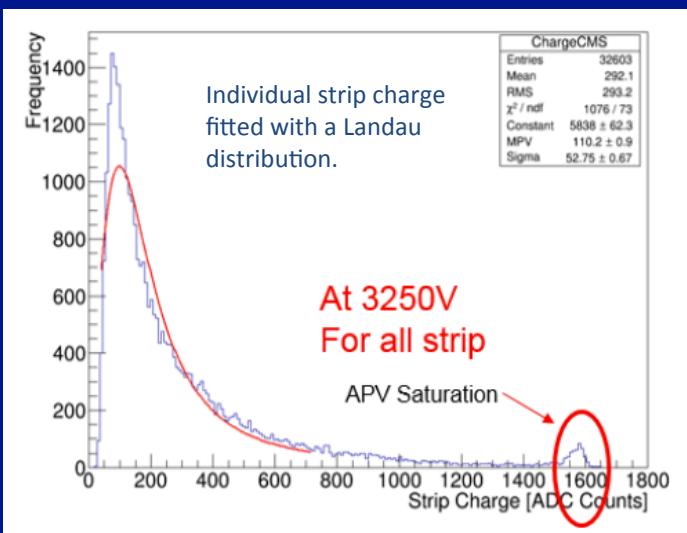
VFAT3

Trigger path : 8 sLVDS pairs @ 320Mbps
64b/bx (128b/bx DDR)
Fast OR : Each pair of channels, lossless
SPZS: Full granularity, up to 6 partitions / bx
DDR : Full granularity, lossless.

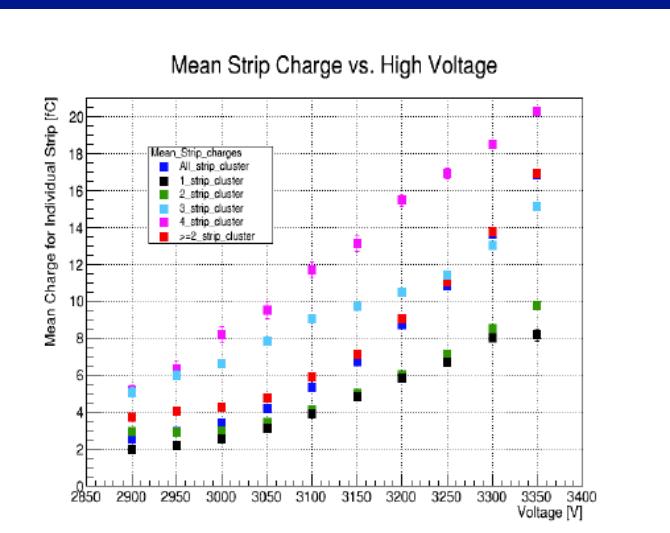
Data path
Full granularity after LV1 + time tag
LV1 latency extended to 25us
LV1 rate extended to 1MHz

Communication interface to GBT
Comm-Port allows bi-directional communication of control commands, CMB (calibration, bias and monitoring) and data readout through a single port to the GBT.

Dynamic range spec : Input charge & dynamic range



Charge per strip (all strips):
 MPV (nominal) = 110 ~ 4 fC
 Mean (nominal) = 292 ~ 10 fC
 99% (nominal) ~ 65 fC
 Mean (max HV) ~ 17 fC
 99% (max HV) ~ 75 fC



Charge Distribution Study of a Large-Area GEM Detector
 for the Readout Electronics of Future Upgrade of the
 CMS Muon Endcap

Vallary Bhupakar*, Marcus Heßmann, Aiwu Zhang
 Department of Physics and Space Science
 Florida Institute of Technology
 August 11, 2015

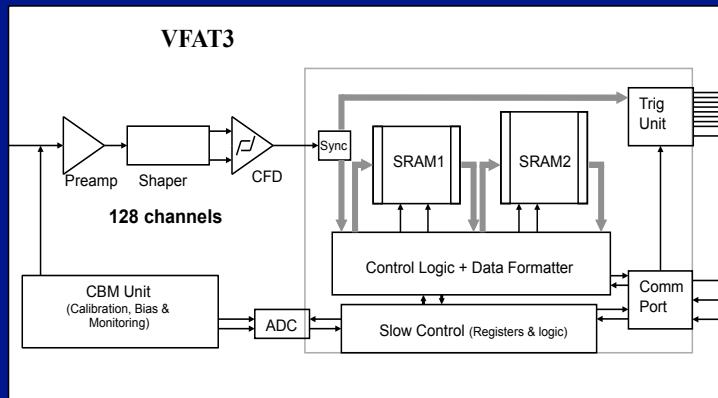
CMS technical note in prep.

VFAT3 front-end specification.

DR Upper limit	Noise floor @ Cd=20pF	Signal seen with S/N=20
10fC	975e (0.156fC)	3.12fC
30fC		
60fC		

VFAT3

Design Team



VFAT3 (currently in assembly phase of design)

CERN :

P. Aspell Coordination

Design Team :

CERN :

M. Dabrowski

INFN Bari

F. Loddo, G. De-Robertis, F. Licciulli

LUT

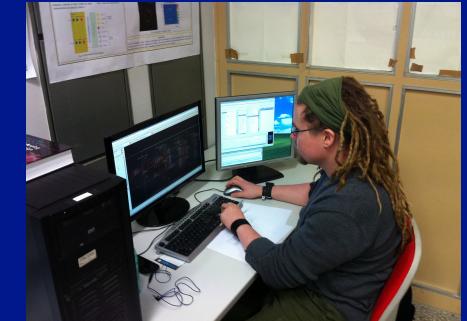
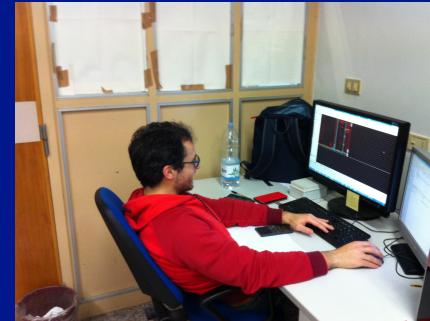
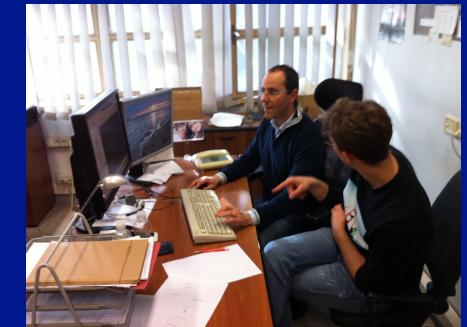
H. Petrow

KU Leuven

B. Van-Bockel

AGH

M. Idzik (AGH coordination)

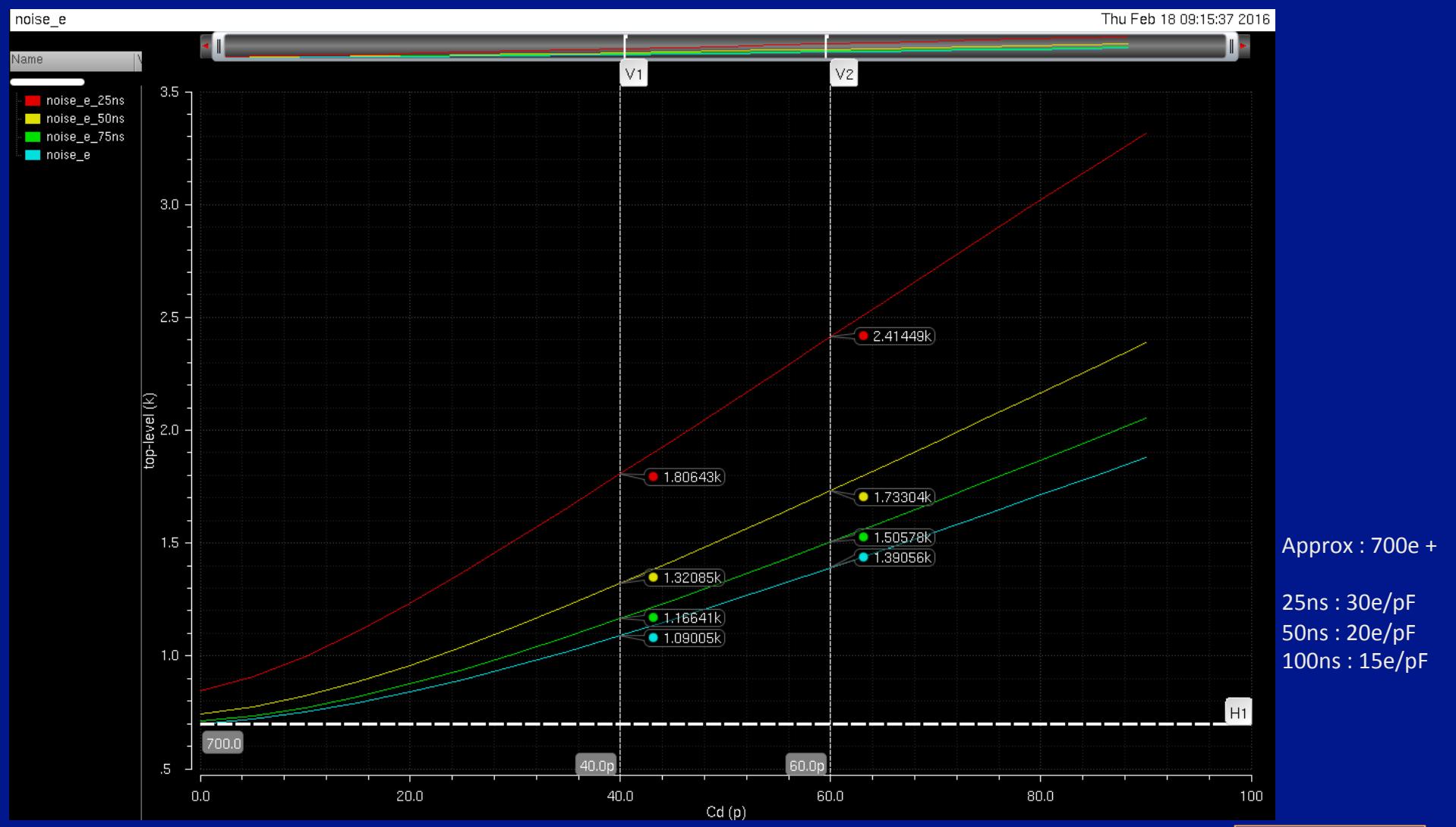


VFAT3 Building Blocks design status

✓	done
➔	ongoing

Modules	Schematic/ verilog code	Simulation Analog or digital	High level Verilog/ verilog AMS model for full chip simulation	Testability added	layout	Verification of module	Chip integration
Analog Front-end	✓	✓	✓	✓	➔		
Calibration block	✓	✓	✓	✓	✓	✓	➔
Bias block, bandgap, DACs etc	✓	✓	✓	✓	✓	✓	➔
Internal temperature sensor	✓	✓	✓	✓	✓	✓	➔
Input protection	✓	✓		✓	➔		
CFD	✓	✓	✓	✓	✓	✓	➔
ADC	✓	✓	✓	✓	✓	✓	➔
Power-on Reset	✓	✓	✓	✓	✓	✓	➔
Control Logic	✓	✓	✓	✓	✓	✓	➔
SRAMs	✓	✓	✓	✓	✓	✓	➔
Slow control system	✓	✓	✓	✓	✓	✓	➔
Trigger Logic	✓	✓	✓	✓	✓	✓	➔
Data Formatter	✓	✓	✓	✓	✓	✓	➔
Slvs (drivers/receivers)	✓	✓			✓	✓	➔

VFAT3 simulated ENC



VFAT3 Simulated ENC

1. DR10: with 50ns, 75ns or 100ns, expected operating mode for GE11 to boost S/N.
2. DR10: with 25ns to achieve similar performance to VFAT2.

Programmable range name	ENC @ Cdet=20pF			
	25ns	50ns	75ns	100ns
HG (DR10)	1259e (0.2fC)	1028e (0.17fC)	972e (0.16fC)	956e 0.15fC
MG (DR30)	2470e	2290e	2260e	2280e
LG (DR60)	4590e	4350e	4350e	4390e

Programmable range name	Minimum signal charge required for S/N = 20			
	25ns	50ns	75ns	100ns
HG (DR10)	4fC	3.3fC	3.1fC	3.1fC

Reminder :
 Charge per strip (all strips):
 MPV (nominal) = 110 ~ 4 fC
 Mean (nominal) = 292 ~ 10 fC
 99% (nominal) ~ 65fC
 Mean (max HV) ~ 17 fC
 99% (max HV) ~ 75 fC

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 Department of Physics and Space Science
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 August 11, 2015

Full chip simulation: Trigger Latency Path verification

Trigger latency path specification

Latency to TMB

1-2bx

4-6bx

+

1-2bx

+

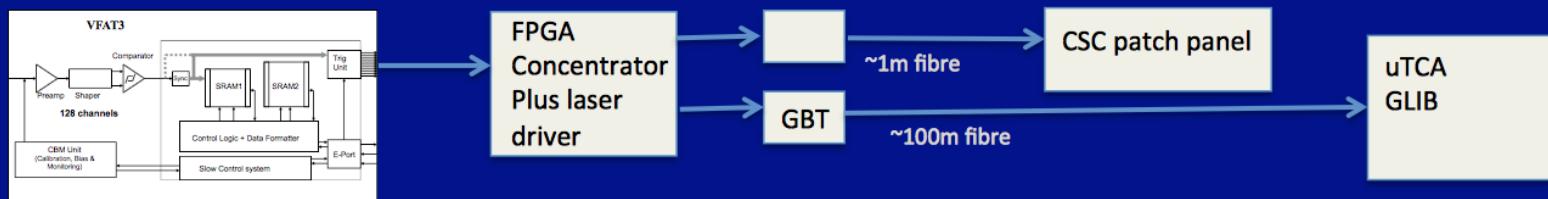
3bx

+

5bx

= 14-18

TOF



Latency to uTCA

1-2bx

4-6bx

+

1-2bx

+

3bx

+

5bx

+

20bx

+

5bx = 39-43bx

Results from simulation

(measured from the start of the injected pulse to the corresponding last bit of the trigger bit transmission)

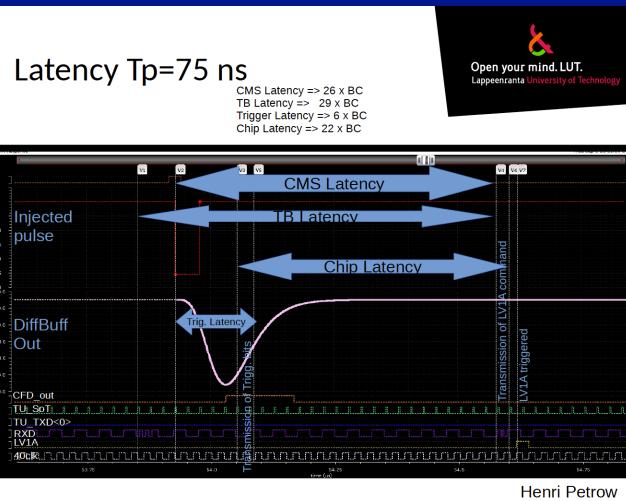
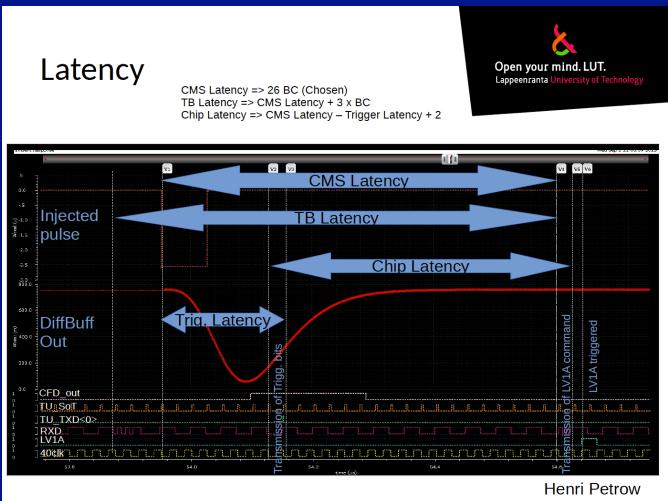
Latency

Trigger latencies with different peaking times:

T _p [ns]	Trig. Path [BC]
100	8
75	6
50	5
25	4

Full chip simulation: Data Path Latency

Latency

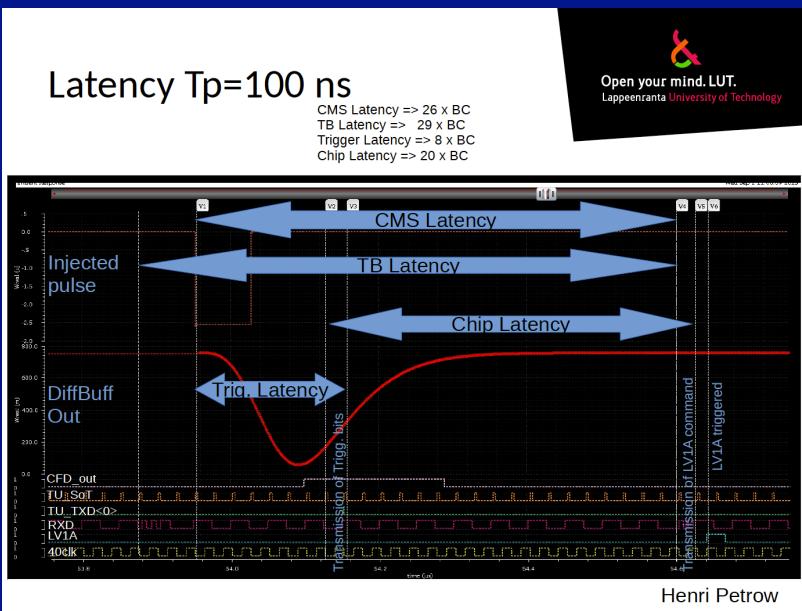


Trigger Latency

Trigger latencies with different peaking times:

Tp [ns]	Trig. Path [BC]
100	8
75	6
50	5
25	4

Latency Tp=100 ns



Trigger Latency = Number of bx between the start of the injected pulse to the corresponding last bit of the trigger bit transmission

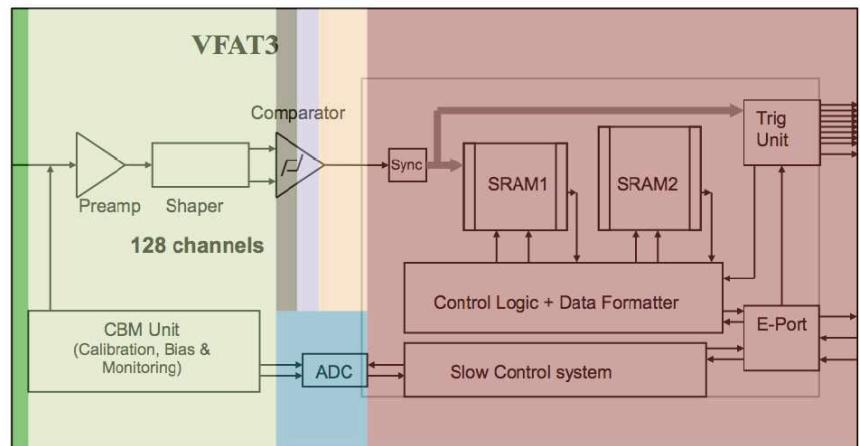
Chip Latency = the programmed value into the VFAT3 slow control registers.

CMS Latency = The actual LV1A latency (in bx) between the signal and the start of the LV1A command string.

TB latency = the number of bx between the start of the CalPulse and the start of the LV1A command strings. To be used in DAQ routines and simulation test benches.

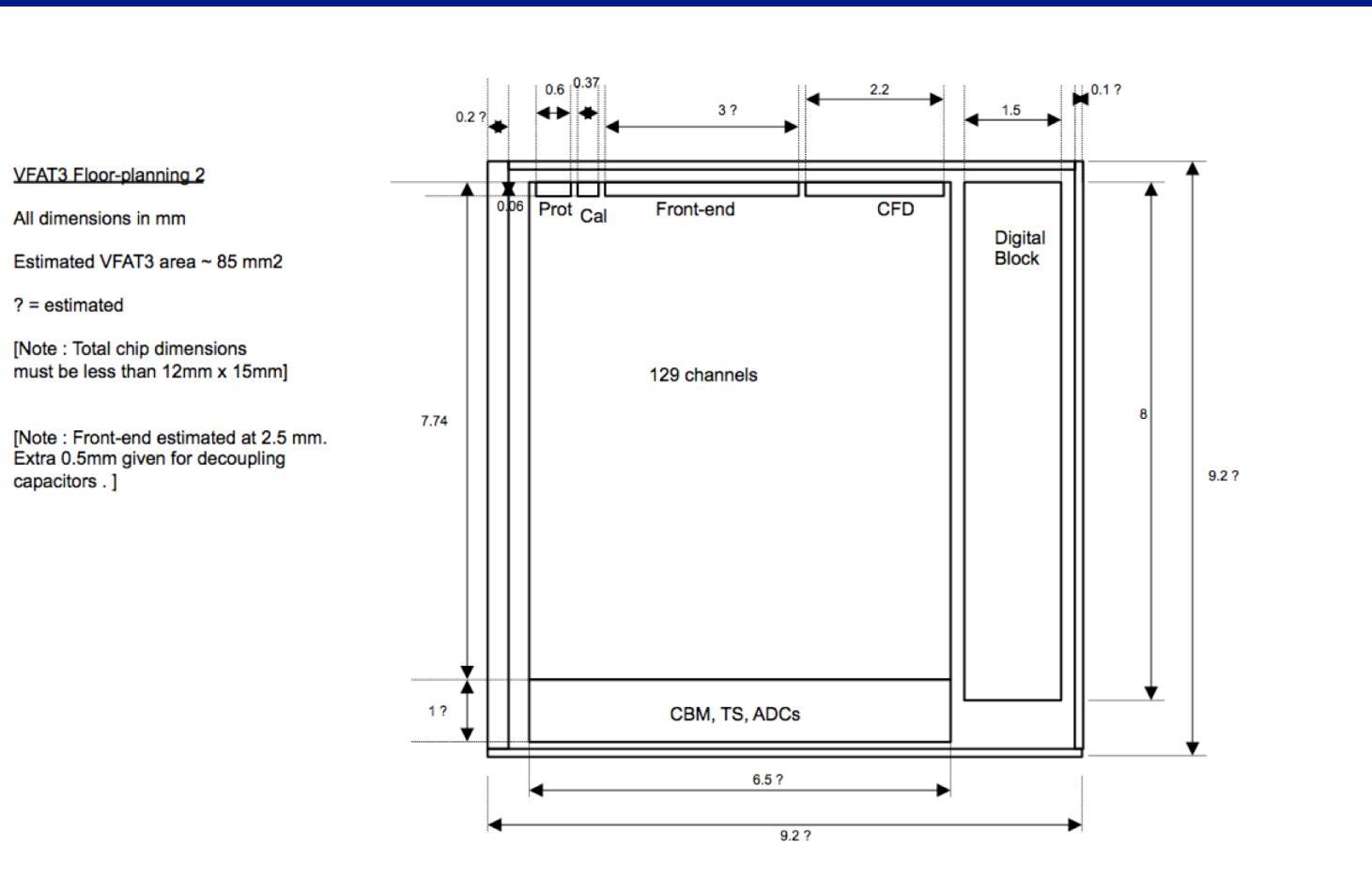
- **Chip latency** = CMS Latency + 2 – Trigger Latency
- **Chip latency** = TB Latency – 1 – Trigger Latency

VFAT3 Power Planning & Analysis



Analog Modules	Power/module	Power/channel	Power/chip
Preamp + shaper	2mW		
Single to diff buff	0.36mW		
CFD	0.36mW		
Total Analog Consumption (including overheads)			approx. 400mW
Digital Modules			
Digital block	86mW		
SLVS driver	2.64mW		
SLVS receiver	0.72mW		
Total Digital Consumption			114mW
Total chip consumption			approx. 520mW

VFAT3 Floor-plan



TSMC 130nm CMOS

Submission planned directly in an MLM engineering run

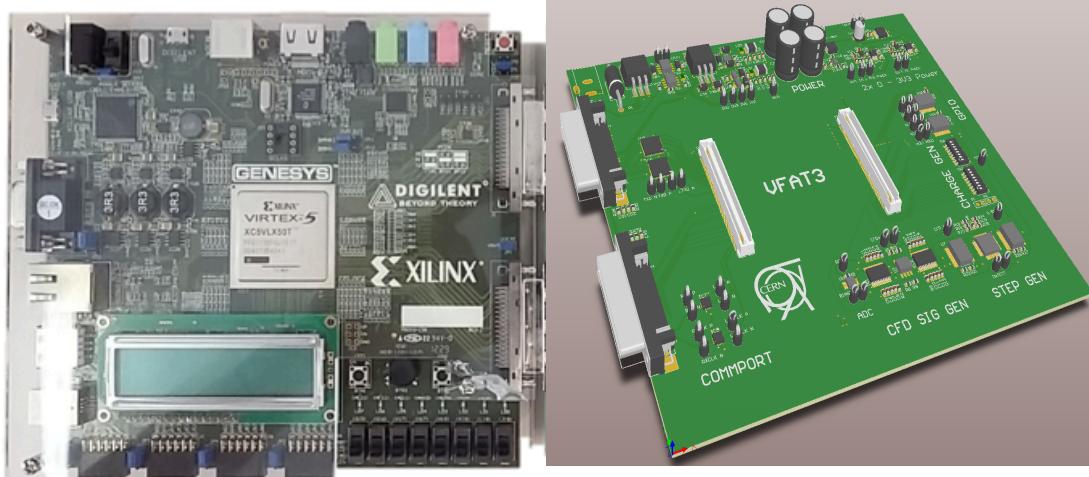
VFAT3 Test System Plan

Design for Functional Test,
Characterisation and Production Tests.

- Xilinx Genesys development board + custom board with 2 stages of daughter board.
- First package a few samples in ceramic package at CERN & test.
- Second package chip in BGA
- Example shown is the GBT SCA system.

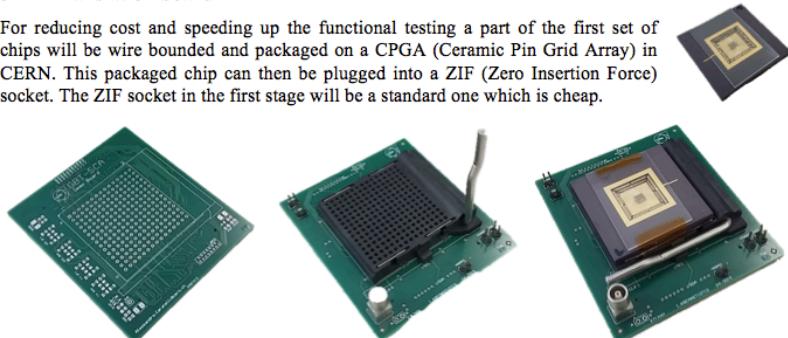
4 Test setup

In total the whole test setup would look like the picture below.

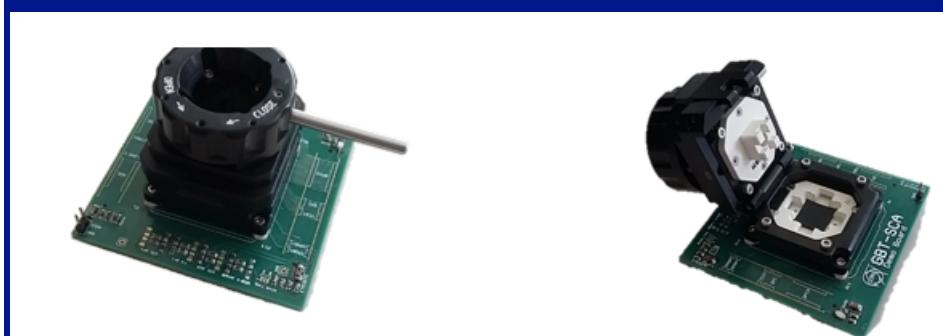


3 Translation board

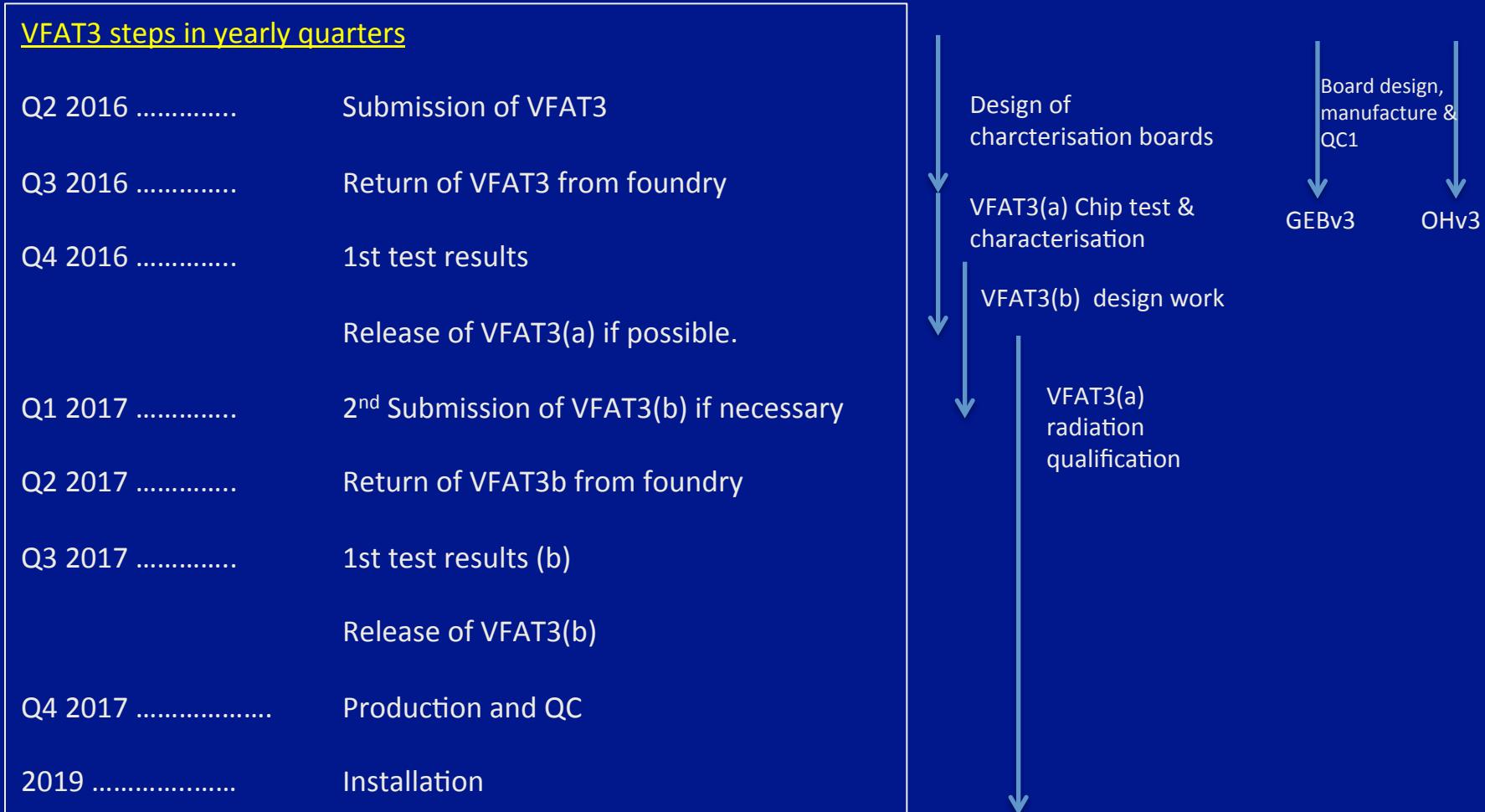
For reducing cost and speeding up the functional testing a part of the first set of chips will be wire bounded and packaged on a CPGA (Ceramic Pin Grid Array) in CERN. This packaged chip can then be plugged into a ZIF (Zero Insertion Force) socket. The ZIF socket in the first stage will be a standard one which is cheap.



Eventually when it is proven that the VFAT3 chip is working correctly, the chip can be properly packaged and a custom ZIF socket can be ordered.



VFAT3 Submission Schedule & Goals



End

Thanks very much

Additional Slides

Detector Studies & Timing Resolution

Timing resolution determined by detector.

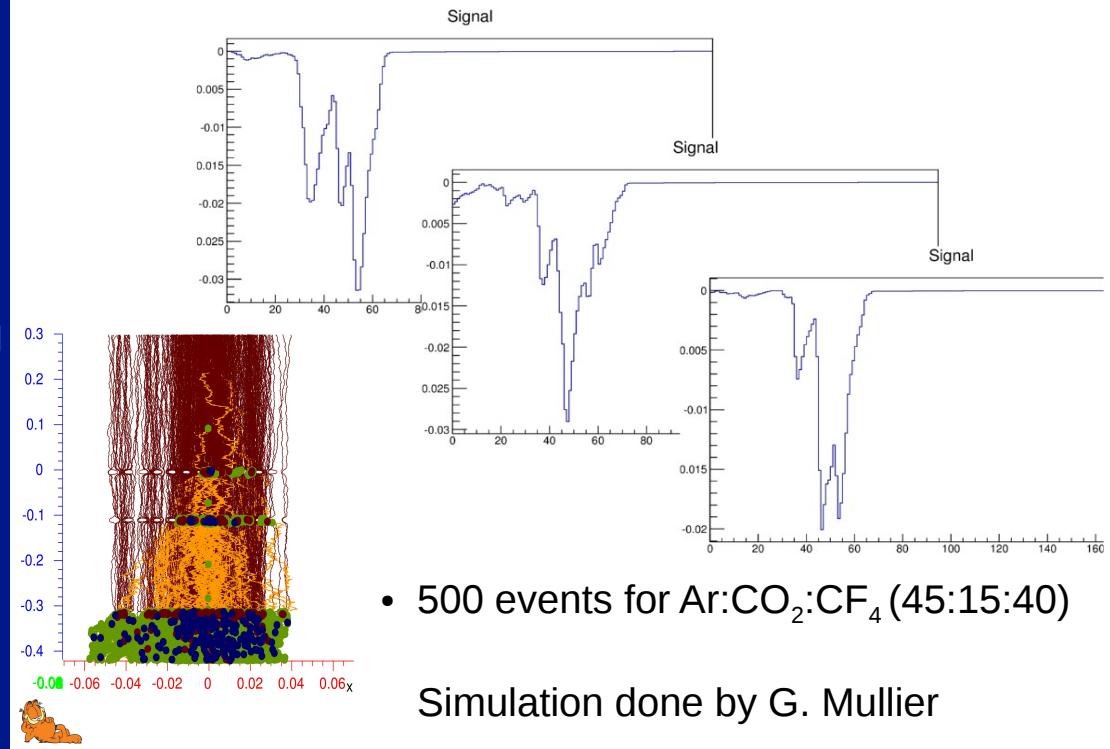
Fast shaping (as with VFAT2) give good timing resolution (<6ns) but bad signal to noise due to ballistic deficit.

Slower shaping times give better S/N but worse timing resolution due to time walk.

VFAT3 analog discriminator would use CFD to correct time walk and recover timing resolution.



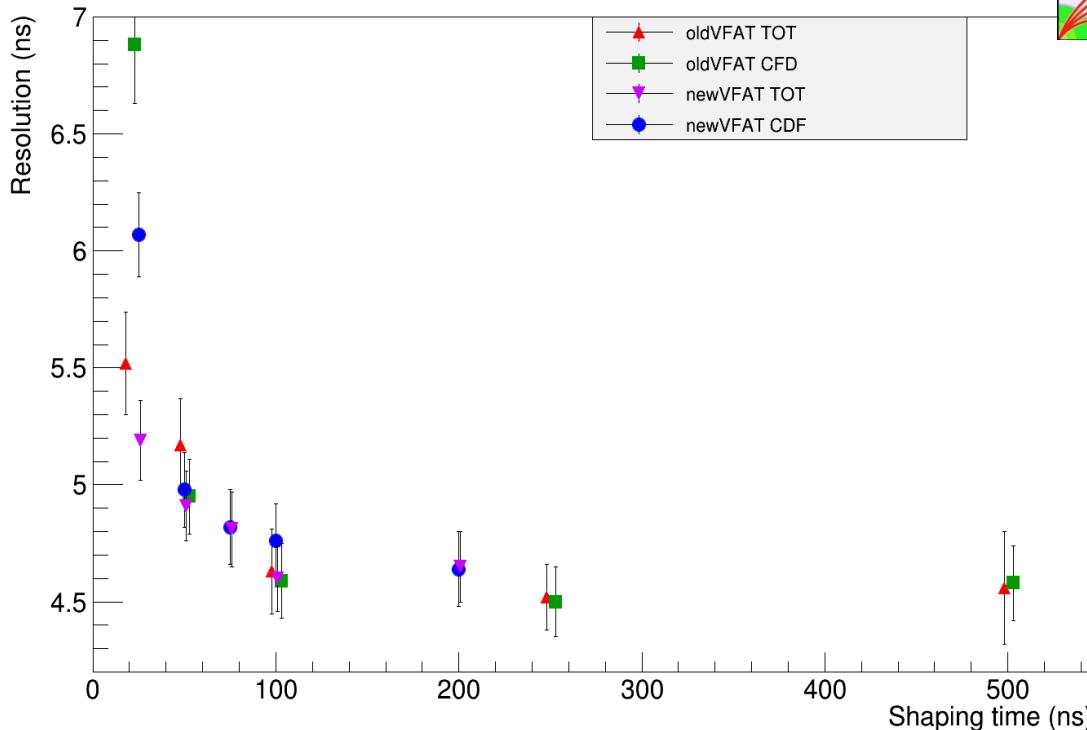
GARFIELD simulations



Recovering Timing Resolution in VFAT3 using a CFD

ULB

all Time Resolutions Ar:CO₂:CF4



Old VFAT3

Shaping time (ns)	20	50	100	200	500
Resolution TOT (ns)	5.52 +/- 0.22	5.17 +/- 0.2	4.63 +/- 0.18	4.52 +/- 0.14	4.56 +/- 0.24
Resolution CFD (ns)	6.88 +/- 0.25	4.95 +/- 0.16	4.59 +/- 0.16	4.50 +/- 0.15	4.58 +/- 0.16

New VFAT3

Shaping time (ns)	25	50	75	100	200
Resolution TOT (ns)	5.19 +/- 0.17	4.91 +/- 0.15	4.81 +/- 0.16	4.60 +/- 0.14	4.65 +/- 0.15
Resolution CFD (ns)	6.07 +/- 0.18	4.98 +/- 0.16	4.82 +/- 0.16	4.76 +/- 0.16	4.64 +/- 0.16

13

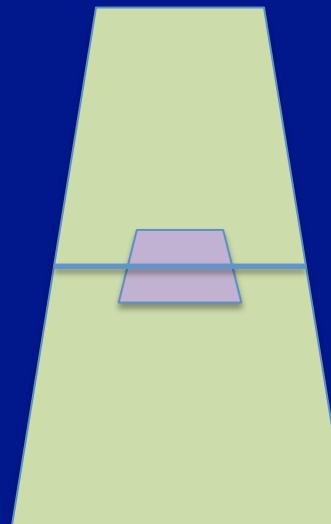
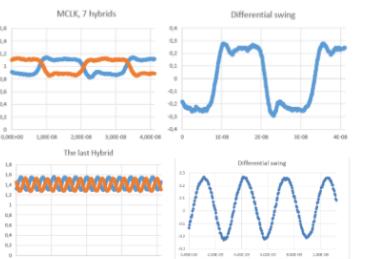
T.Maerschalk,
ULB

GEBv3

- Signal integrity:

- 40 MHz:
fine

- 320 MHz:
borderline



GEBv2 signal measurements show good operation @ 40MHz but boarder line signal integrity @ 320MHz.

Solution : Split GEB into two pieces, placing the OH in the middle therefore reducing the capacitance of the longest SLVS lines by a factor 2.

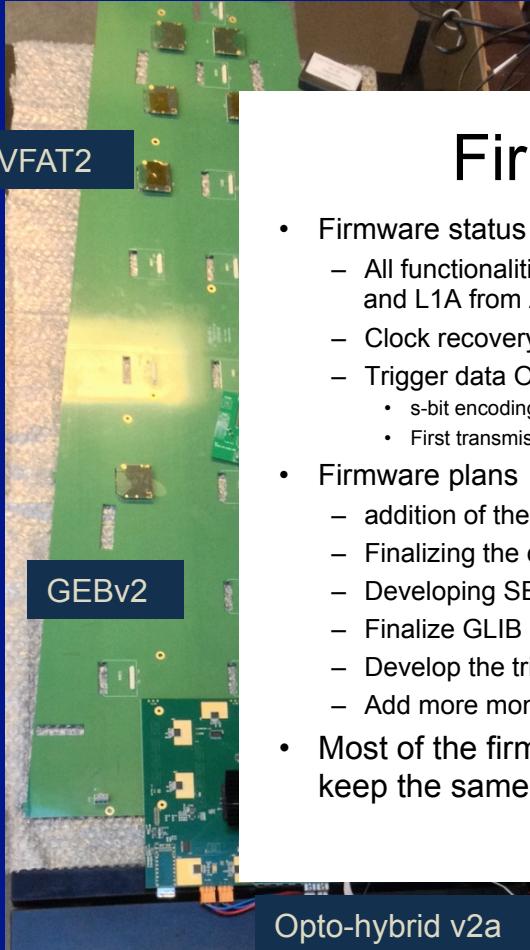
- Advantages of splitting the GEB

- Shorter lines → more tolerance for the receiver
 - Possibly faster production and assembly
 - Might fit into an oven → faster assembly and a possibility to mount packaged VFAT3 chips directly to the GEB → better signal integrity, possible cost savings
 - No Halogen-free PCB material for 1.2 m, 1 meter should be ok.

- Disadvantages of splitting the GEB

- Cooling, etc. needs to be redone
 - Less space for the OH
 - How to connect the ground planes of the two GEBs

Prototyping for the Slice Test



GE1/1 inside the cooling box

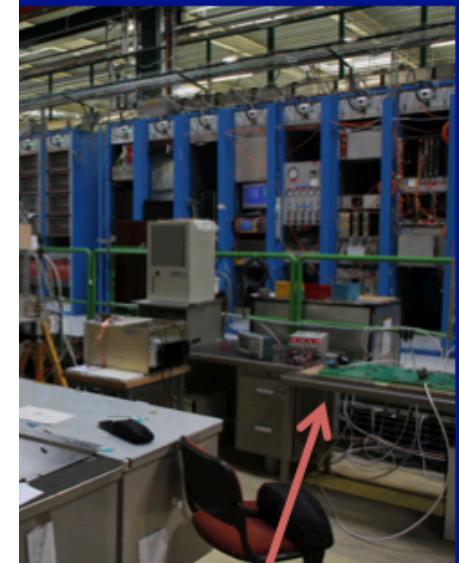
Firmware for slice test

- Firmware status
 - All functionalities to take data exist (demonstrated at test beam, getting clock and L1A from AMC13)
 - Clock recovery from optical link tested on non-GBT links
 - Trigger data OH-CSC transmission:
 - s-bit encoding tested (Max 8 s-bit per detector per BX)
 - First transmission between OH and CSC TMB performed last week
- Firmware plans
 - addition of the GBT and CCB HDMI links
 - Finalizing the calibration routines (also for QC tests)
 - Developing SEU mitigation
 - Finalize GLIB event builder
 - Develop the trigger data processing on GLIB for slice test
 - Add more monitoring and diagnostic functions
- Most of the firmware can be reused for the LS2 electronics (we keep the same FPGA on Opto-hybrid)

Opto-hybrid v2a

ME1/1

CERN 904



GE1/1 Setup for VFAT
and GEB tests.

Production and Quality Control Planning of v3 parts.

VFAT3:

- Functional test of each VFAT3 module : Carried out at CERN.
- VFAT3 packaged in CERN ceramic packages.
- Characterisation Tests : Characterisation to be done for both CERN ceramic package and custom BGA.
- Production Test : Characterisation routines plus production test routines to be developed.

Production test for all BGA packaged chips using ZIF socket daughter board.

GEBv3:

- Production probably in China.
- PKU to supervise production and perform initial QC1 checks in China.
- GEBs shipped to LUT for component mounting including packaged VFAT3 chips followed by QC2 tests.
- GEBs shipped to CERN for QC3 (system test in 904).

OHv3:

- Production is being investigated in S. Korea. Production supervised by University and QC1 (using standard lab equipment to be done in S. Korea). QC1 procedure to be defined by ULB.
- OHs shipped to ULB for QC2 (more extensive testing including optical links)
- OHs shipped to CERN for QC3 (system test in 904)