Development of a rad-hard switch for the HV power distribution in the ATLAS-Upgrade

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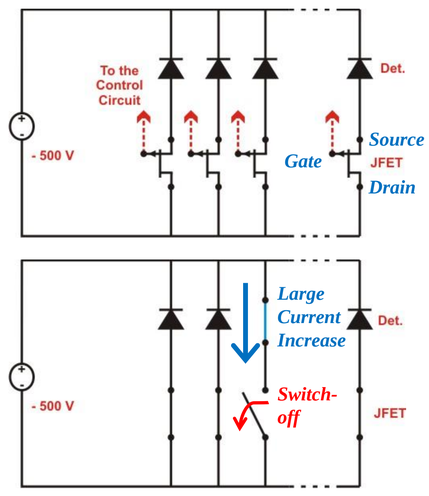
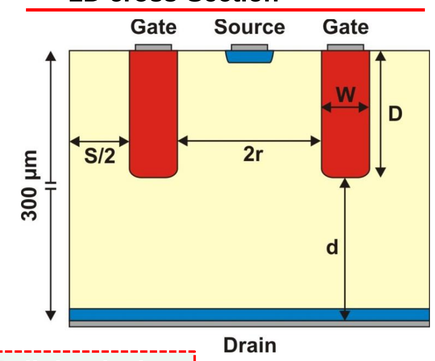
— Abstract—

- New silicon vertical JFET transistor to be used as switch for the HV powering scheme in the ATLAS upgrade Inner Tracker.
- Based on a trenched technology developed at the IMB-CNM.
- Thorough optimization work has been performed by 2D and 3D TCAD simulations.
- Selected designs have been chosen for device fabrication at the IMB-CNM clean room. First prototypes have been recently produced.
- Features of the first fabrication devices are presented
- First characterization results show excellent agreement with simulation, already meeting ITk specifications.
- Simulations of radiation hardness show good performance

— Custom Vertical JFET switch for HV-MUX—

Goal: *Switching-off a **malfunctioning sensor** when it demands too much current to the power supply*

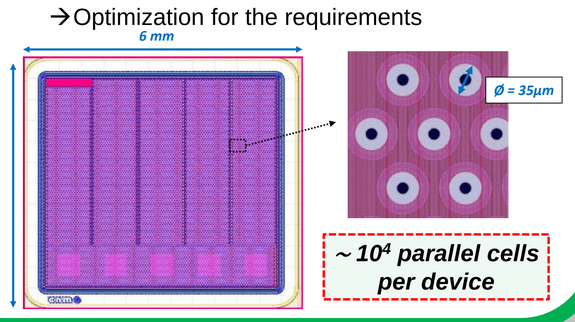




Cellular design

- *Each cell presents a conduction channel, surrounded by a deep trench (with circular layout), which constitutes de gate electrode.*
- *The channel current is modulated by the depletion region extended from the gate-substrate reverse-biased junction*

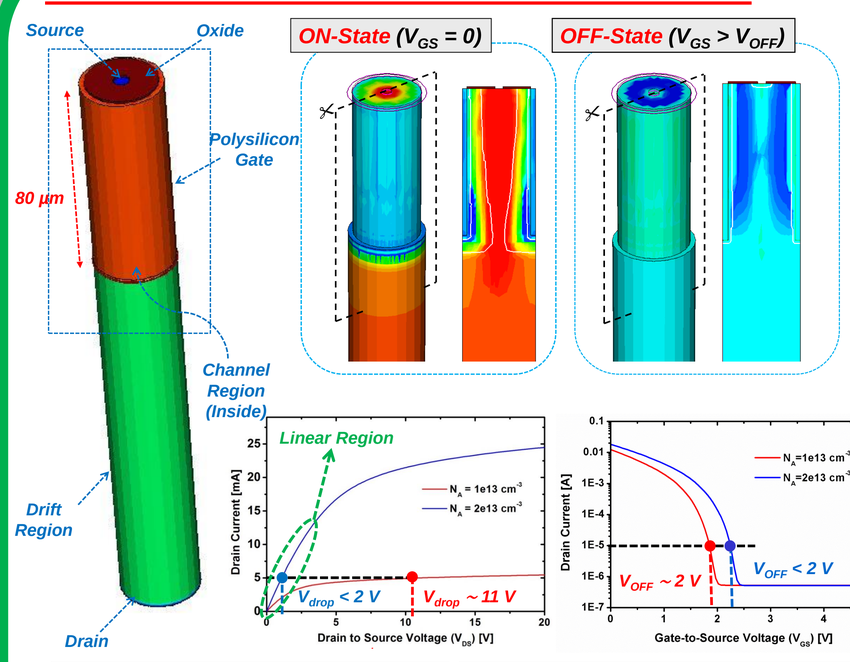
- **Features**:
  - **Depletion mode device** → (Normally ON)
  - **3D Device** with **Vertical Conduction**
    - →High voltage capabilities
    - →Rad-hard against ionization
    - →Low switching-off voltage
  - **P-type**
    - → Lower (and known) displacement damage
  - **Cellular design**
    - →Adaptable current capability
  - **Custom made**
    - →Optimization for the requirements



~ 10^4 parallel cells per device

— Performance —

Inner cell (3D simulation)



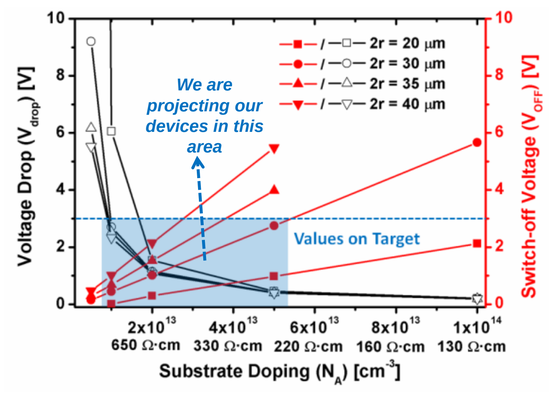
ON-State performance is **characterized by** the voltage drop (V_{drop}) caused on the sensor bias

V_{OFF} is the V_{GS} value for which **I_{OFF} is comparable to the sensor leakage** in normal operation (~ 10 µA)

— Optimization —

Design Optimization Variables

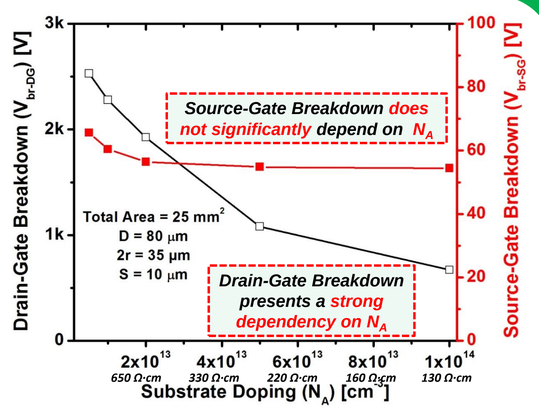
- Channel width: **2r**
- Trench Depth: **D**
- Substrate Doping Concentration: **N_A**



Requirements for the application

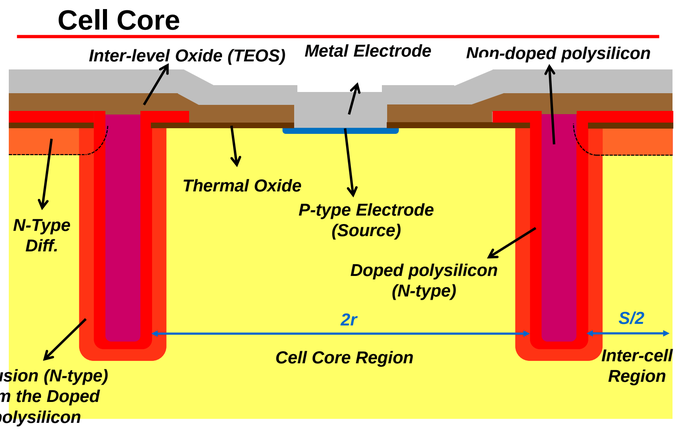
Figure of Merit	Requirement	Target Value
V_{BR}	> 500 V	~ 1000 V
I_{ON}	1-10 mA	5 mA
V_{drop}	few volts	< 3 V
V_{OFF}	< 3 V	< 1 V
I_{OFF}	< 200 µA	~ 10 µA
Area	< 9×9 mm^2	6×6 mm^2

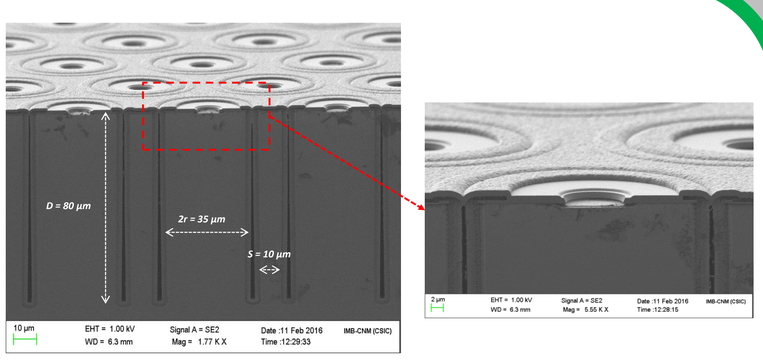
- **D** is optimized ranging **60-100 µm**
  - Trenches with **D < 50 µm** lead to strong **Increase of V_{OFF}**
  - Deeper trenches lead to **worse yield**



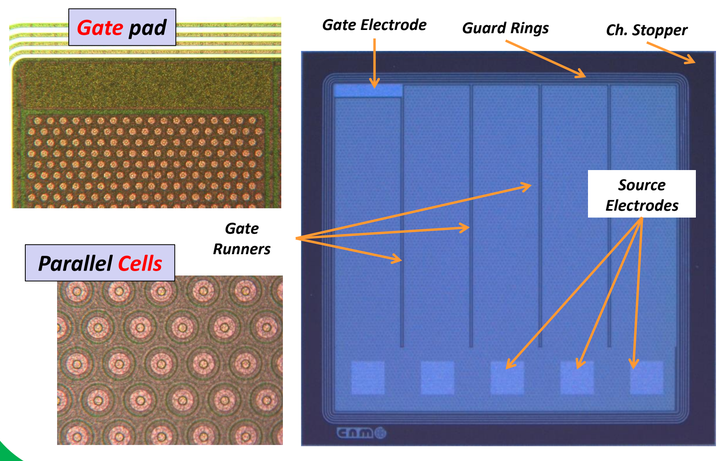
Edge termination techniques (floating guard Rings, deep N-type diffusions, P-Spray....) are considered to recover the breakdown values

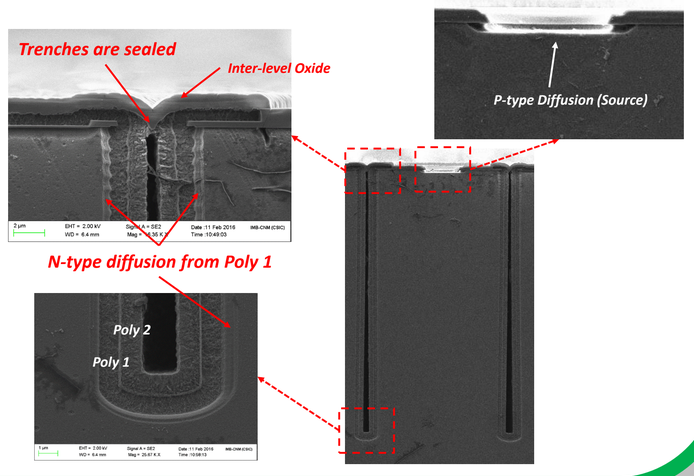
— Fabrication —





Trench Etching (Deep RIE Technique) and **filling** (with polysilicon) are the critical fabrication steps





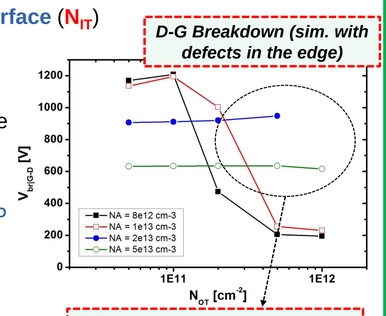
— Radiation Hardness—

Requirements for the application (Strips)

- Devices are expected to operate under **Fluence ~ 2×10^{15} n_{eq}/cm^2** and **Dose ~ 50 Mrad**

Ionization (TID) Effects

- Two physical **mechanisms**:
  - Accumulation of **positive fixed charge** within the oxide volume (N_{OT})
  - Formation of charge **traps at the Si/SiO_2 interface** (N_{IT})
- Expected electrical **effects**:
  - Minor effect on V_{OFF}, V_{drop} and I_{OFF}
  - Degradation of the voltage capability of the Gate-Source junction ($V_{br|G-S}$)
  - Impact on edge termination efficiency
    → **Increase of I_G and/or reduction of $V_{br|G-D}$**



No significant TID effects have been observed in V_{OFF}, V_{drop} and I_{OFF} in the performed TCAD Simulations

Displacement Damage (DD) Effects

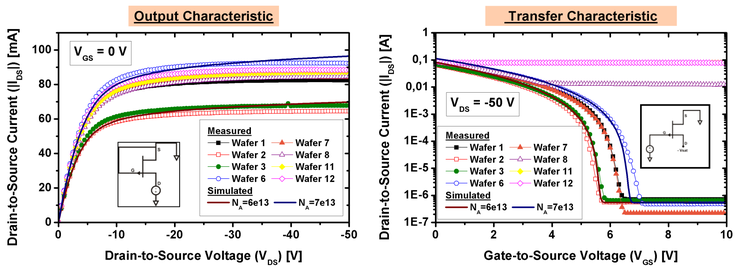
- Different effects depending on the **operation mode**:
  - **OFF-State**: **Charge generation**, reduction of **minority carrier lifetime**, and **trap assisted tunneling** are major issues
  - **ON-State**: **Majority carrier removal** and **mobility degradation** are important
- Expected **effects**:
  - In **OFF-State**: Increase of V_{OFF} , I_{OFF} and I_G
  - In **ON-State**: I_{ON} decrease with an increment of V_{drop}

OFF-State issues can be studied with TCAD Simulations
→ **Perugia Model of silicon Traps**

ON-State performance is like a lowly doped silicon resistor
→ **Study of Mobility degradation in irradiated diodes and resistors**

— First Measurements —

Wide Channel Devices (2r = 35 µm; s = 10 µm)

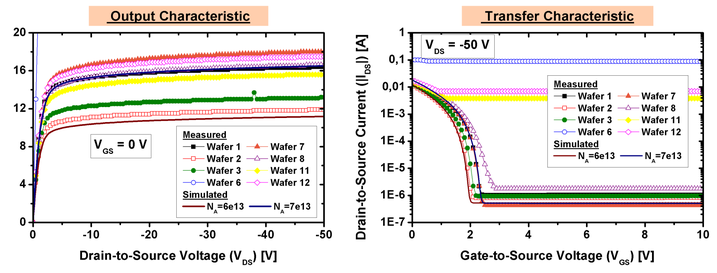


	I_{DSS} (I_{DS} @ V_{DS} =-50V)	V_{drop} (V_{DS} @ I_{DS} = 5mA)	V_{OFF} (V_{GS} @ I_{DS} =10 µA)	I_{OFF} (I_{DS}@V_{GS}=10V)
Measured	65 – 92 mA	0,25 – 0,32 V	5.4 – 6.8 V *	0.2 – 0.7 µA *
Sim (6e13)	70 mA	0.32 V	5.5 V	0.5 µA
Sim (7e13)	96 mA	0.26 V	6.5 V	0.5 µA

**Devices with very high I_{OFF} excluded*

- *Very ideal JFET devices*
- *This device case (wide):*
  - ✓ *Very high current*
  - × *High cut-off voltage (~ 6 V)*
- *Good agreement with simulations → Confirms simulation results*
- *Allows an estimation of substrate doping*

Narrow Channel Devices (2r = 23 µm; s = 10 µm)



	I_{DSS} (I_{DS} @ V_{DS} = -50V)	V_{drop} (V_{DS} @ I_{DS} = 5mA)	V_{OFF} (V_{GS} @ I_{DS} =10 µA)	I_{OFF} (I_{DS}@V_{GS}=10V)
Measured	12 – 18 mA	0.46 – 0.64 V	1.90 – 2.55 V*	0.4 – 1.7 µA*
Sim (6e13)	11 mA	0.68 V	1.85 V	0.5 µA
Sim (7e13)	17 mA	0.50 V	2.25 V	0.5 µA

**Devices with very high I_{OFF} excluded*

- *This case (narrow):*
  - ✓ *High enough current*
  - ✓ *Low enough V_{OFF}*
  - → *Close to target device*
- *Good agreement with simulations → Confirms simulation results*
- *Good starting point for fine optimization*

— Conclusions —

- A new silicon vertical JFET technology is now being developed at the IMB-CNM (CSIC) for the HV-MUX switches required in the future high luminosity upgrade Inner Tracker of the ATLAS experiment.
- Based on a 3D trenched detector technology, the V-JFET has been optimized to meet the high voltage, low resistance, low switch-off voltage, and radiation hardness requirements of the application.
- A complete fabrication procedure has been developed together with a specific layout, which includes a broad number of experiments.
- First prototype batch has been fabricated at the IMB-CNM clean room. Measurements show good agreement with simulations and already meet the HV-MUX specifications.
- Radiation hardness is now under study with the aid of both TCAD simulations and physical models reported in the literature. A thorough irradiation program is planned for the fabricated prototypes.

[*] P. Fernández-Martínez, et al., *"Rad-hard JFET switch for the HV-MUX system of the ATLAS upgrade Inner Tracker"*, Journal of Instrumentation 11 C01043, January 2016

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