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Rad-Hard Vertical JFET switch for the HV-MUX system of the ATLAS upgrade ITk

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This work presents a new silicon vertical JFET transistor, based on a trench technology developed at the IMB-CNM, to be used as switch for the High-Voltage power distribution in the ATLAS upgrade Inner Tracker. After a thorough optimization work, performed by TCAD simulations, selected designs have been chosen for device fabrication at the IMB-CNM clean room. The first prototypes have been recently produced, and the first characterization results show excellent agreement with simulation, already meeting the ITk specifications. The technological process and the simulated rad-hard prospects will be also shown.

Summary

The high-luminosity upgrade of the LHC will demand a substantial improvement of both the radiation sensors and their associated electronics in the ATLAS experiment, in terms of performance, radiation hardness, and compactness. Specifically, the upgrade of the silicon strip sensors represents a large increase in area and number of sensors. Cable space limitations do not permit each sensor to be individually biased. Therefore, groups of sensors will need to share a common high voltage line.

A High Voltage Multiplexing (HVMUX) scheme has been proposed in which a failed sensor is disconnected from the bias bus to permit normal operation of the remaining sensors. Each sensor requires a slow-controlled switch that can survive the high radiation environment, operate in high magnetic fields, and switch more than 500V.

This work presents a new silicon, vertical JFET switch, based on a trench technology developed at the IMB-CNM, which fulfils the HVMUX specifications. This VJFET, produced on a high-resistivity p-type substrate, is conceived as a cellular device, where each cell presents a conduction channel, surrounded by a deep trench with circular layout. The trenches, typically 80 μ m deep, are filled with highly-doped n-type polysilicon to form the gate electrode. The source electrode is implemented with a highly-doped p-type layer at the centre of each cell. The drain electrode, common to all cells, is implanted on the backside, far away from the trenches, to allow for voltage capability in the order of 1000V.

In normal operation, Gate and Source are held at 0V, while drain is at a negative voltage, allowing a current flow through the channel. If VGS is increased above a threshold value, the channel depletes and the VJFET turns off. In fact, its operation in depletion mode (normally-on) stands out among the main features of this switch, as it allows the sensors to be biased without applying any voltage on the VJFET gate. As it is a 3D device with vertical conduction, high voltage capability and low switch-off voltage are achieved, together with ionizing radiation hardness. On the other hand, the layout configuration and the p-type substrate election will contribute to reduce the effects of radiation displacement. Finally, the cellular design and the custom fabrication will allow meeting the specifications for the ITk. 2D and 3D simulations have been performed, confirming all these features.

The first batch of VJFET devices has been produced at the IMB-CNM clean room, with results that already meet the HVMUX specifications for the pre-irradiated devices. Devices with a narrow cell of 23 μ m diameter present very ideal JFET characteristics, in good agreement with the simulations: Cut-off voltage below 2.5V, and on-state current above 15mA, whereas both the off-state current and the gate leakage remain below 1 μ A.

A compile of the test results, together with details of the fabrication process will be provided in the final contribution.

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