The use of the ATLAS New Small Wheel front end Electronics for the HL-LHC MDT upgrade

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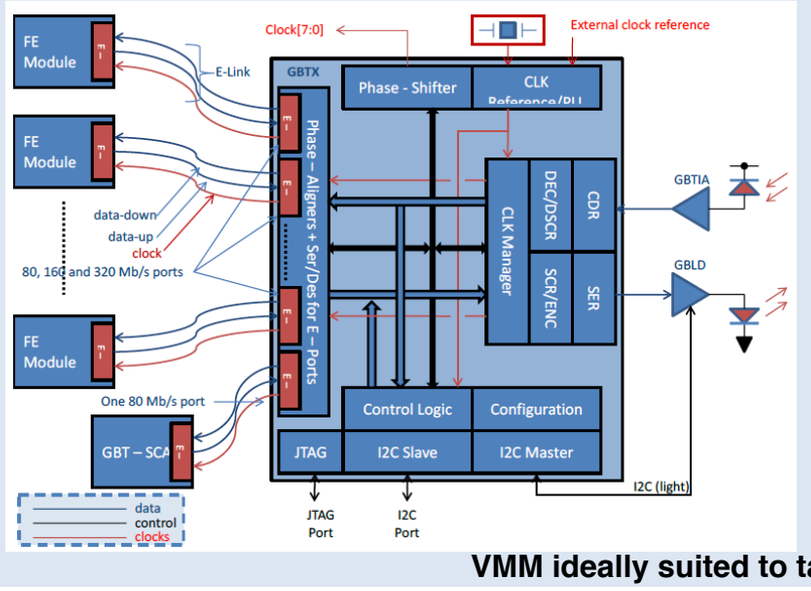
The ATLAS New Small Wheels (NSW) Phase I Muon System upgrade will use Micromegas and small-strip Thin Gap Chambers (sTGC) as both trigger and precision readout detectors. A new ASIC, the VMM, is being developed as a front end of both detector technologies. The VMM is a sophisticated ASIC, System on Chip (SOC), providing digitised amplitude and time information as well as independent trigger paths for both detector systems. In this poster we describe the proposed use of this ASIC (and also the overall NSW electronics readout architecture) for the readout of the planned HL-LHC MDT detector upgrade. Details of the proposed architecture, bandwidth requirements, and plans for implementation are presented. The similarity to the Phase I system and the resulting benefits is stressed.

The GBTx chipset and the New Small Wheel Electronics

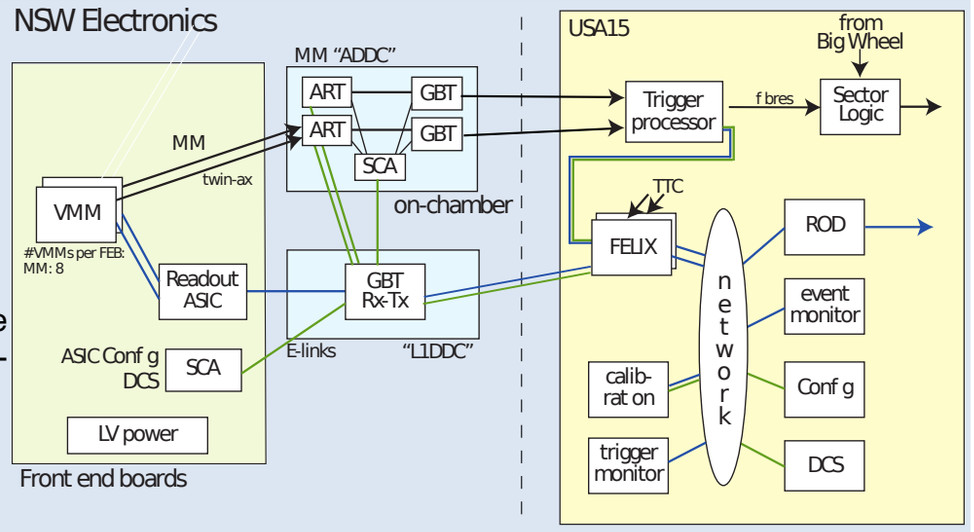


GBTx

- Versatile, radiation tolerant, 3.2 Gbps effective rate designed for the LHC Experiments.
- Bidirectional, can handle simultaneously Data, TTC, Detector Control and Configuration.
- Designed to directly and simply interface with high performing “system on a chip” front ends.

Features

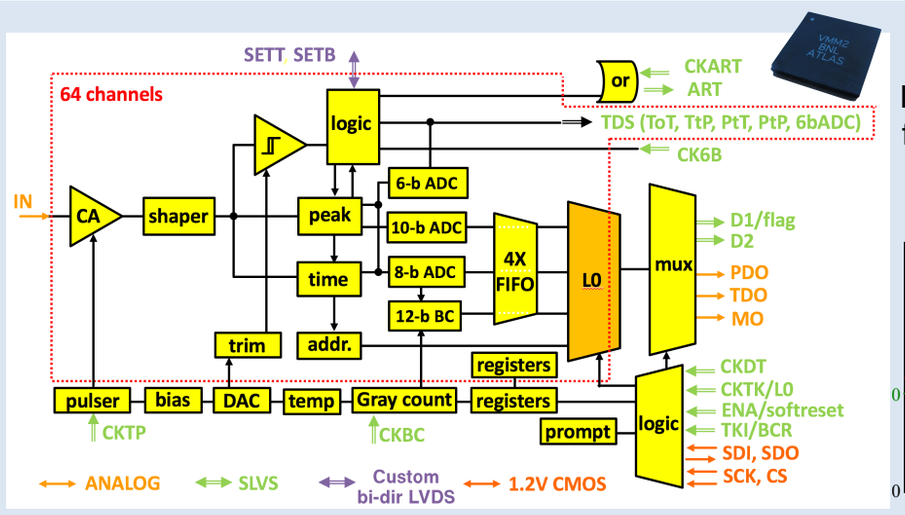
- Has 5 groups of e-links individually programmable in: 8 x 80 Mbps or 4 x 160 Mbps or 2 x 320 Mbps e-links each.
- Synthesises clocks from 40 MHz
- Phase aligned serialiser de-serialiser to e-links
- I2C for configuration of other ASICs in the family



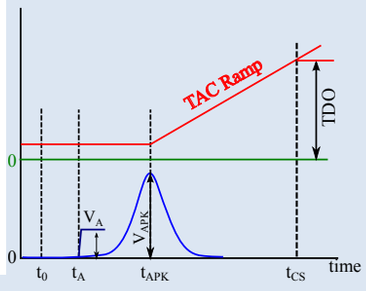
VMM ideally suited to take advantage of these properties

The MDT readout can be exactly the same as the NSW readout!

The VMM ASIC - Architecture and Specifications



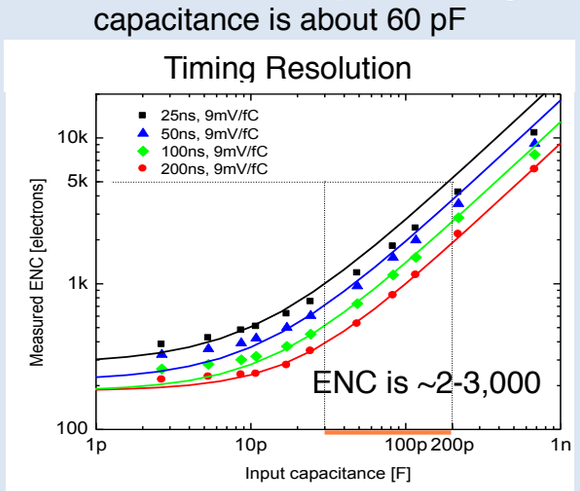
VMM is a custom Application Specific Integrated Circuit (ASIC) fabricated in the 130 nm Global Foundries 8RF-DM process.



Present VMM Specifications

Channels	64
Z_{in} [Ω]	50 - 75
Gain [mV/fC]	0.5 - 16
Gain [mV/pe]	0.125 - 4
Charge linear range [pe]	250 - 8,000
Charge resolution [fC]	~1-2
Shaper	unipolar or bipolar
Shape order	3rd cc
Peaking time [ns]	25 - 200
Pulse width [ns]	200 - 800
Discrimination	yes (hysteris)
Programmable deadtime	to be added
Threshold DAC	10-bits
Amplitude measurement	direct voltage
Timing measurement	TAC (peak or thr)
Time Walk [ns]	< 2
Timing resolution [ns]	< 1
Timing conversion	8-bits
Timing dynamic range	12 coarse + 8 fine
L1 buffer memory	64 deep / channel
Power/channel [mW]	< 10

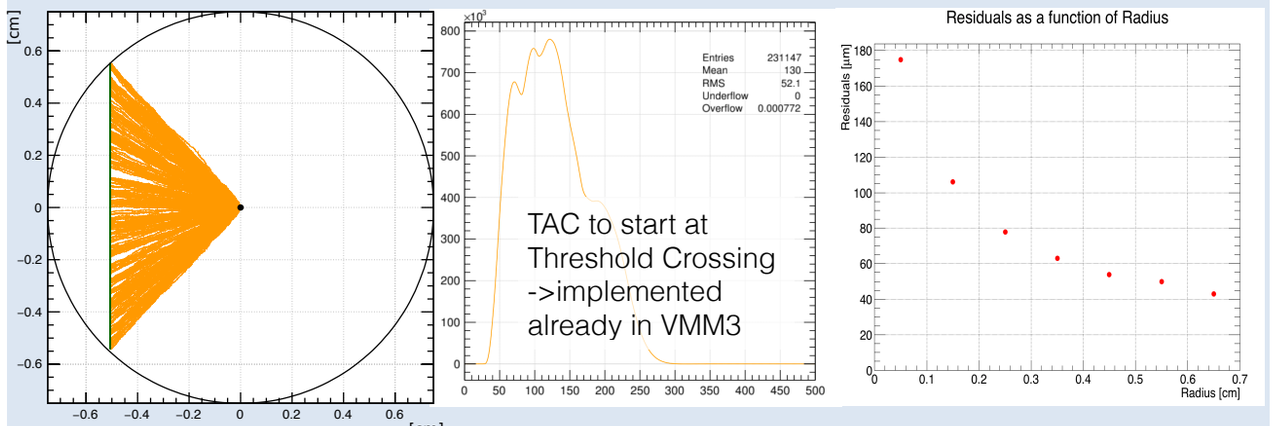
For the MDT tubes ~ 10 pF/m the largest capacitance is about 60 pF



Timing resolution well under 1 ns

Simulation - The MDT Readout based on VMM and GBTx

Simulation of Incident Tracks through Garfield++. Analytic VMM shaper and residual calculation

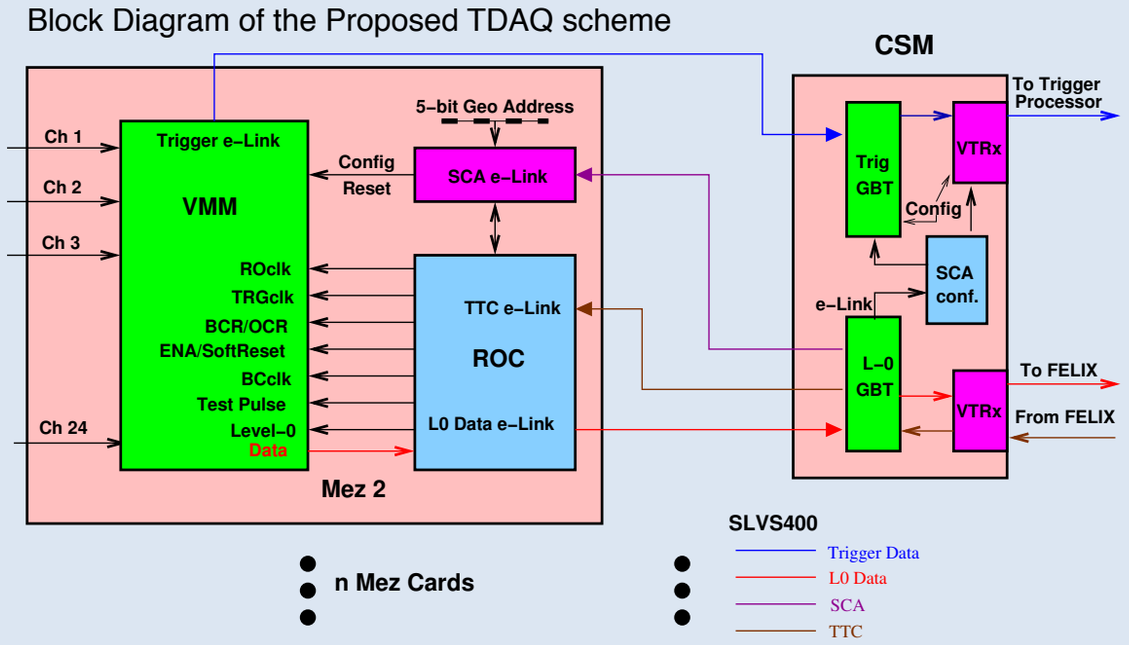


Resolution is basically noise limited and shorter integration time would result in higher resolution. The charge collected in 15 ns is ~80% of that collected in 25 ns. VMMx will include a 15 ns peaking time in addition to the four already existing.

$$\sigma_t = \frac{ENC}{Q}\tau_{peak} \propto 1/\sqrt{\tau_{peak}}$$

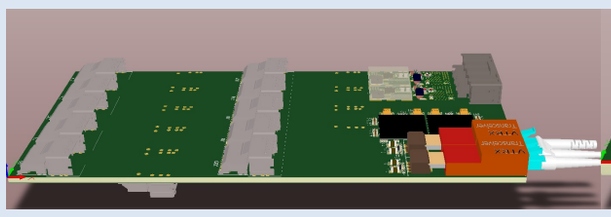
$$\frac{\sigma_{15}}{\sigma_{25}} \propto \frac{\sqrt{15}}{\sqrt{25}}\frac{Q_{25}}{Q_{15}} \approx 1$$

Block Diagram of the Proposed TDAQ scheme

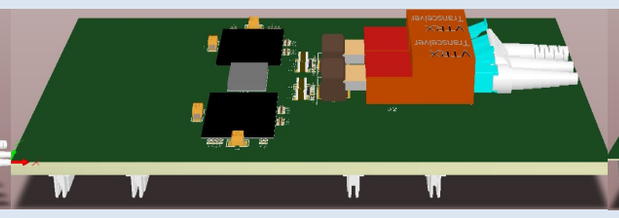


- Simple and compact system with direct, full resolution trigger path in parallel to the L0/ L1 Readout which does not need a “Hit Extractor” (as alternative designs require).
- Trigger BCID matching, L0, L1 FIFOs handled already in the Mezzanine card in a way exactly compatible with the Phase-I NSW readout.
- Radiation tolerant (no FPGAs are used)
- Robust TTC distribution, Mezzanine ROC with PLL for clean clock regeneration
- DCS and configuration handled by the SCA
- VMM can handle about 0.5 MHz single tube rate (2 GBTx or 1 LpGBTx)

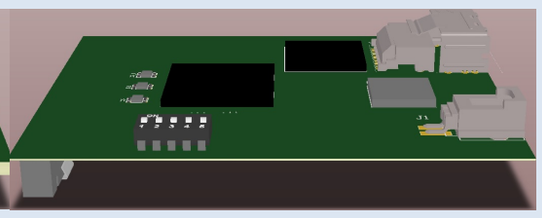
Prototypes for Testing



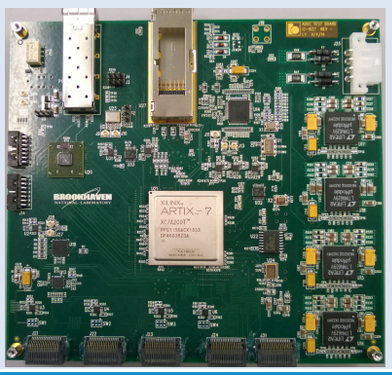
CSM with Mini-SAS (new cables are used) connectors and GBTx. Two VTRx are used to send L0 and Trigger data.



CSM compatible with existing connectors (old cables are used) connectors and GBTx. Two VTRx are used to send L0 and Trigger data.



Mezzanine Card with mini-SAS connector and VMM, SCA and a Read out Controller



- Use ADDC-v1 prototype developed for Micromegas Trigger
- Trigger outputs from VMM3 do not yet implement e-link
- Use Artix-7 to emulate e-link protocol with GBT-FPGA code provided by CERN