Preliminary Experimental Results of A 14-bit Split-SAR ADC for ATLAS LAr Phase-II Upgrade

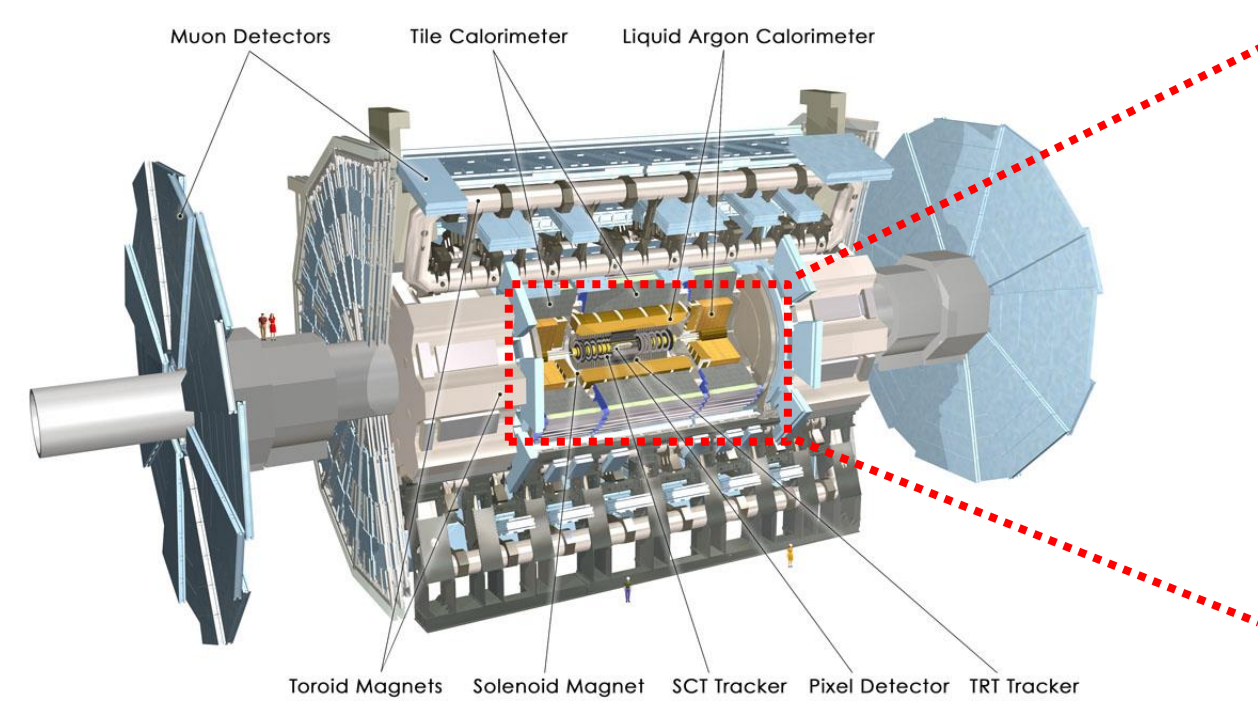**Hongda Xu[1], Yongda Cai[1], Ling Du[1], Datao Gong[2], and Yun Chiu[1]**

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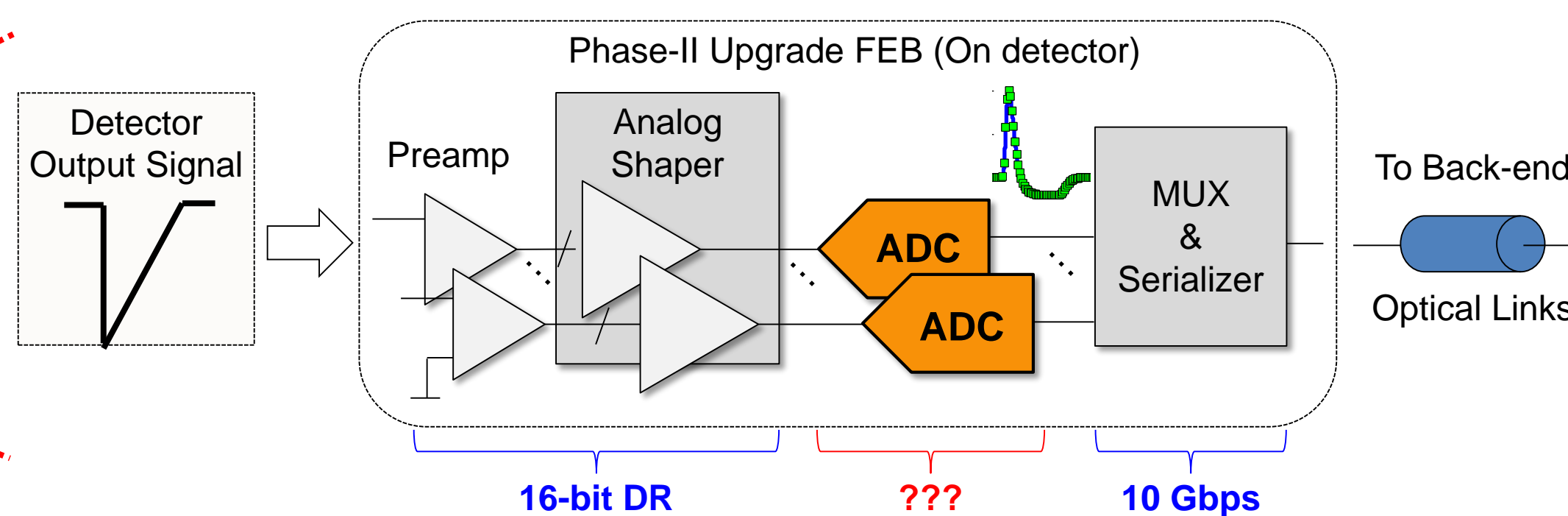
Background and Motivations
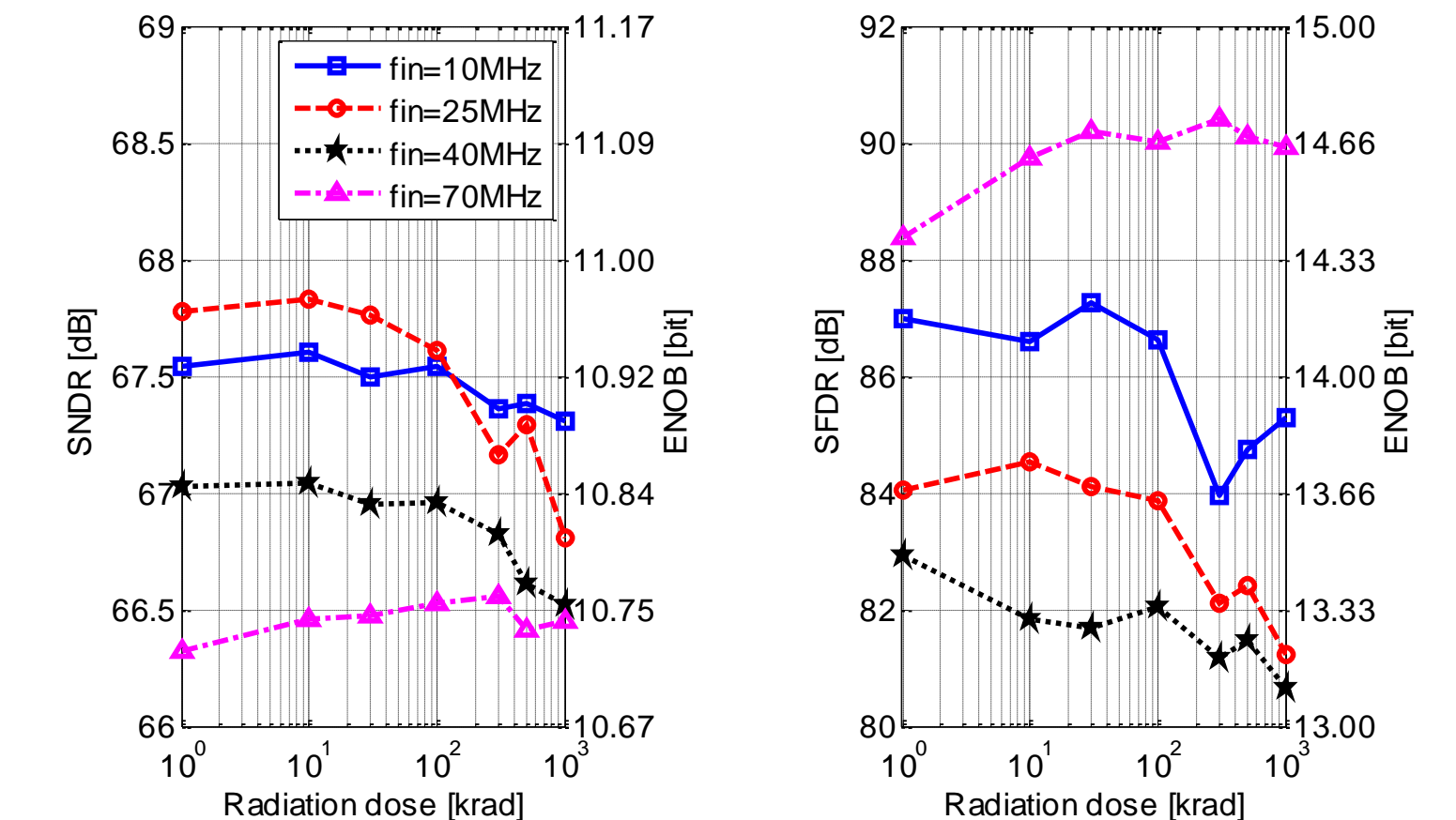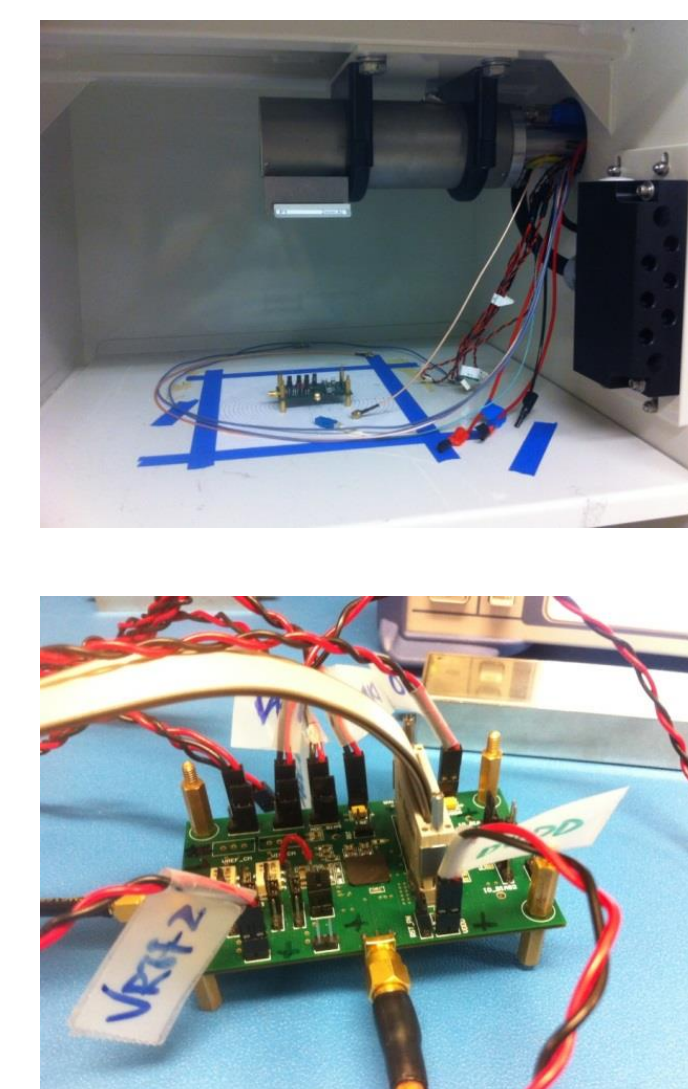
ADC Specs for Phase-II LAr Readout

- High resolution: **12-14 bits**
- High speed: **40-80 MS/s**
- Low power, low area
- Radiation-tolerant

- Pipelined ADC: High-gain residue amplifier hard to scale w/ process
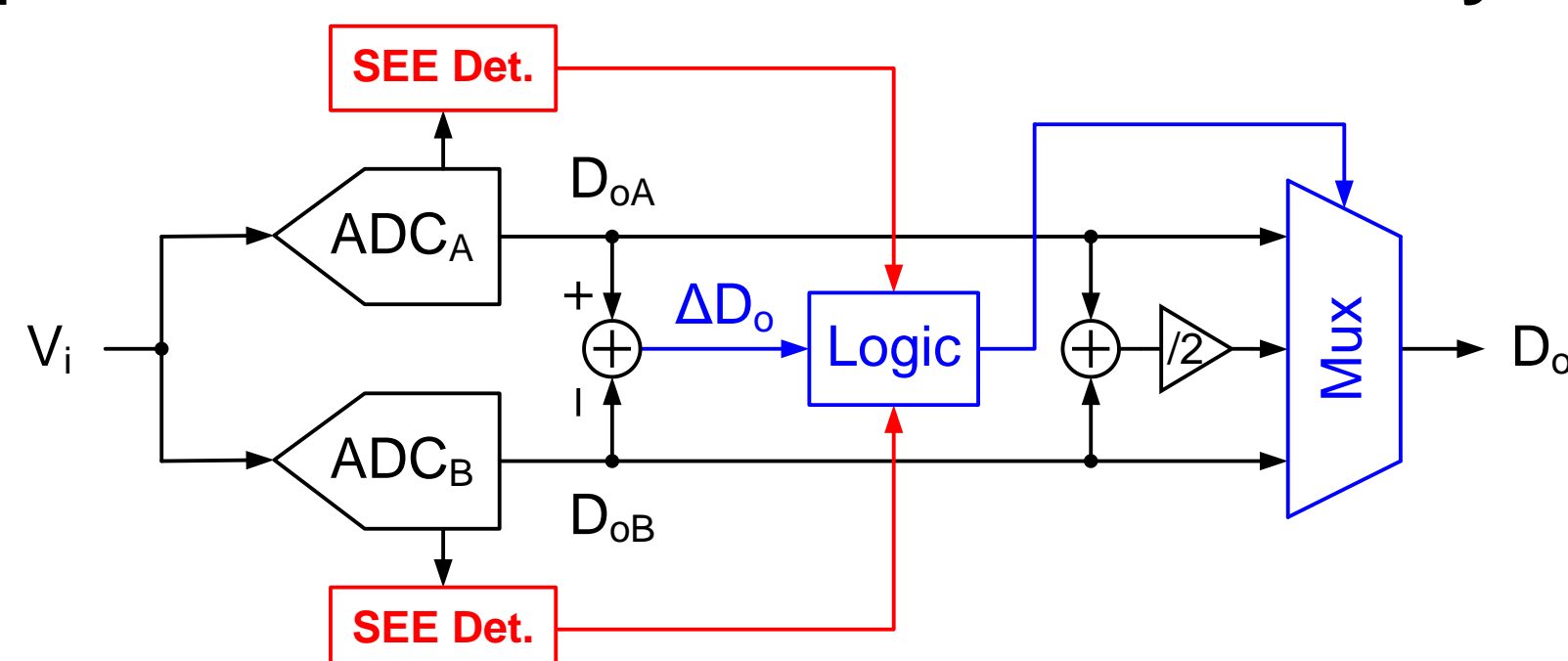- SAR ADC: low-power, low-area is a strong candidate for Phase-II

Previous TID Results (TWEPP'14)

- 12-bit, 160-MS/s ADC in 40-nm CMOS
- Total radiation dose up to 1 Mrad
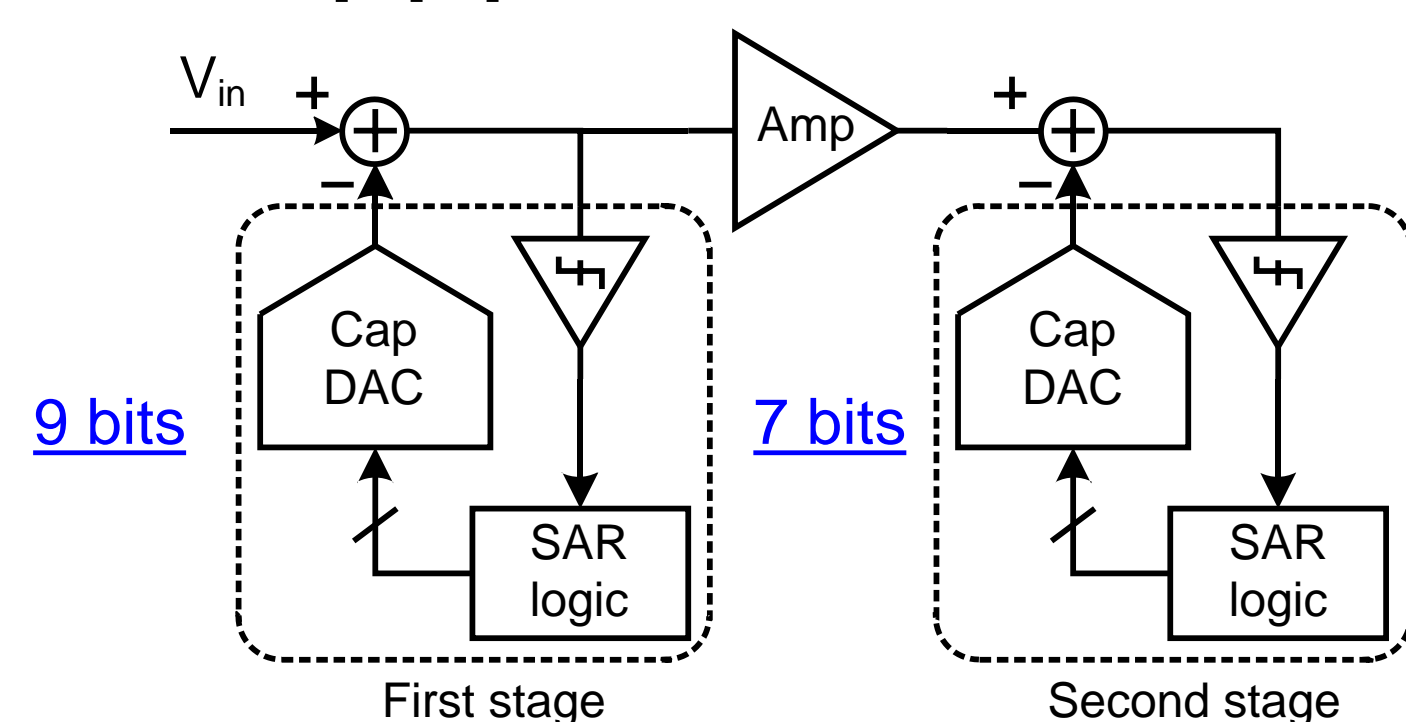- No significant degradation on SNDR, SFDR

Split SAR Architecture

- **Split ADC and architectural redundancy**

- If ΔD_o is large, choose the output of the ADC that is not hit
- A 3-dB SNR gain with normal operation (i.e., no hit)
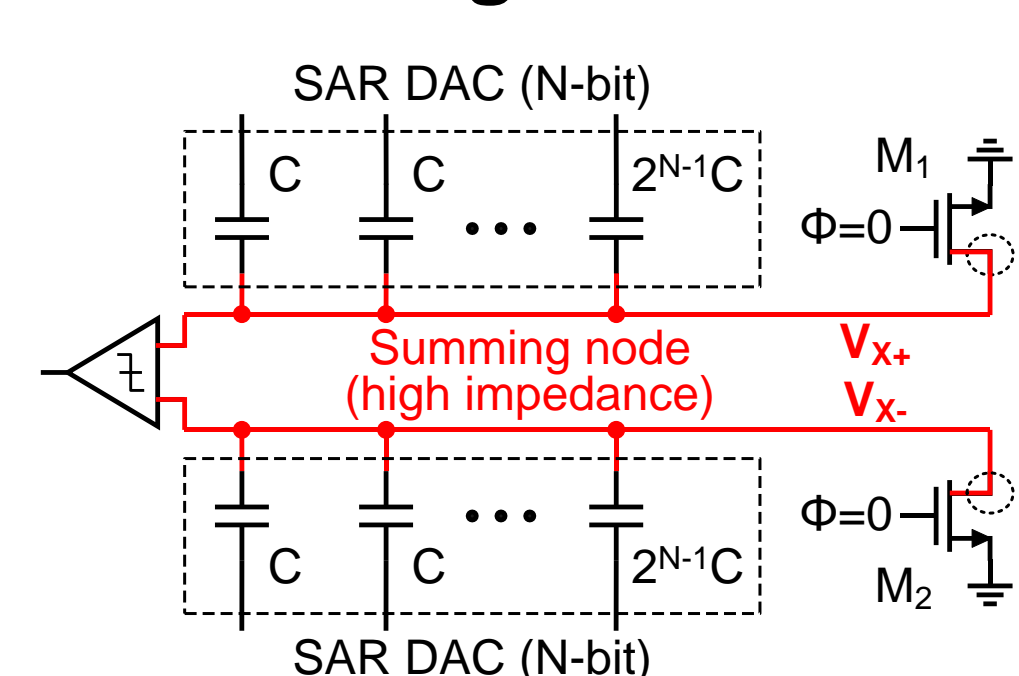
- **Two-step pipelined structure**

9 bits   7 bits

First stage   Second stage

- Fewer number of bits in first stage
- Amplifier removed from SAR Loop

→ **Fast Conversion**

Single-Event-Effect (SEE) Protection (*To be verified*)
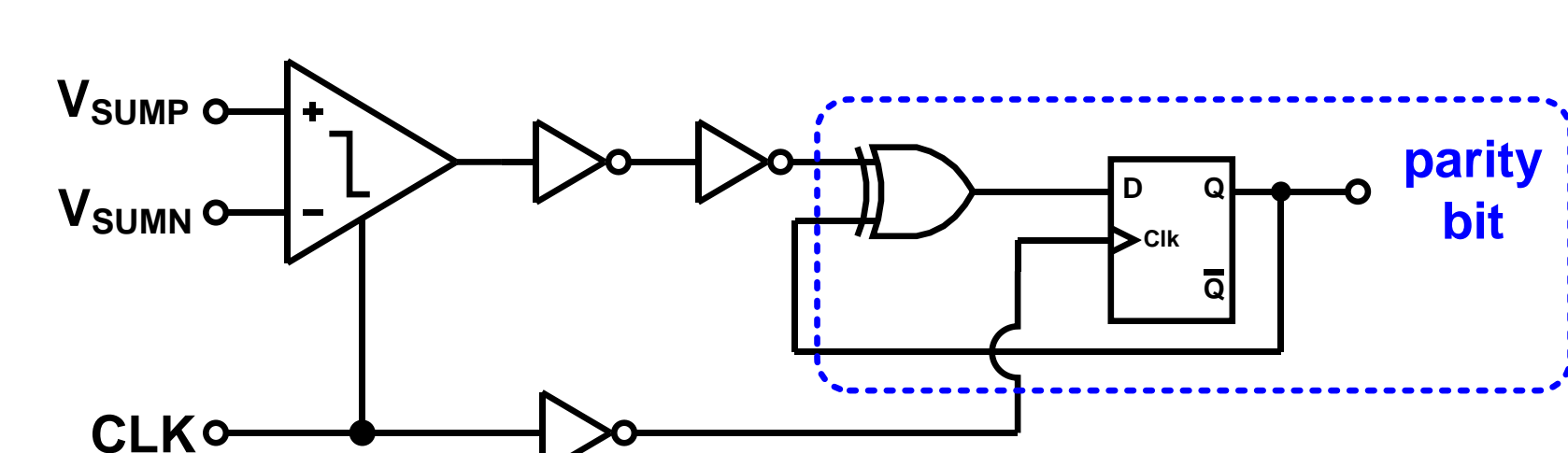
- **Summing-Node Hit Detection**

- SEE detector is formed by a pair of resistors, a "substrate-current amplifier", and some digital logics.

Example

For $Q_{SEE} = 100$ fC and $C_{TOT} = 2$ pF, $V_{err} = 50$ mV !

- **2nd-Stage SAR Error Detection**

  - If SEE error occurs, the extra bit will be identical to the LSB.

extra cap in 2nd-stage DAC

normal condition   normal condition w/ noise   SEE
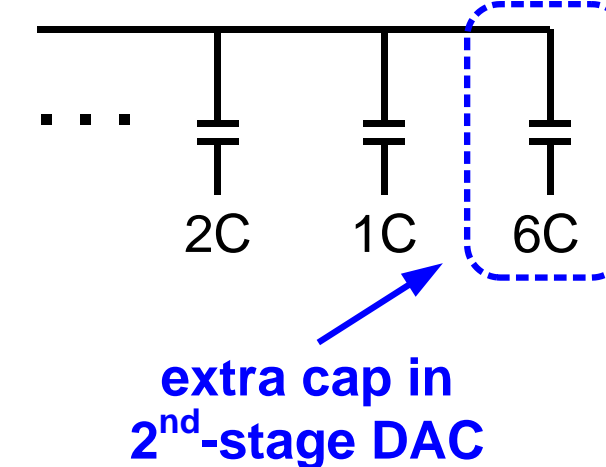
- **Data-Latch Error Detection**
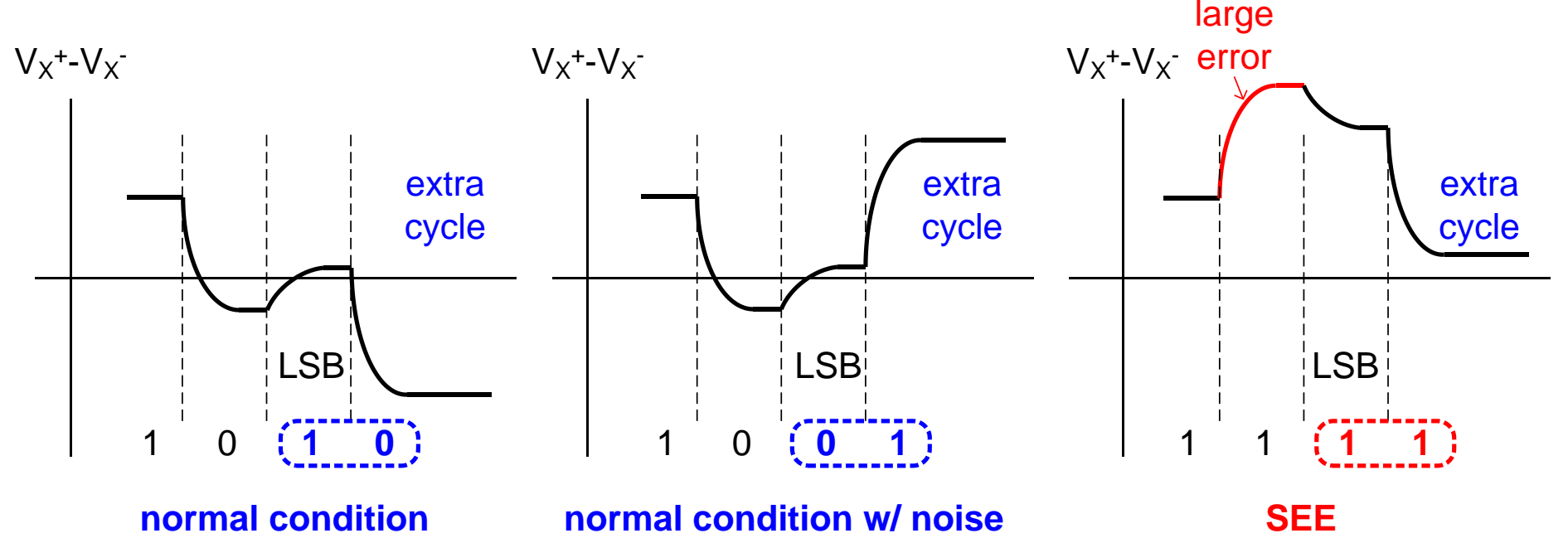
- Data latch not TMR-protected to reduce the comparator loading
- Data latches hit during residue amplification may cause error

Preliminary Electrical Measurement Results
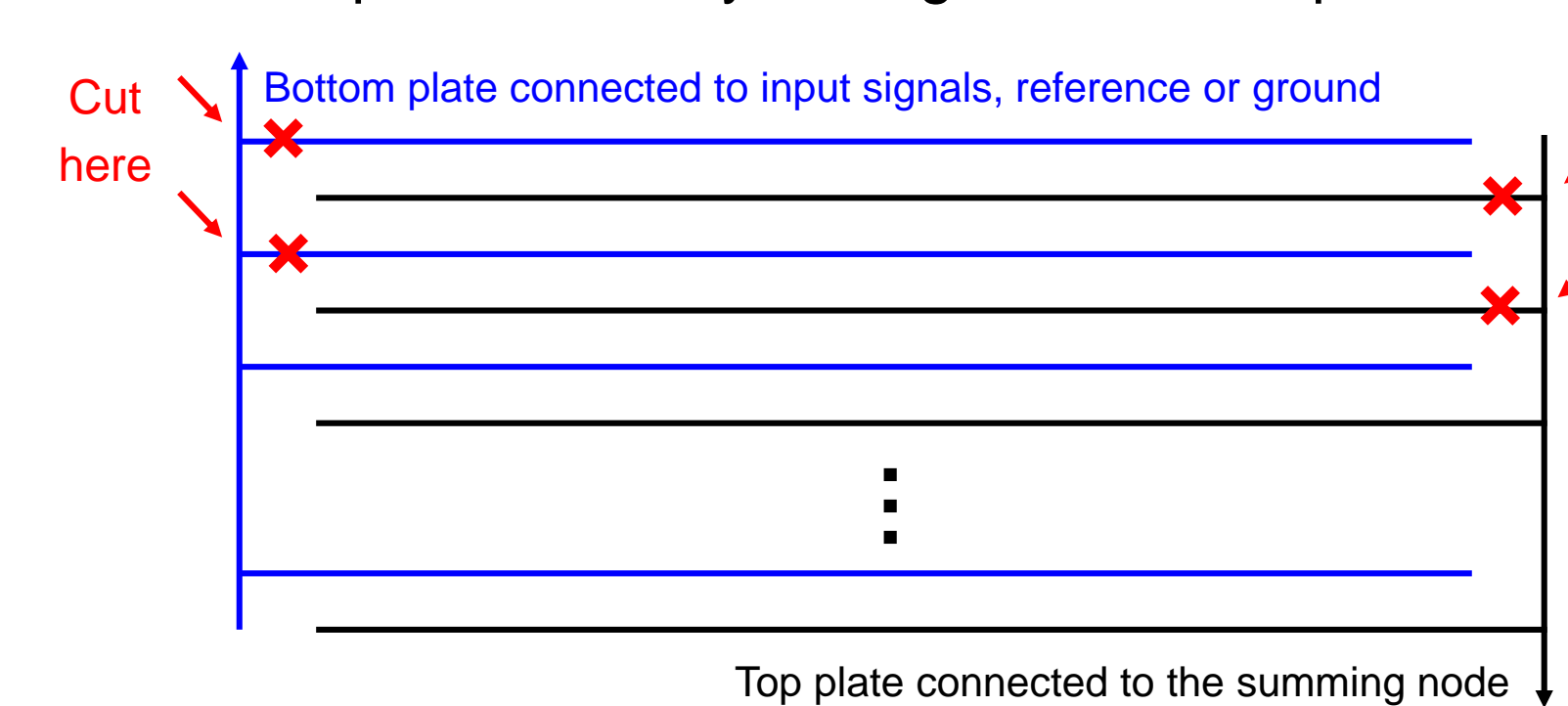
- **Super-radix-2 issue**

  Due to a layout error, the SAR capacitor array in the first stage suffered a large mismatch error, resulting in a super-binary weight for the most significant bit (MSB).

fs=40 MHz
fin=10.081MHz
Data length: 16k samples

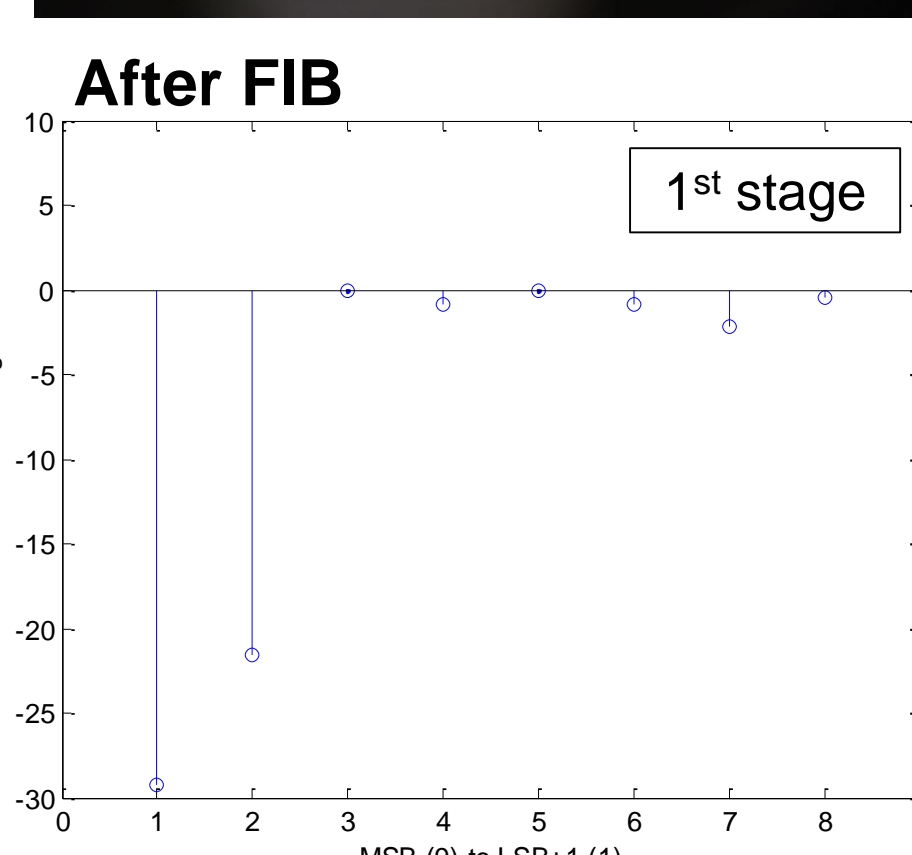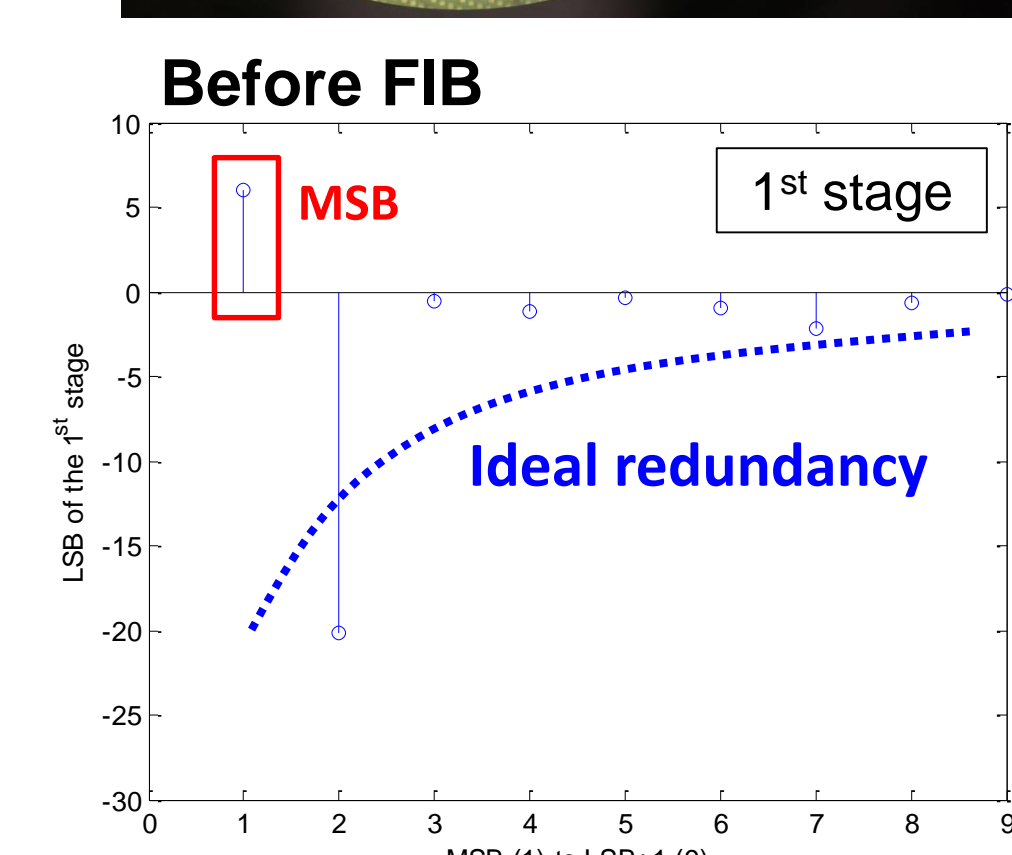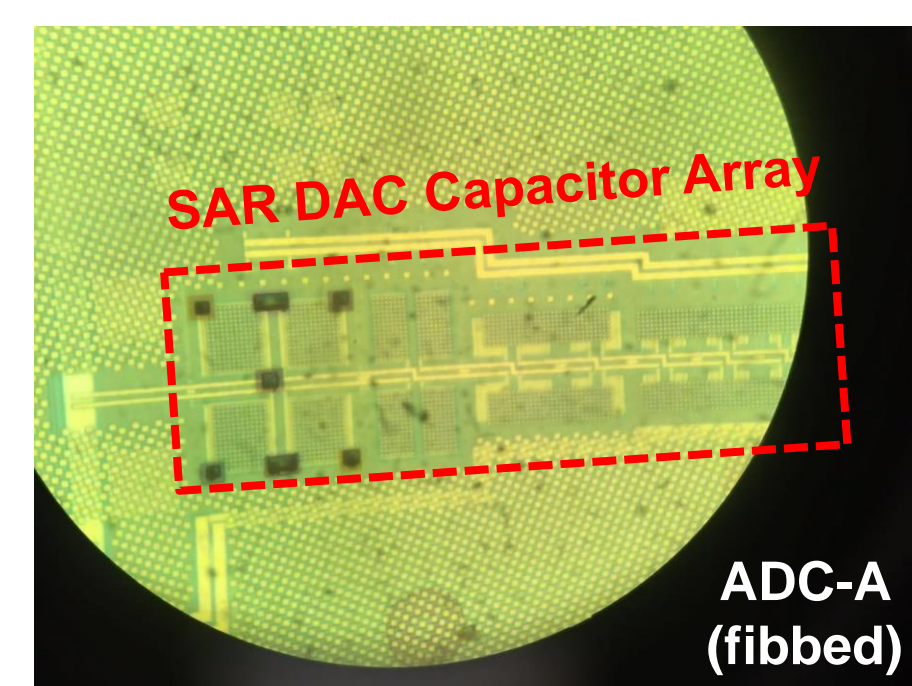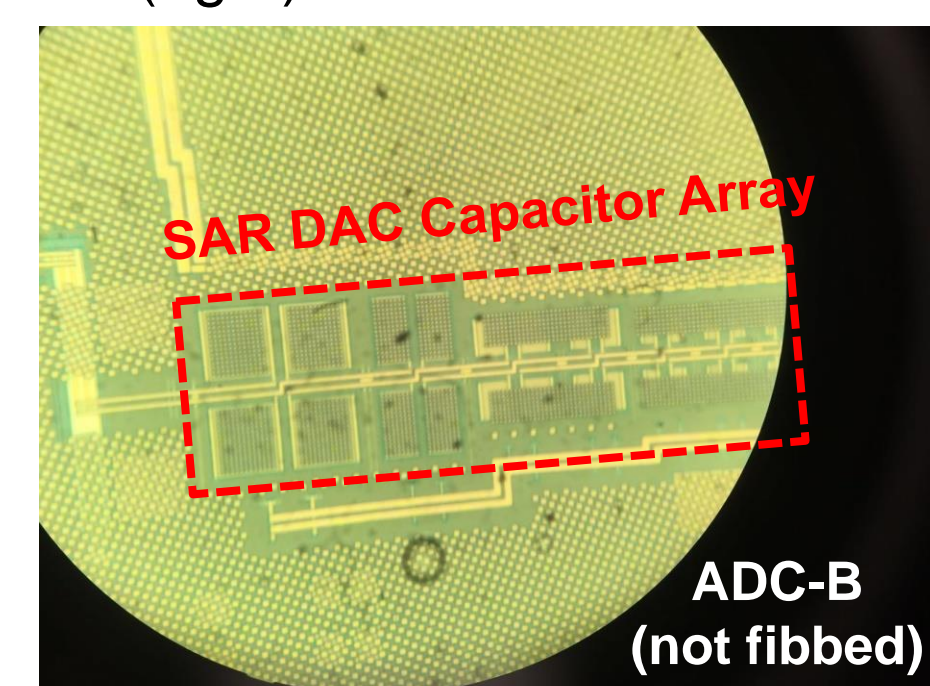SFDR = 82.77dB   SNDR = 64.22dB   ENOB = 10.38bits
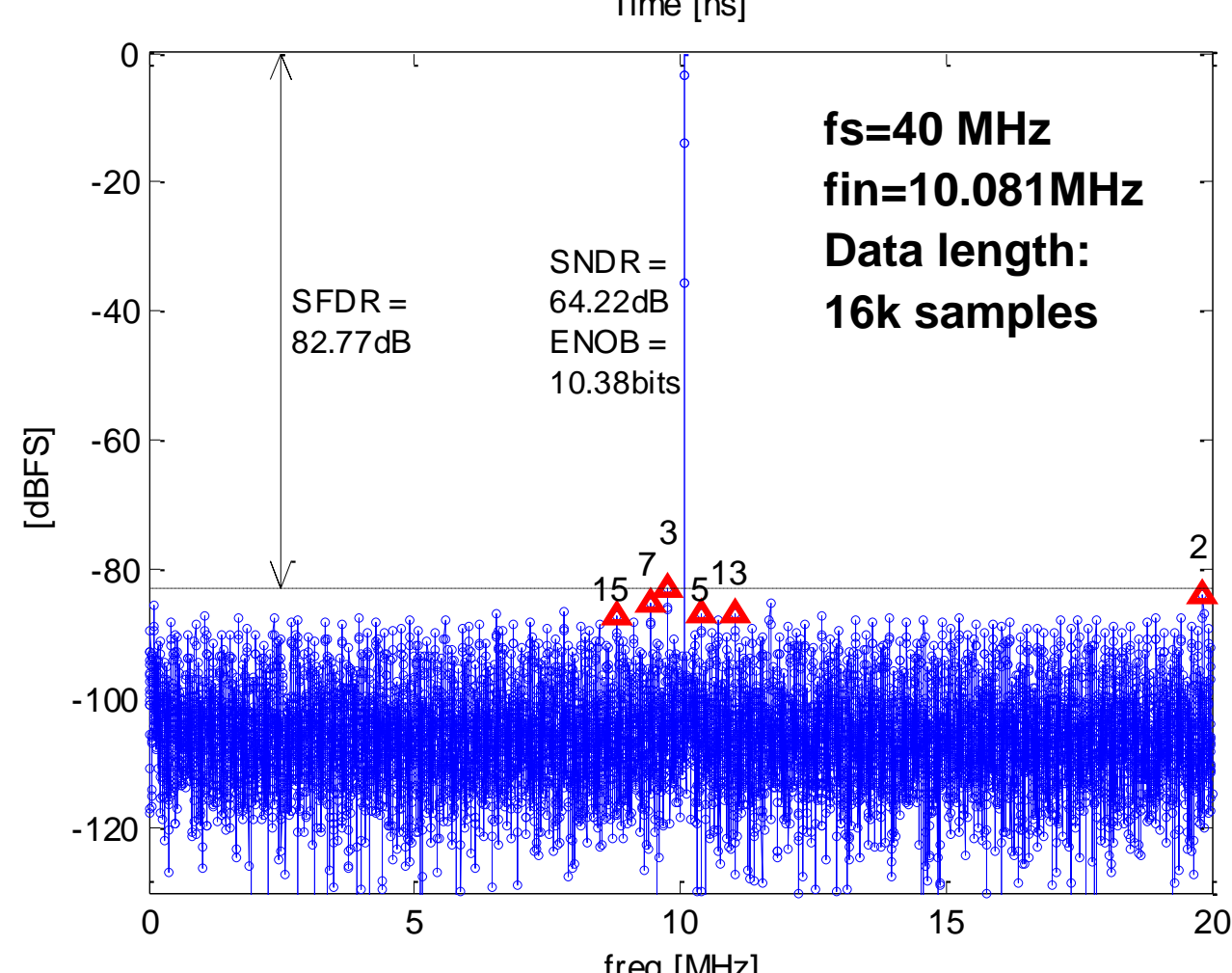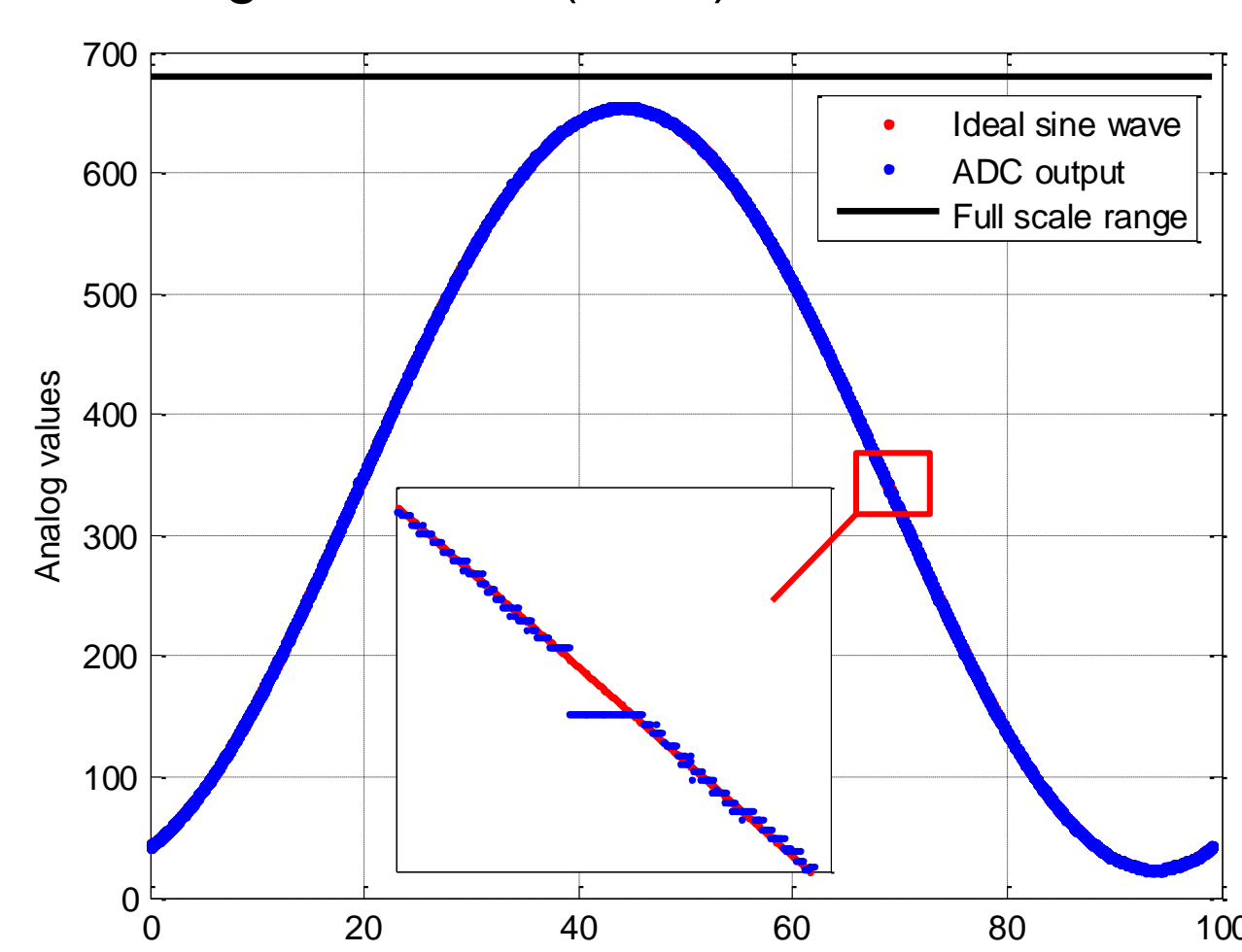
Missing detection levels is observed in the time domain waveform (upper plot) and SNDR and SFDR are limited to ~65 dB and ~80 dB respectively (lower FFT plot).

- **FIB Surgery**

  Focused ion beam (FIB) surgery is performed to reduce the MSB capacitor size by cutting the MOM capacitor fingers.
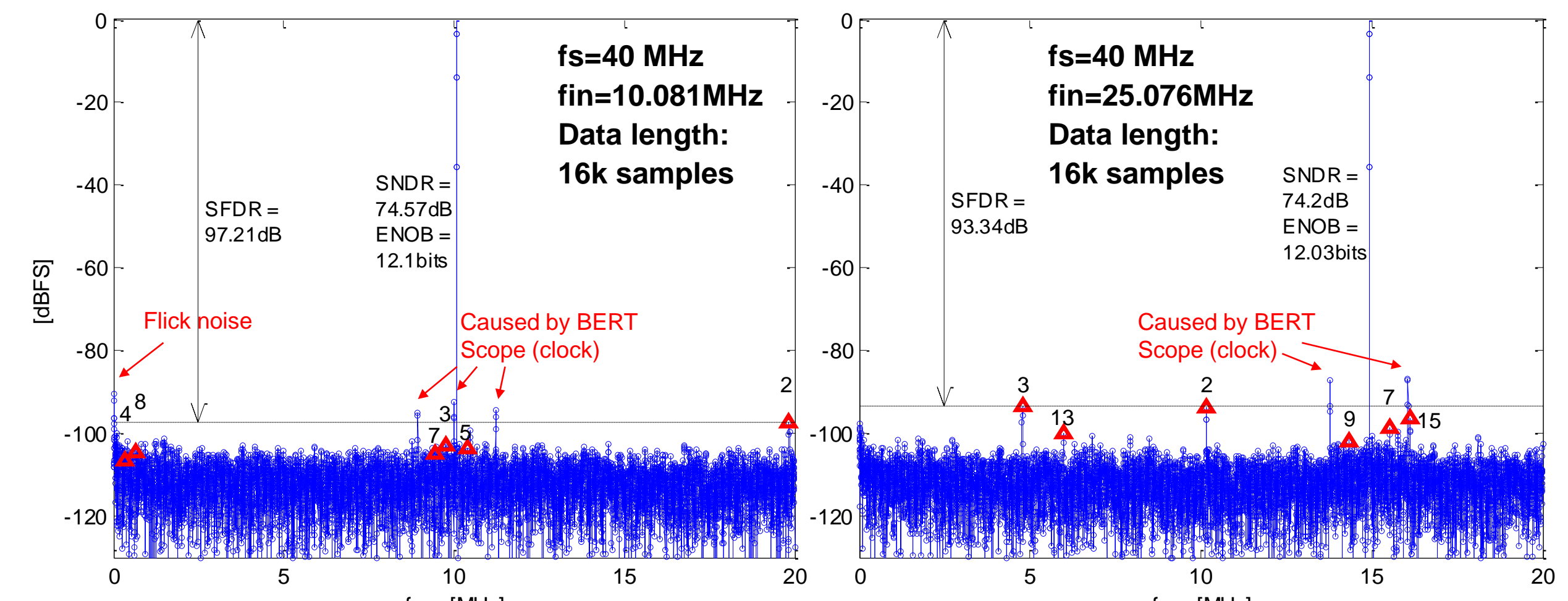

Bottom plate connected to input signals, reference or ground

Cut here   Cut here

Top plate connected to the summing node

Micrographs of 1st stage DAC of non-fibbed (left) and fibbed (right) sub-ADC

SAR DAC Capacitor Array   SAR DAC Capacitor Array

ADC-B (not fibbed)   ADC-A (fibbed)

**Before FIB**   **After FIB**

1st stage   MSB   Ideal redundancy   1st stage

$redundancy(y-axix) = w_i - \sum_{i+1}^{10} w_j - 1$ (w_i is the bit weight and $i = 1$-9.)

- **Single Channel Measured Performances**

fs=40 MHz
fin=10.081MHz
Data length: 16k samples

SFDR = 97.21dB   SNDR = 74.57dB   ENOB = 12.1bits

Flick noise   Caused by BERT Scope (clock)

fs=40 MHz
fin=25.076MHz
Data length: 16k samples

SFDR = 93.34dB   SNDR = 74.2dB   ENOB = 12.03bits

Caused by BERT Scope (clock)

- Over 97-dB SFDR and 74.5-dB SNDR (ENOB = 12.1 bits) are measured after FIB at 10 MHz input for a sample rate of 40 MSPS.

Dynamic Performance @ fs = 40 MHz

ENOB: 12 bits, 11 bits, 10 bits
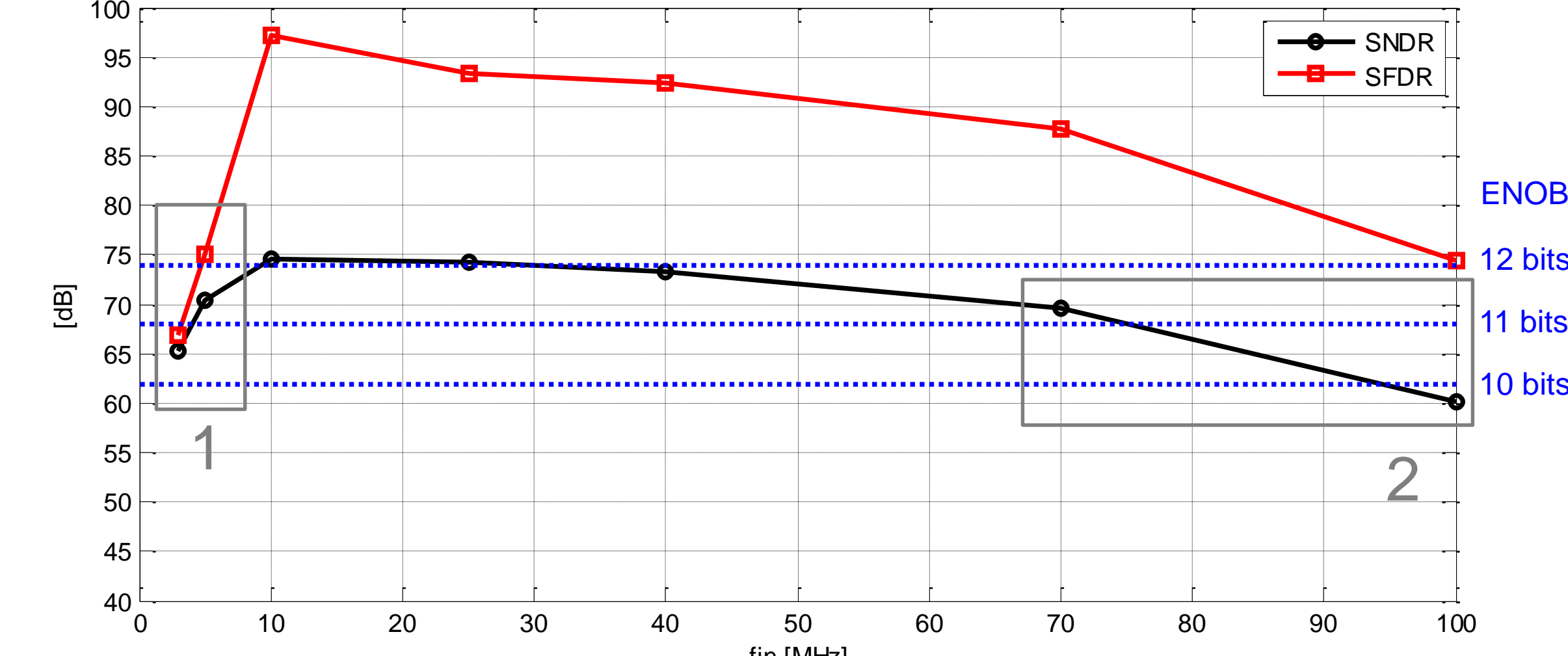
- Region 1: At low input frequency, it is likely limited by the input network on the PCB (balun etc.)
- Region 2: At high input frequency, it is likely limited by clock jitter.