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Preliminary Experimental Results of A 14-bit Split-SAR ADC for ATLAS LAr Phase-II Upgrade

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Preliminary experimental results of a 14-bit split-SAR ADC prototype implemented in 65-nm CMOS are reported. Inherent architectural redundancy and the newly proposed SEE-detection circuitry constitute two prominent features of this work for efficient SEE detection and correction (to be experimentally verified). With FIB and foreground calibration, the prototype ADC measured a 74.6-dB peak SNDR and a 97.2-dB SFDR at 40 MSPS for a single channel of the two split paths. More measurements and especially irradiation tests will be performed in the near future.

Summary

Based on the successful total ionizing dose (TID) testing results of our 12-bit, 160-MSPS SAR ADC in 40-nm CMOS (TWEPP'14), we proposed a 14-bit radiation-tolerant SAR ADC prototype in 65-nm CMOS for ATLAS LAr calorimeter Phase-II upgrade (TWEPP'15), which can also be employed by the CMS experiment. The proposed ADC adopts a split structure, in which two identical sub-ADCs sample the same input simultaneously but convert it independently. If the difference between the two outputs is below a certain threshold, then the final output will be formed by averaging the two conversion results (i.e., no area or power penalty). If the two outputs are largely different from each other, then the codes from a SEE detection circuit will be examined to identify which channel's output is intact (and used as the final result). The split architecture also enables a digital background calibration to correct the bit-weight errors within the two sub-ADCs. Several SEE detection circuits are also introduced to protect critical internal circuit nodes, such as the SAR summing nodes and the bit registers in the SAR loop. Besides, triple modular redundancy (TMR) is also employed to protect the digital circuits.

An initial electrical testing was performed on the prototype in a non-radiative environment. Due to a layout error, the SAR capacitor array in the first stage suffered a large mismatch error, resulting in a super-binary weight for the most significant bit (MSB). The ensuing missing decision levels around the midpoint of the conversion curve limited the measured SNDR and SFDR to 65 dB (equivalent to 10.5 ENOB) and 77 dB, respectively, for a sample rate of 40 MSPS. We performed focused ion beam (FIB) surgery to reduce the MSB capacitor size, which successfully restored the internal redundancy of the ADC. With FIB, one channel of the split-ADC measured a 74.6-dB peak SNDR (equivalent to 12.1 ENOB) and a 97.2-dB SFDR at 40 MSPS. More measurement and SEE results will be obtained soon.

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