Design of low power 12bit 40MSPS SAR ADCs with a redundancy algorithm and digital calibration for high dynamic range calorimeter readout

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Summary

✓Two SAR ADCs were developed in the context of the ATLAS experiment's Liquid Argon Calorimeter (LAr) readout upgrade for Phase-II of the LHC.
✓A fully differential architecture was used for both prototypes featuring **12bit 40MS/s** in a **CMOS 130nm 1P8M** process.
✓The core of the first prototype consumes **11mW** and its total area is **2.63mm².**
✓The core of the second prototype consumes **6.5mW** and its total area is **0.344mm².**
✓A generalized algorithm is used with a **redundancy** in **14 steps**, allowing a **digital correction** of the mismatch effects in the capacitor array.

The redundancy

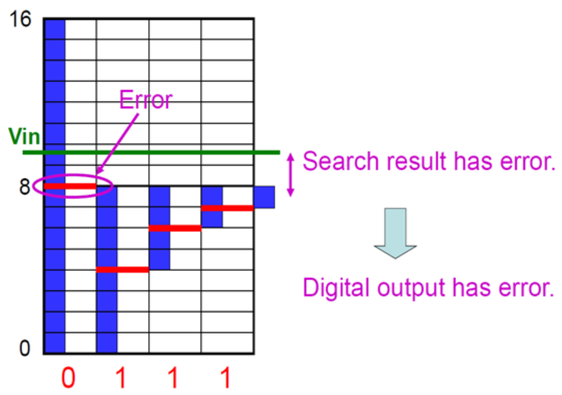

Fig 1: *Example of decision error due to incomplete DAC settling.*

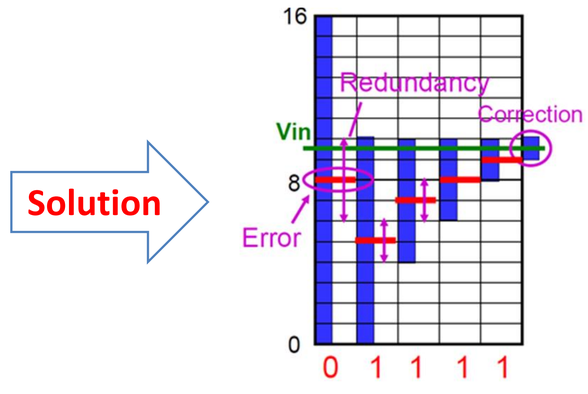

Fig 2: *Operation of a redundant search algorithm of a 4-bit 5-step SAR ADC.*

✓ Redundancy ➔ Robust toward *incomplete DAC settling* time issues.
➔ Possibility to calibrate the *capacitors mismatch*.
✓ During each conversion step (*k*), and to set the corresponding bit, the analog input voltage is compared to a reference voltage generated according to a redundancy vector ***p(k)***.

	Generalized non-binary search algorithm	
Step k	**p(k) [Prototype 1]**	**p(k) [Prototype 2]**
1	2048	2048
2	1012	840
3	456	480
4	252	300
5	144	180
6	80	120
7	46	60
8	26	30
9	14	16
10	8	8
11	4	6
12	2	4
13	2	2
14	1	1

Table 1. *A 12-BIT 14-STEP SAR ADC P(K) VALUES*

SAR ADCs architectures

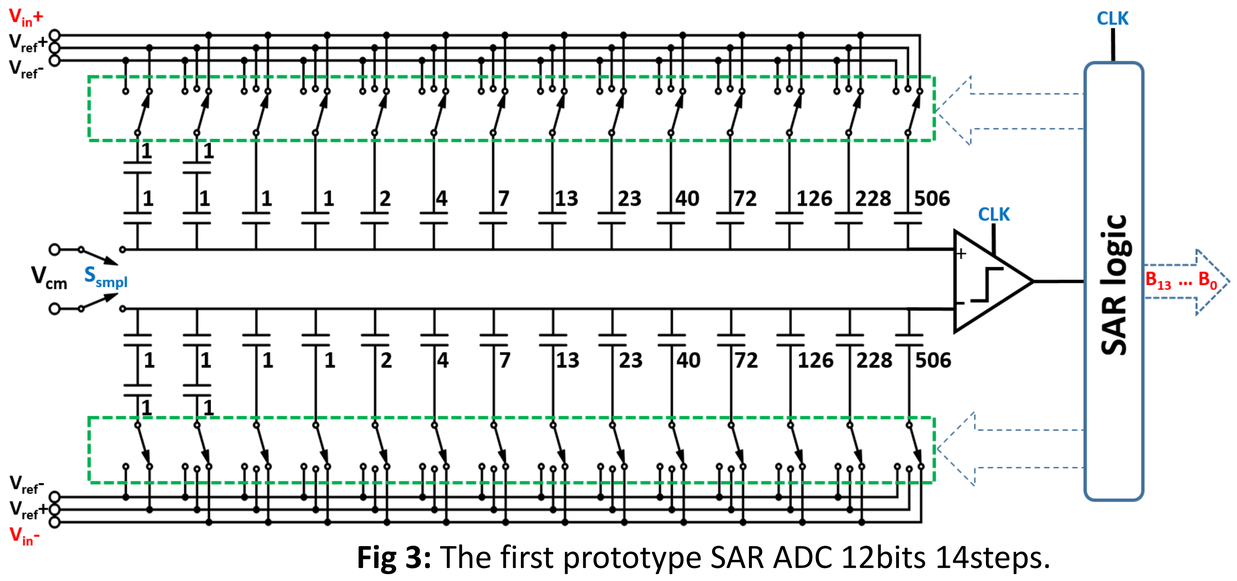

Fig 3: The first prototype SAR ADC 12bits 14steps.

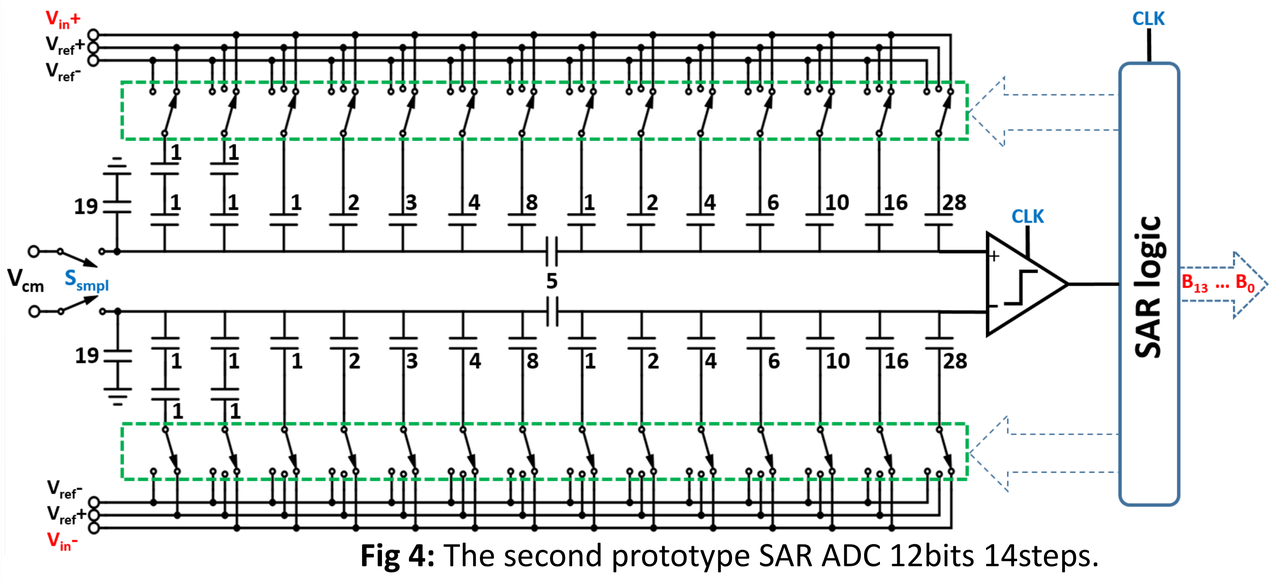

Fig 4: The second prototype SAR ADC 12bits 14steps.

✓ The redundancy algorithm **(14 steps)** is implemented in the analog part of the SAR ADCs **(12bits, 40MS/s)**.

✓ The **first prototype** uses a **one segment** capacitive DACs with only 2^{11}unit capacitors instead of 2^{12} for a conventional SAR.

➔ This design is robust regarding the parasitic capacitors issues.

✓ The **second prototype** uses a **two segments** capacitive DACs with an improvement of **12** in term of total capacitance.

➔ Reduced dynamic power consumption.

➔ Total area divided by **7,6**.

✓ A **monotonic** switching algorithm is used for these prototypes saving about **70%** of dynamic power consumption compared to conventional switching algorithm.

Test results

	Without digital calibration	With digital calibration
ENOB	**9,9b**	**10,7b**
INL	**+2.94/-4.74LSB**	**+1.28/-2.17LSB**

Table 2. *Test results of* ***the first prototype***

➢ These results were obtained at a limited speed (~8MS/s) because of some limitations of the first prototype and the testing board.

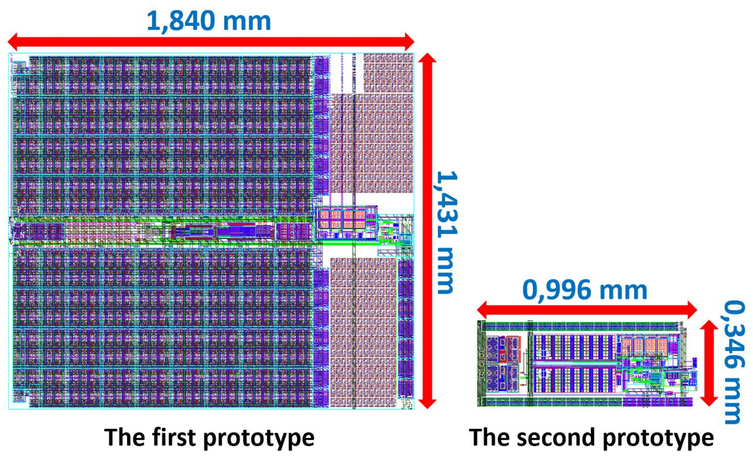

Fig 5: The layout of the two prototypes SAR ADC 12bits

➢ The **limitations** of the first prototype are :
- **Large area** for the core chip
- The difficulty to reach the 12bits resolution during the limited sampling time (2ns) due to the **total capacitors** (2^{11}units).

➢ The second prototype should overcome almost these limitations. Prototypes expected by March end.