Summary

- Two SAR ADCs were developed in the context of the ATLAS experiment’s Liquid Argon Calorimeter (LAr) readout upgrade for Phase-II of the LHC.
- A fully differential architecture was used for both prototypes featuring 12bit 40MS/s in a CMOS 130nm 1P8M process.
- The core of the first prototype consumes 11mW and its total area is 2.63mm².
- The core of the second prototype consumes 6.5mW and its total area is 0.344mm².
- A generalized algorithm is used with redundancy in 14 steps, allowing digital correction of the mismatch effects in the capacitor array.

The redundancy

- Redundancy ⇒ Robust toward incomplete DAC settling time issues.
- Possibility to calibrate the capacitors mismatch.
- During each conversion step \( k \), and to set the corresponding bit, the analog input voltage is compared to a reference voltage generated according to a redundancy vector \( p(k) \).

SAR ADCs architectures

- The redundancy algorithm (14 steps) is implemented in the analog part of the SAR ADCs (12bits, 40MS/s).
- The first prototype uses a one segment capacitive DACs with only \( 2^{11} \) unit capacitors instead of \( 2^{12} \) for a conventional SAR.
  ⇒ This design is robust regarding the parasitic capacitors issues.
- The second prototype uses a two segments capacitive DACs with an improvement of 12 in term of total capacitance.
  ⇒ Reduced dynamic power consumption.
  ⇒ Total area divided by 7.6.
- A monotonic switching algorithm is used for these prototypes saving about 70% of dynamic power consumption compared to conventional switching algorithm.

Test results

<table>
<thead>
<tr>
<th>ENOB</th>
<th>Without digital calibration</th>
<th>With digital calibration</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>9.9b</td>
<td>10.7b</td>
</tr>
<tr>
<td>INL</td>
<td>+2.94/-4.74LSB</td>
<td>+1.28/-2.17LSB</td>
</tr>
</tbody>
</table>

Table 2. Test results of the first prototype

- The limitations of the first prototype are:
  - Large area for the core chip
  - The difficulty to reach the 12bits resolution during the limited sampling time (2ns) due to the total capacitors (\( 2^{11} \)units).
- The second prototype should overcome almost these limitations. Prototypes expected by March end.