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Design of low power 12bit 40MSPS SAR ADCs with a redundancy algorithm and digital calibration for high dynamic range calorimeter readout

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We present two SAR ADCs using a generalized redundant search algorithm and offering the flexibility to relax the requirements on the DAC settling time. Two more bits of redundancy allow also a digital calibration, based on a code density analysis to compensate the capacitors mismatching effects. A monotonic switching algorithm is used for these prototypes saving about 70% of dynamic power consumption compared to conventional switching algorithm. A fully differential was used for both prototypes featuring 12bit 40MS/s in a CMOS 130nm 1P8M process.

Summary

For high dynamic calorimeter such as ATLAS-LArg, the design of a specific radiations hard ADC is one of the critical challenges. The resolution required is 12 or 14 bits depending on the number of gains in the shaper stages. The speed could be 40MS/s or 80MS/s depending on pile up noise issues. In these configurations, pipelined architecture was widely used during the last years. But following the scaling of CMOS process, SAR architecture appears more suitable because it presents a lower power dissipation feature. But the main limitations to deal with are the DAC settling time and the capacitors mismatching issue. This paper presents two SAR ADCs with a generalized redundant search algorithm to relax the requirements on the DAC settling time and also allowing a digital calibration to compensate the capacitors mismatching effects. The first prototype uses a one segment capacitive DACs with a reduced capacitors array (only 2^11unit capacitors to reach 12 bits resolution instead of 2^12 for a conventional SAR). This single segment architecture makes the design robust regarding the parasitic capacitors issues. However it leads to a large area circuit, despite the reduced capacitors array configuration. A bottom plate sampling scheme is used to reduce the charge injection effects. The typical sampling time, following our simulations, was about 2ns. A multi-stages high speed comparator was designed including two static preamplifiers and a final dynamic latch stage. The core of the first prototype consumes 11mW and his total area is 2.63mm2. The test results of this prototype features 9.9bit ENOB, and +2.94/-4.74LSB INL before calibration. But after calibration the INL is improved to +1.28/-2.17LSB and the ADC achieves 10.7bit ENOB. A comparison of these results with those from a reference COT ADC on the same testing board, points out that this ENOB corresponds to some limitations of our testing board. Another improved board was designed and updated results are expected very soon.
Some limitations of the first prototype were the area for the core chip, and also the difficulty to reach the 12bits resolution during the limited sampling time (2ns) with the total capacitors (2^11units). Therefore a second prototype was designed with two segments DAC architecture. Comparing the core layout of these 2 prototypes, we found an improvement of 12 in term of reduced total capacitance. The core of the second prototype consumes 6.5mW and its total area is 0.344mm2. But the segmented design is more sensitive to parasitic capacitors, hence a very careful layout has been done do deal with. A novel charge pump reference buffer is included. This second prototype is really suitable for a next multichannel circuit. The design is fully differential featuring also 12bits 40MS/s in a CMOS 130nm 1P8M process. The redundancy and digital calibra-

tion possibilities are similar to the first prototype. This second prototype was sent to production and should be delivered by March end.

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