FAST TRACKER

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on behalf of ATLAS collaboration and ATLAS Fast-TracKer upgrade project

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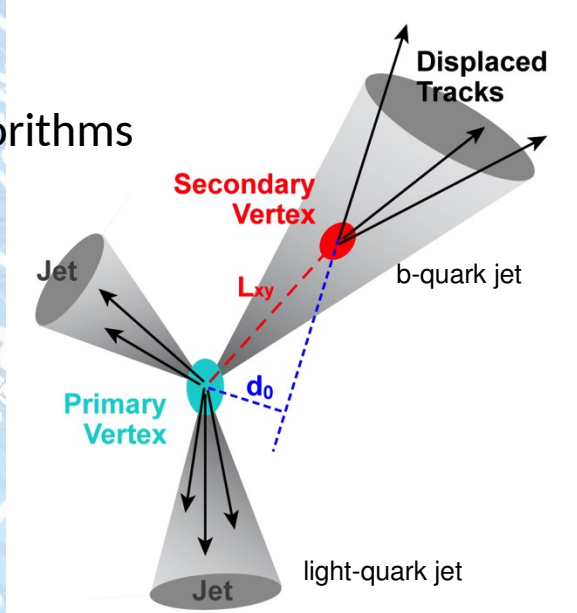
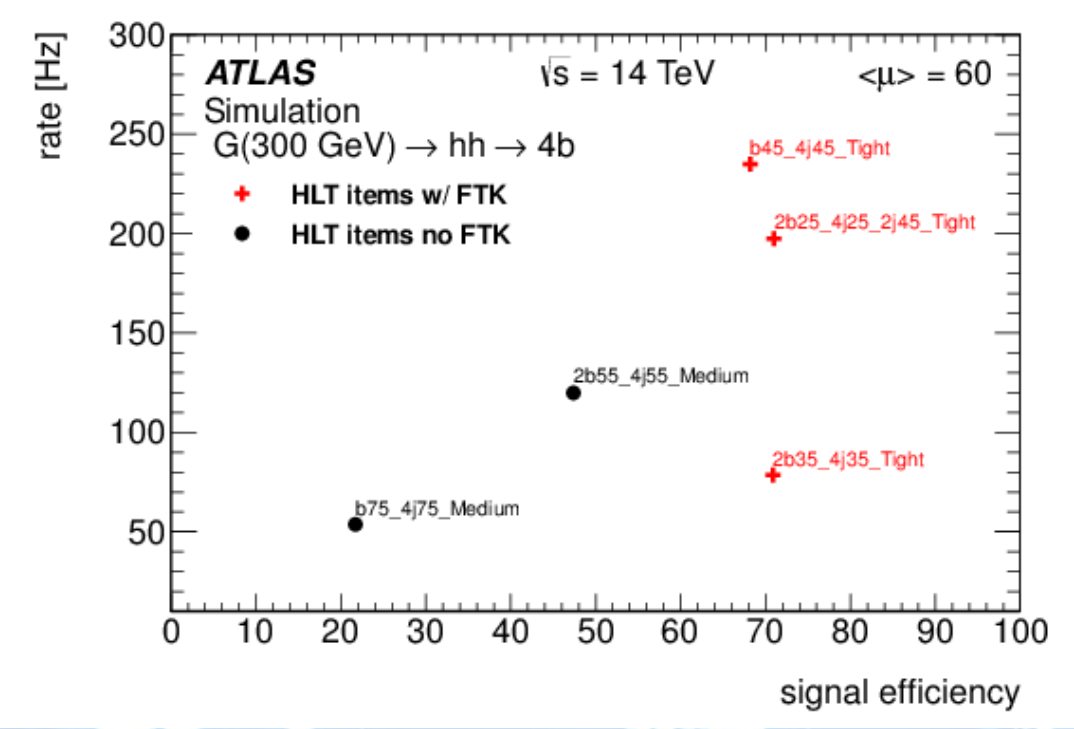
ACES 2016

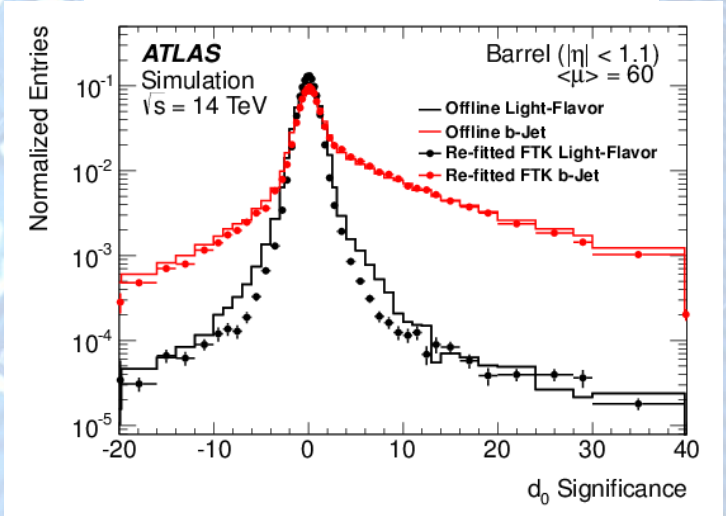
Physics motivations examples

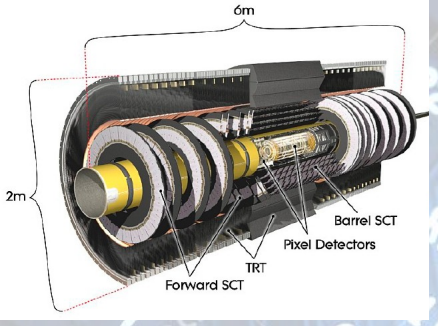
FTK performance ATL-COM-DAQ-2014-011

- Exploit full-scan FTK tracking in HLT
- Tau identification and Jet/MET pileup correction
- Primary vertex reconstruction for pileup resilient algorithms
- Can improve efficiency for multi-b jet signals
  - 3x efficiency improvements for ~fixed rate

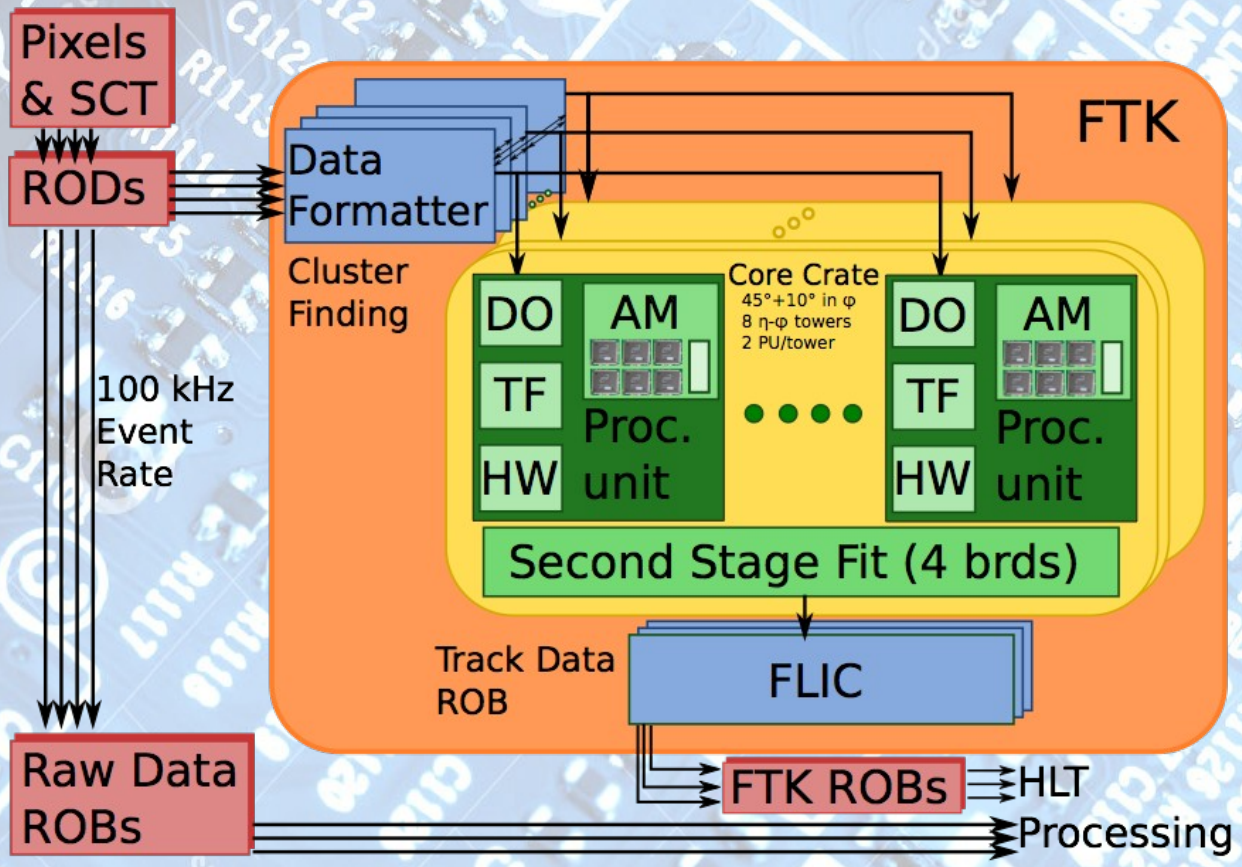








FTK architecture



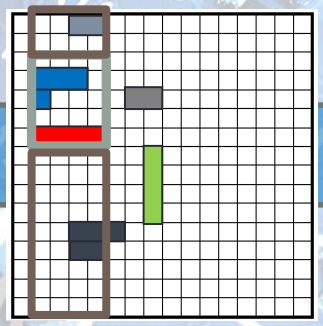
The Fast Tracker feeds HLT with full scan tracking at 100 kHz $p_T > 1$ GeV

Combination of ATCA and VME cards

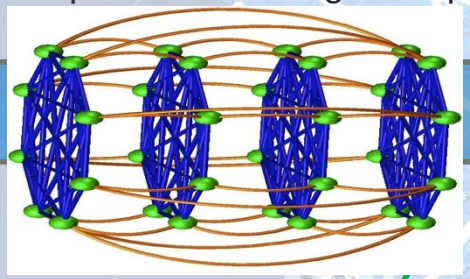
8192 ASICs (65nm)
1 billion patterns
~2000 FPGAs
Thousands of I/O links up to 10 Gb/s

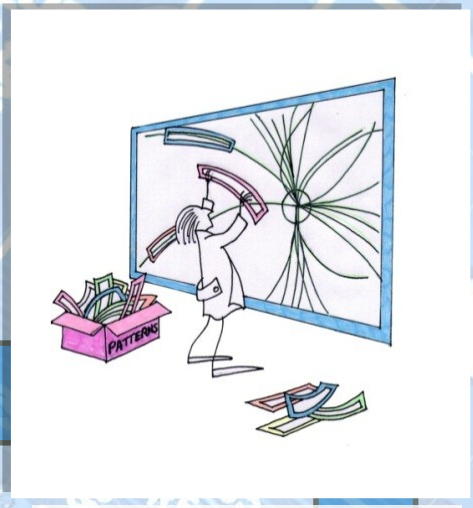
FTK Main Algorithms

Custom pixel clustering algorithm on FPGAs

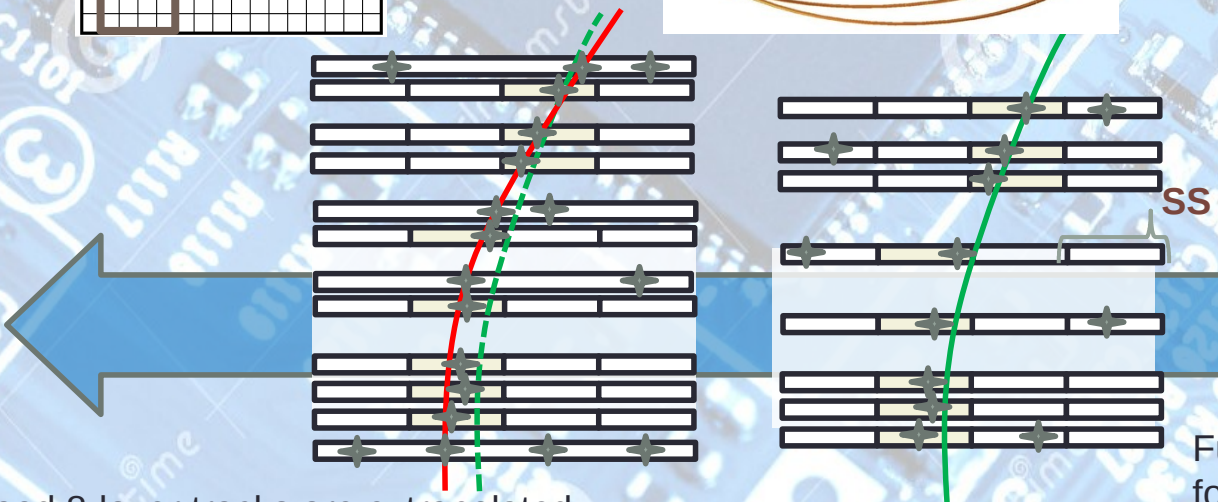


The data is geometrically distributed to the processing units and compared to existing track patterns.





AM Pattern matching 8 layers: 3 pixels + 5 micro-strips.
Hits compared at reduced resolution.



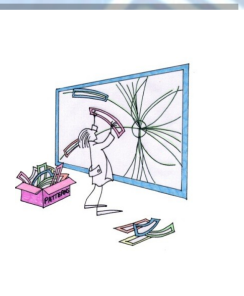
Good 8-layer tracks are extrapolated to additional layers, improving track quality

$$p_i = \sum_j C_{ij} \cdot x_j + q_i$$

Full hits precision retrieved for good roads.
Fits reduced to scalar products.

System Components

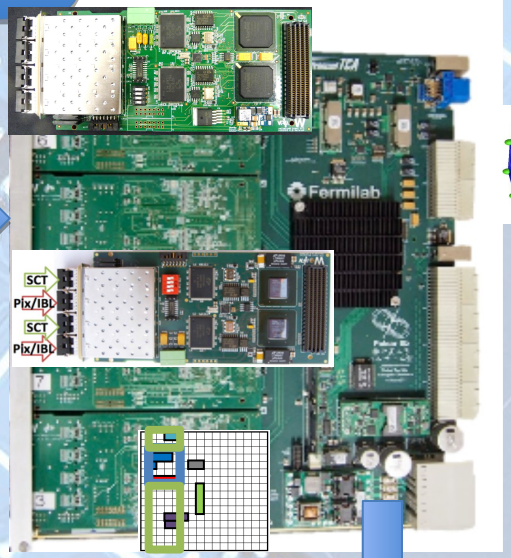
~8000 ASICs (65nm)
~2000 FPGAs
Thousands of I/O links up to 10 Gb/s

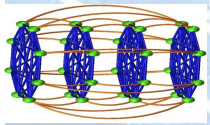


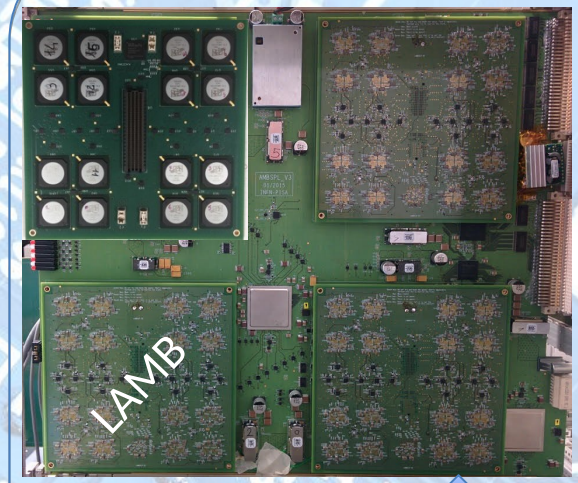
128 PUs
128 AMB

128 IM + 32 DF

DF-DF conn.





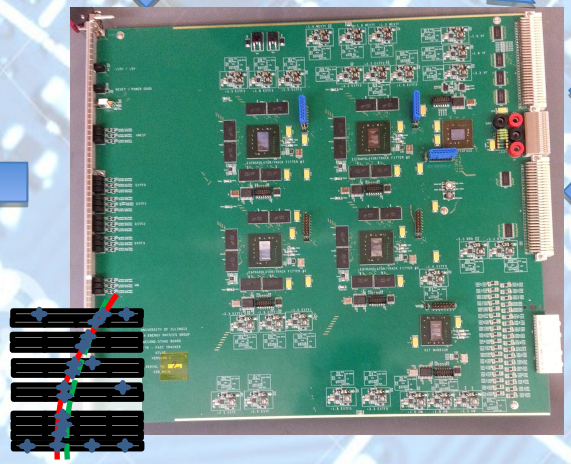


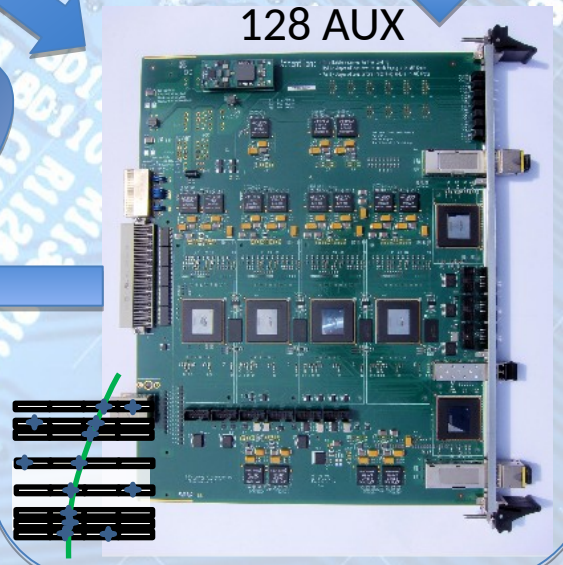
SSB-SSB conn.

128 AUX

2 FLIC

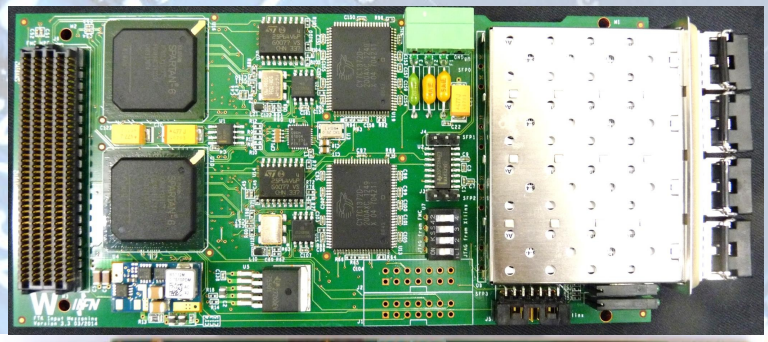
32 SSB

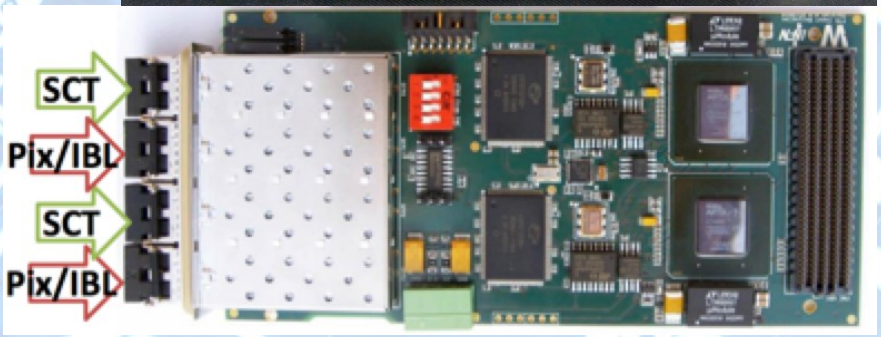




FTK input system (ATCA)

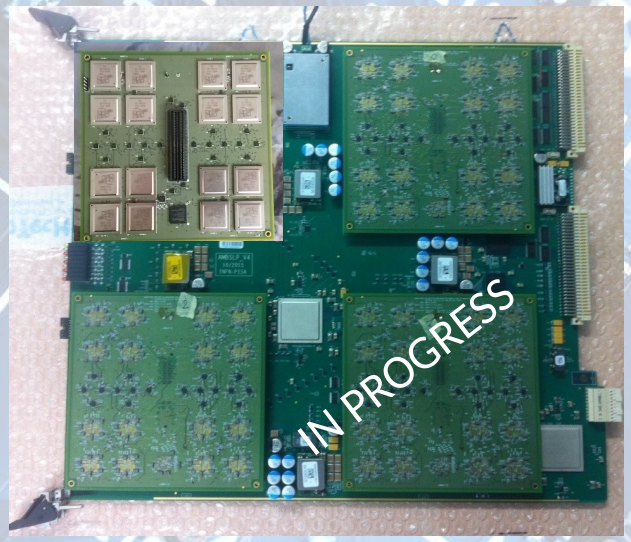
- IM cards: Waseda + Frascati
  - Perform clustering
  - Interface with Inner Detector
  - Receive 380 input S-Links
- 83/64 IM Artix7 produced
- 80/64 IM Spartan6 produced
- First cards used at point 1 since mid-2015





- DF cards: Stanford + Chicago (+FNAL)
  - Distribute data to processing units
  - Map readout to processing towers
  - Allows for overlap
  - Uses LAPP IPMC card
- 33/32 DFs produced
  - More spares becoming available

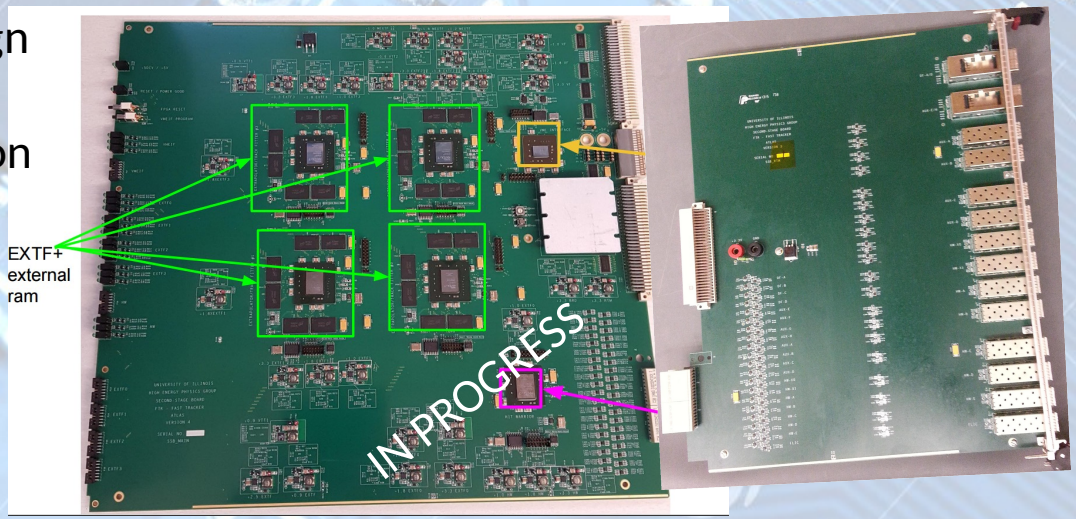
FTK core processing (VME)



- AUX cards: Chicago
  - Send clusters to AM board
  - On the fly data organization
  - 8-layer track fitting
  - partial duplicate removal
- 20/16 produced

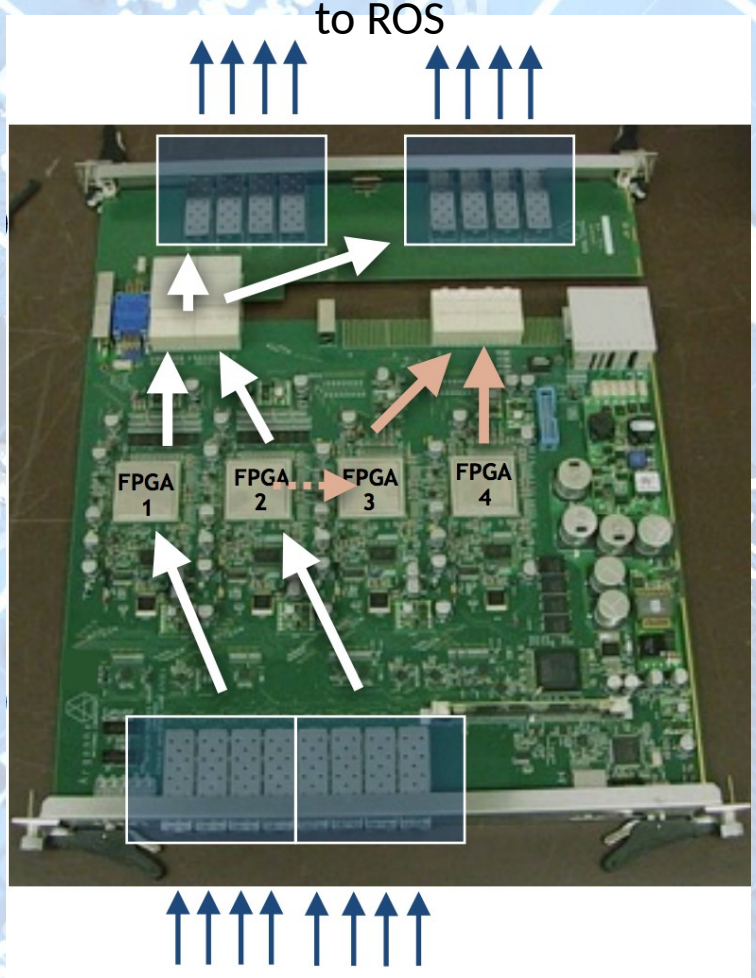
- AMB cards Pisa
  - AM based pattern recognition
  - PRR in March

- SSB cards: Illinois Urbana Champaign
  - On the fly data organization
  - 8-layer to 12-layer extrapolation
  - 12-layer track fitting
  - global duplicate removal
- 10/8 RTMs being assembled
- 2/8 SSB main cards assembled
  - Under test
  - Remaining 8 assembled next



FTK to HLT interface (ATCA)

- FLIC: Argonne
  - Interfaces FTK with the rest of TDAQ
  - Formats data for HLT processing
  - Local to global hit position conversion
  - Uses LAPP IPMC card
- 3/2 cards produced

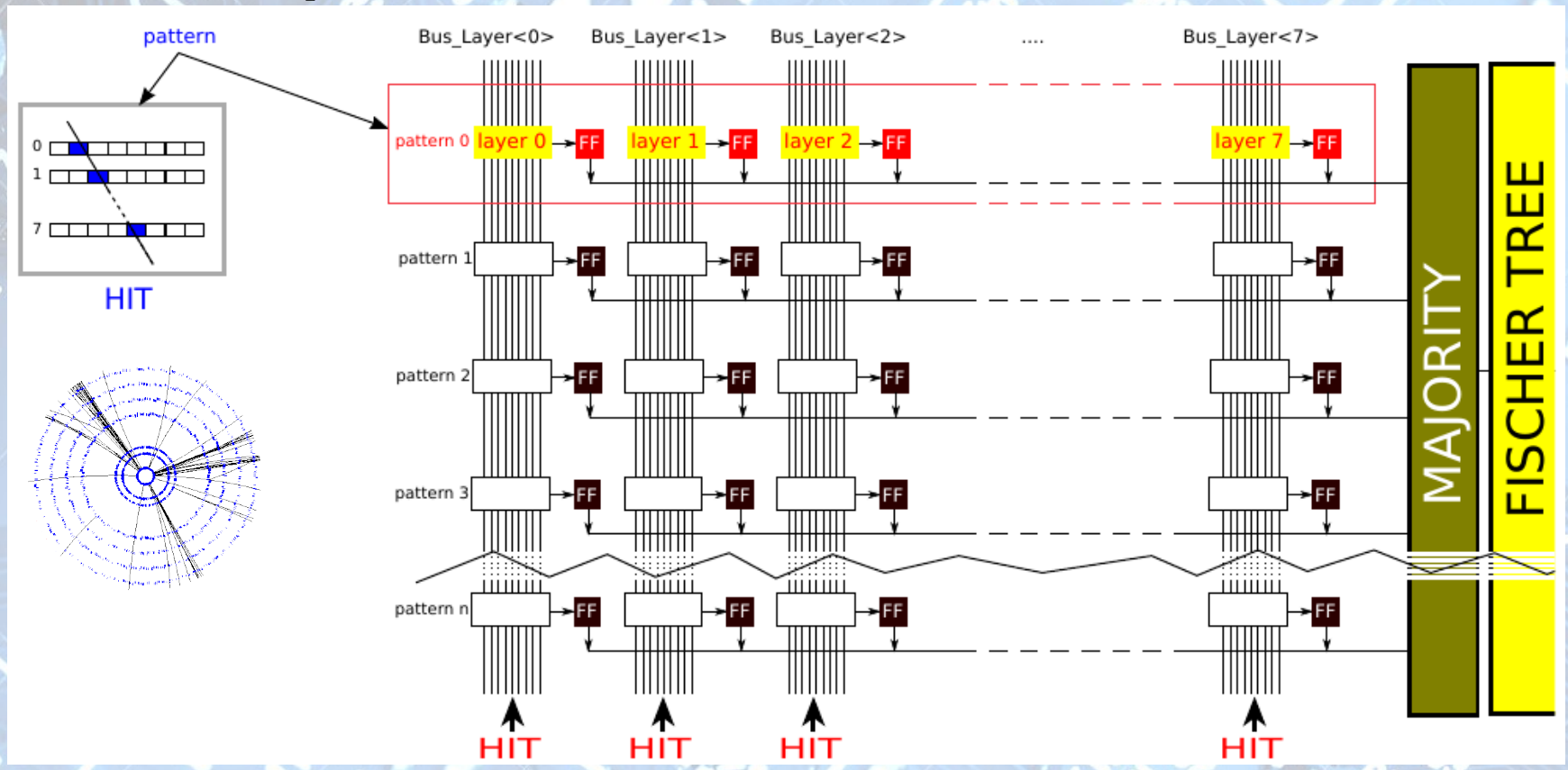


FTK HW production status

Board Name	2016 cards /AM06 needed	Produced & tested	Production status
IM Spartan 6	64	80	full
IM Artix 7	64	83	full
Data Formatter	32	35	full
AUX	16	20	all for 2016
AM06 chip	1024	119	In production
AMB	16		PRR in March
SSB	8		In production
FLIC	2	3	full

12.5% processing and barrel only coverage in 2016

AMChip Architecture



- 1 Flip-flop (FF) for each layer stores layer matches
- All patterns are compared in parallel with incoming data (HIT) pattern matching is finished as soon as all data is loaded (low latency)
- Fast pattern matching and flexible input
- the AM readout is based on a modified Fischer Tree[1]

[1] P. Fischer NIM A461 (2001) 499-504

AMChip 06 Memory cell architecture

- Based on 6T SRAM memory cell
- Connected to a XOR boolean function
- Comparison of bit lines and memory content is done through combinatorial network

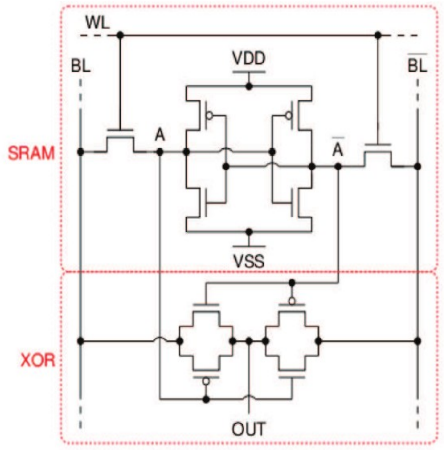


Fig. 6. Schematic diagram of the XOR-based single-bit CAM cell.

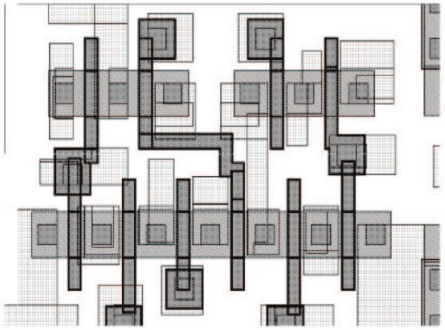


Fig. 7. Layout of the XOR-based CAM cell in 65 nm CMOS technology.

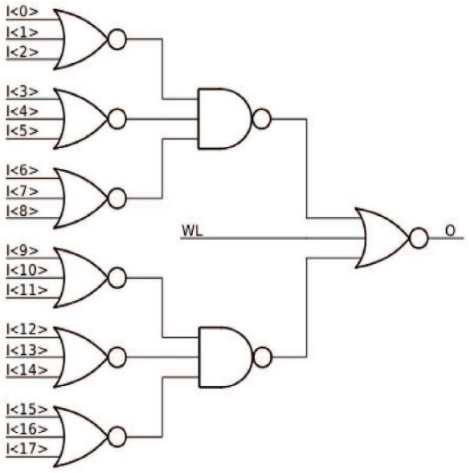
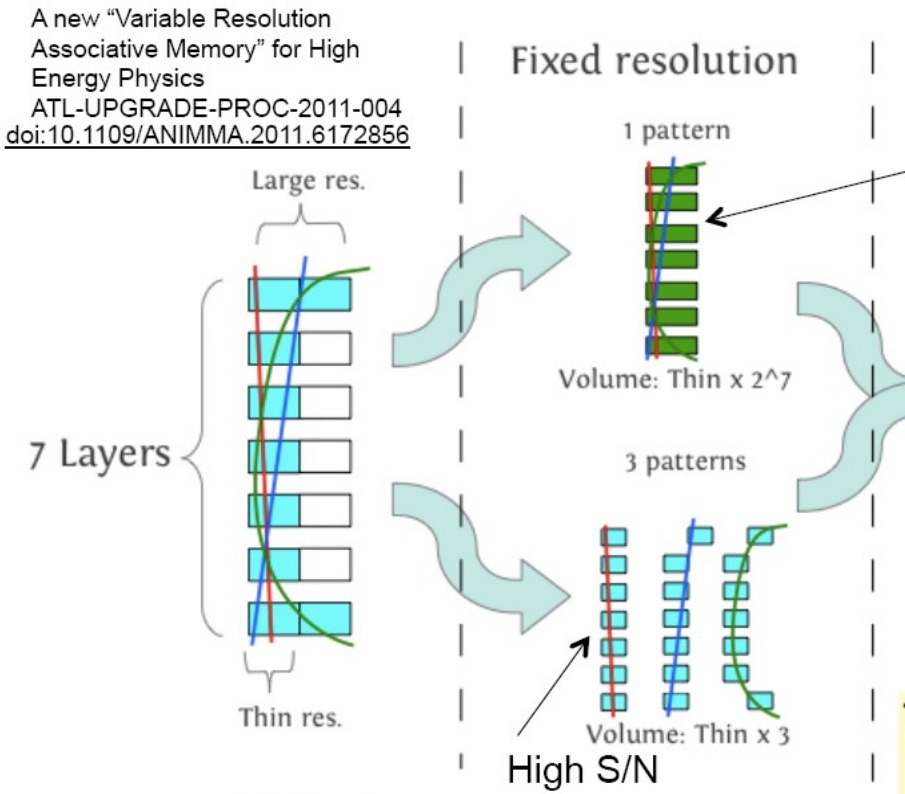


Fig. 8. Schematic diagram of the 18-bit NOR logic gate.

Variable pattern matching resolution

A new "Variable Resolution Associative Memory" for High Energy Physics
ATL-UPGRADE-PROC-2011-004
doi:10.1109/ANIMMA.2011.6172856

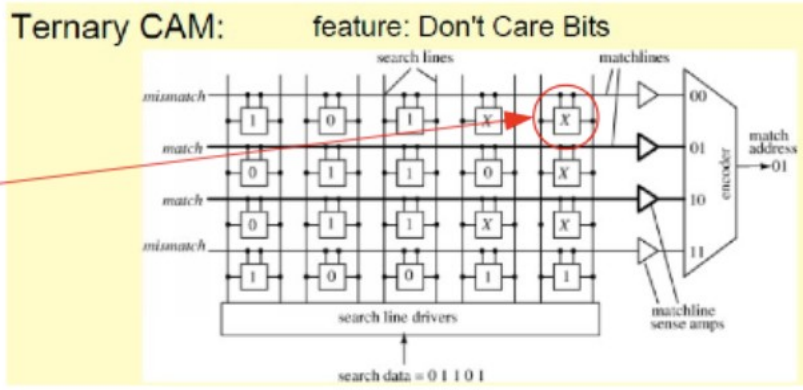


Good rejection and occupy only one pattern location.

Per-pattern choice of optimal resolution.

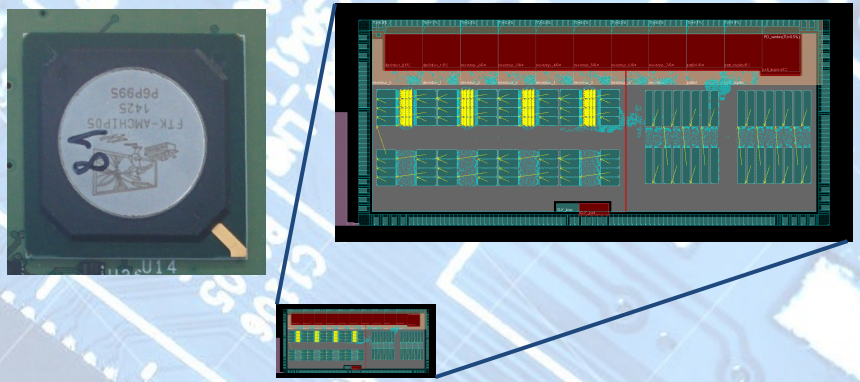
We can use **don't care** on the least significant bit when we want to match the **pattern layer @ Large resolution** or use all the bits to match it **@ Thin resolution**

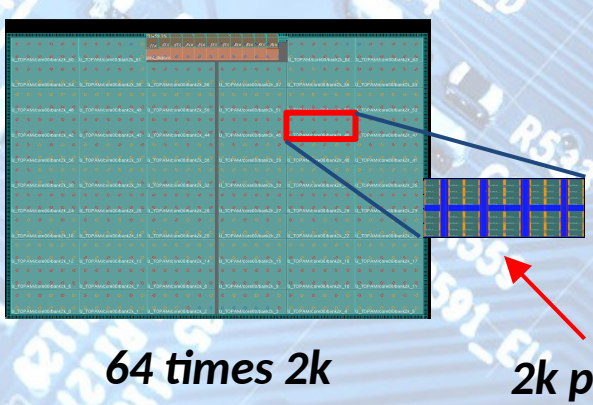
Coincidence window is programmable layer by layer and pattern by pattern



From AM05 to AM06

- AM05 last small area prototype (2015)
  - 65nm, 2 Gb/s IO links, 23x23 BGA
  - 12 mm^2, 3 k patterns
- AM06 large area prototype
  - 65nm, 2 Gb/s IO links, 23x23 BGA
  - ~160 mm^2, 128 k patterns, 400M transistor
  - aim was a working device in a single submission
- Design assembled early 2015
  - Added “spare logic”
  - Increased setup and hold margins
  - Additional worst case corner
- Design submitted Jun 2015
  - 3 typical, 3 slow and 3 fast wafers
    - ± 7.5% saturation current





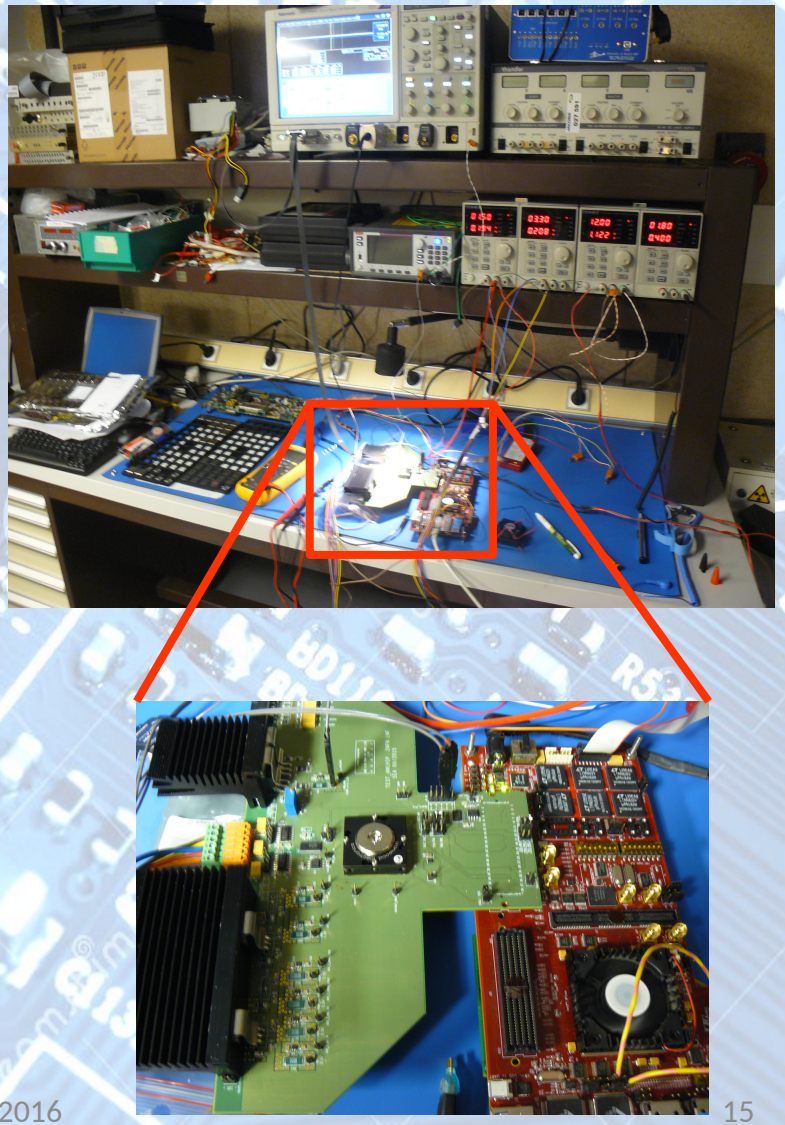
AMchip06 – It's here!

Design: INFN Milano, LPNHE, INFN Frascati, INFN Pisa

Jan 7, 2016 received
149 AM06 slow corner devices

AM06 testing results

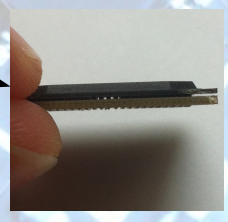
- AM06 includes built-in self test (BIST)
  - Tests full chip (w/ large coverage) in ~1 second
  - 16 chips for first LAMB at CERN within 7 days!
- 143 devices tested
  - 119 chips without defects
  - Yield 83% +- 3% (estimate was 74%)
    - Faulty chips have localized defects
- AM06 “slow corner” works well
  - at 100 MHz (nominal speed), 1.15 V supply
  - more to be learned on power supply margin
  - more AM06 being packaged: staged delivery
- Considering an improved package
  - Include decoupling capacitors to improve power stability
- Preparing large scale testing at external company
  - Full FTK installation 8192 good devices + spares



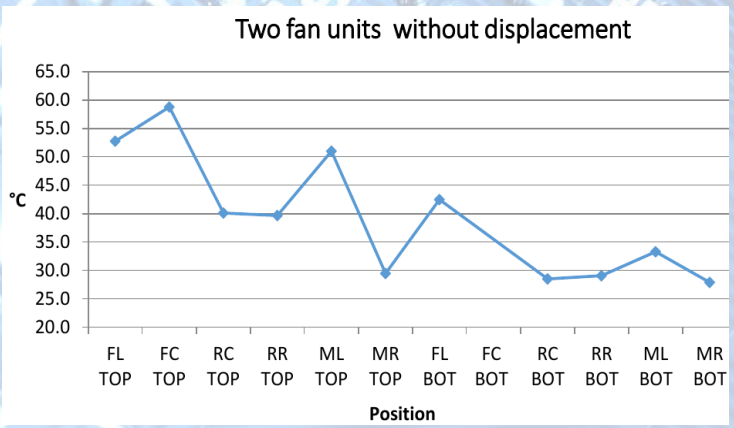
AM board

Pisa

- AMBv4 received in December
- Next (and final) version submitted
  - Fix few issues: including a bug from the CAD
  - Limited, but non zero, schedule risk
    - Working closely with the supplier
- Distributing up to 400W
  - Expected usage at 250W
  - Cooling performance critical
- LAMBs ready since September
  - Tested with AM05-AM06 adapter
- Now have 5 LAMBs in hand
  - First full AM board assembled
- PRR in March
  - after tests of fully loaded AM board

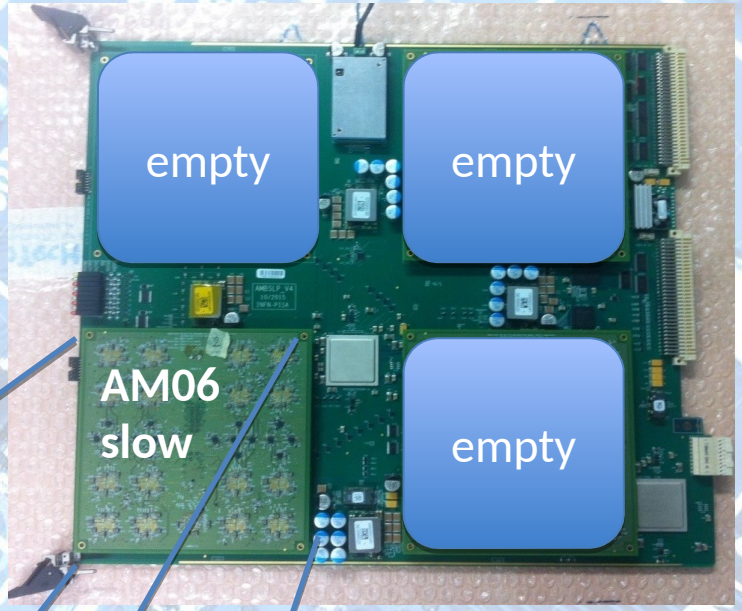


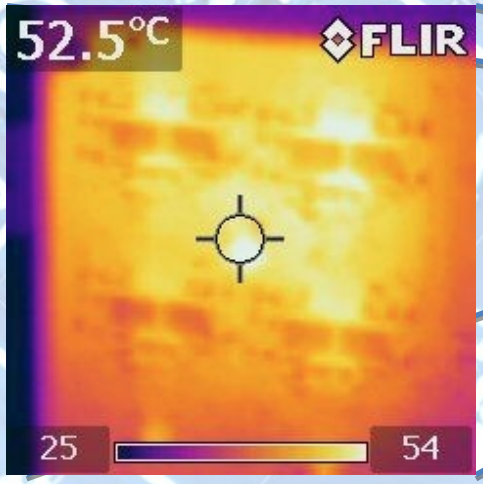
Mock up cooling measures 2014/15

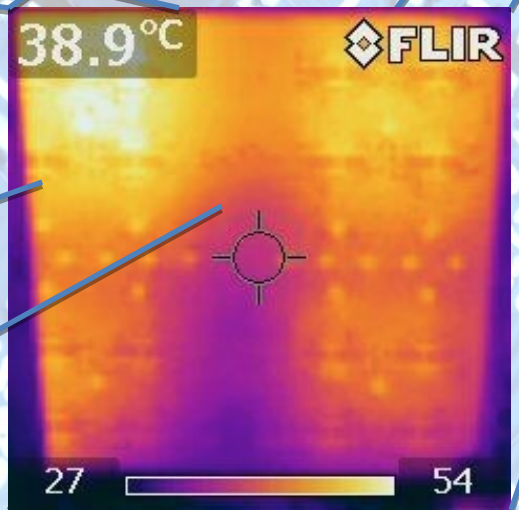


AM06 on AM board first tests

- AM06 slow @ 1.15V
  - At full usage 3.3 A, 3.8W, plus ~0.3W for IO
  - Expected usage 40-50%
  - Goal for cooling 70% usage = 3W
- Single LAMB cooled well at ~4W per AM06
  - 4W pessimistic condition
  - Good indication for full AMB in realistic case
- Full AMB tests on going
  - Will use USA15 infrastructure





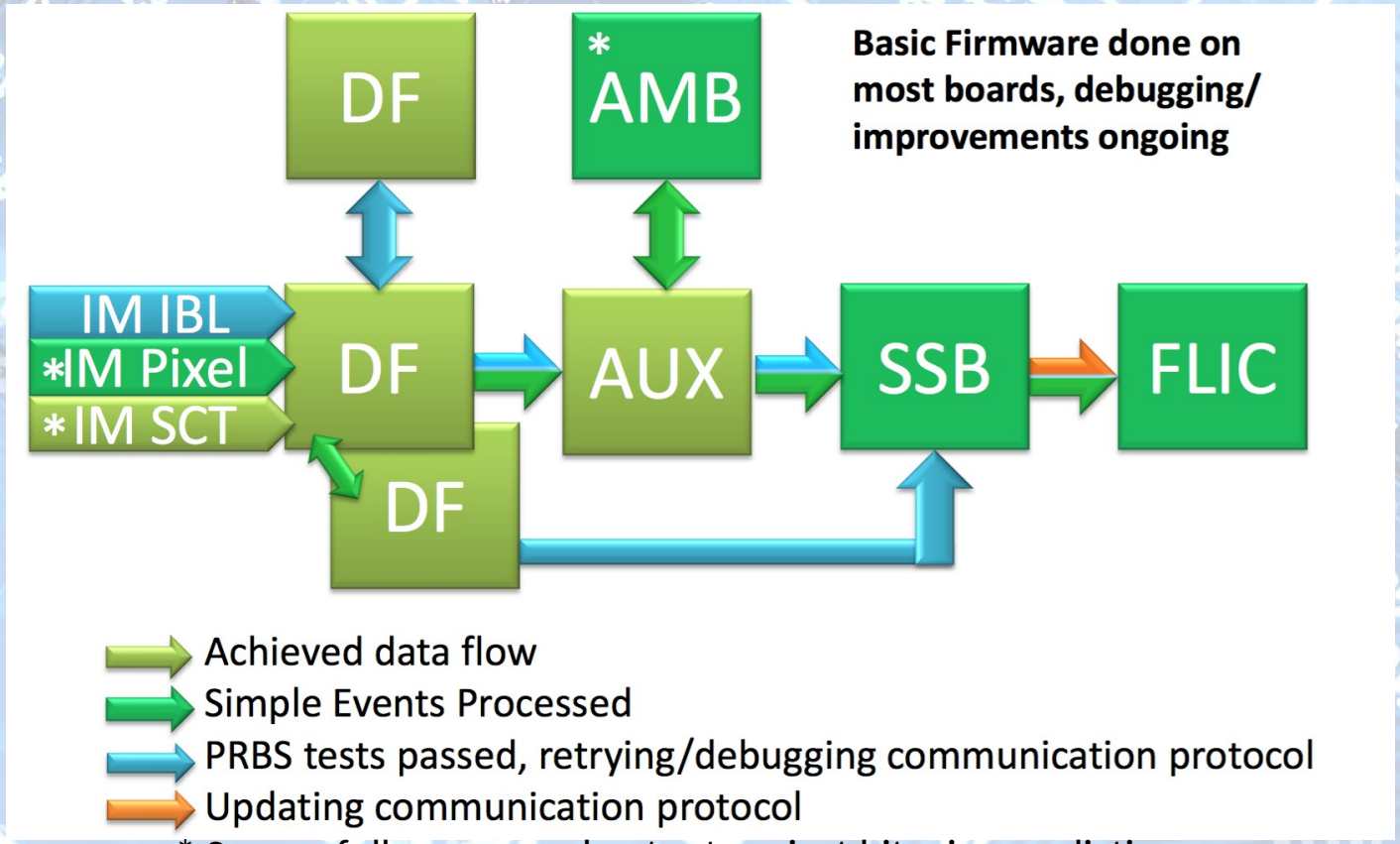


Schedule

- Apr 2016: full installation of IMs, DFs and FLICs
- July 2016: launch production of more AM06
  - after 3 AMB tests, but before barrel commissioned
- Sep 2016: full installation of
  - 16 AUXes, 16 AMBs (50 to 100% populated), 8 SSBs
- Nov 2016: launch production of more processing cards
  - after barrel only system will be commissioned
- May 2017: full coverage FTK installed

Integration status

- Focus now: tests, integration and commissioning
  - Status differ board by board, from early testing to advanced commissioning

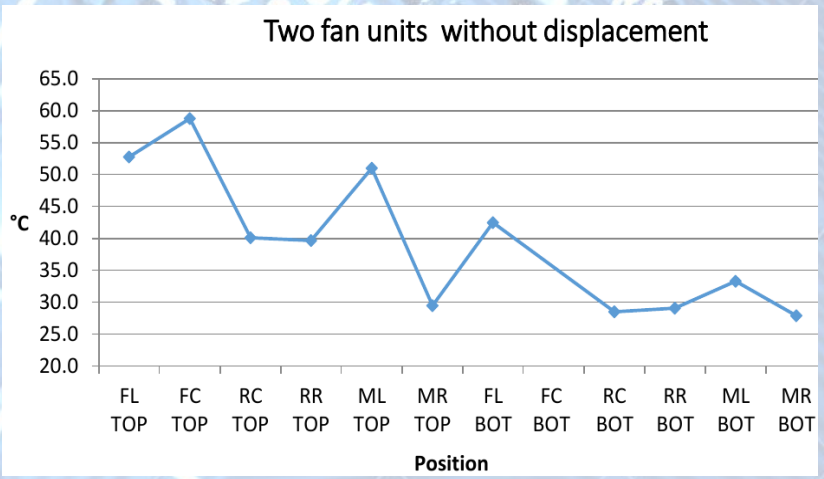


USA15 infrastructure

Argonne, Geneva, Pavia, Pisa, all

- ATCA: fully installed
  - 2 racks for IM-DFs with two 14-slot ATCA shelves each
  - one shelf installed with full DFs + IMs modules
  - 1 rack for FLIC with one 6-slot ATCA shelf
- VME: 2 racks installed (system for 2016)
  - Wiener bin + Wiener PS + Wiener and Pavia's fan tray
  - Wiener bin + CAEN PS + 2 Pavia's fan trays: prototype system for production
- Preliminary VME cooling tests done with mockup boards
  - System ready for cooling tests with AMB fully loaded of AM06

PCB temperature



Summary

- The FTK hardware is coming together
  - Most HW for barrel only system is produced
  - SSB in production
  - AM06 and follow up AMB on the critical path
    - AM board schedule squeezed as much as possible
- AM06 works well !
  - Meets FTK goals
  - More to be learned about operational margin
- Focus now: firmware, software, testing, commissioning
- Commissioning FTK in steps as production completes

Acronyms

- FTK: Fast TracKer
- IM or FTK_IM: FTK Input Mezzanine
- DF: Data Formatter
- AUX: Auxiliary card
- AMB: Associative Memory Board
- LAMB: Little Associative Memory Board
- AM05 and AM06: Associative Memory chip version 5 and 6
- SSB: Second Stage Board
- FLIC: FTK to Level-2 Interface Crate
- HLT: High Level Triggers
- PU: Processing Unit = AMB+AUX