ATLAS L1 Track Trigger

Overview and status of the R&D

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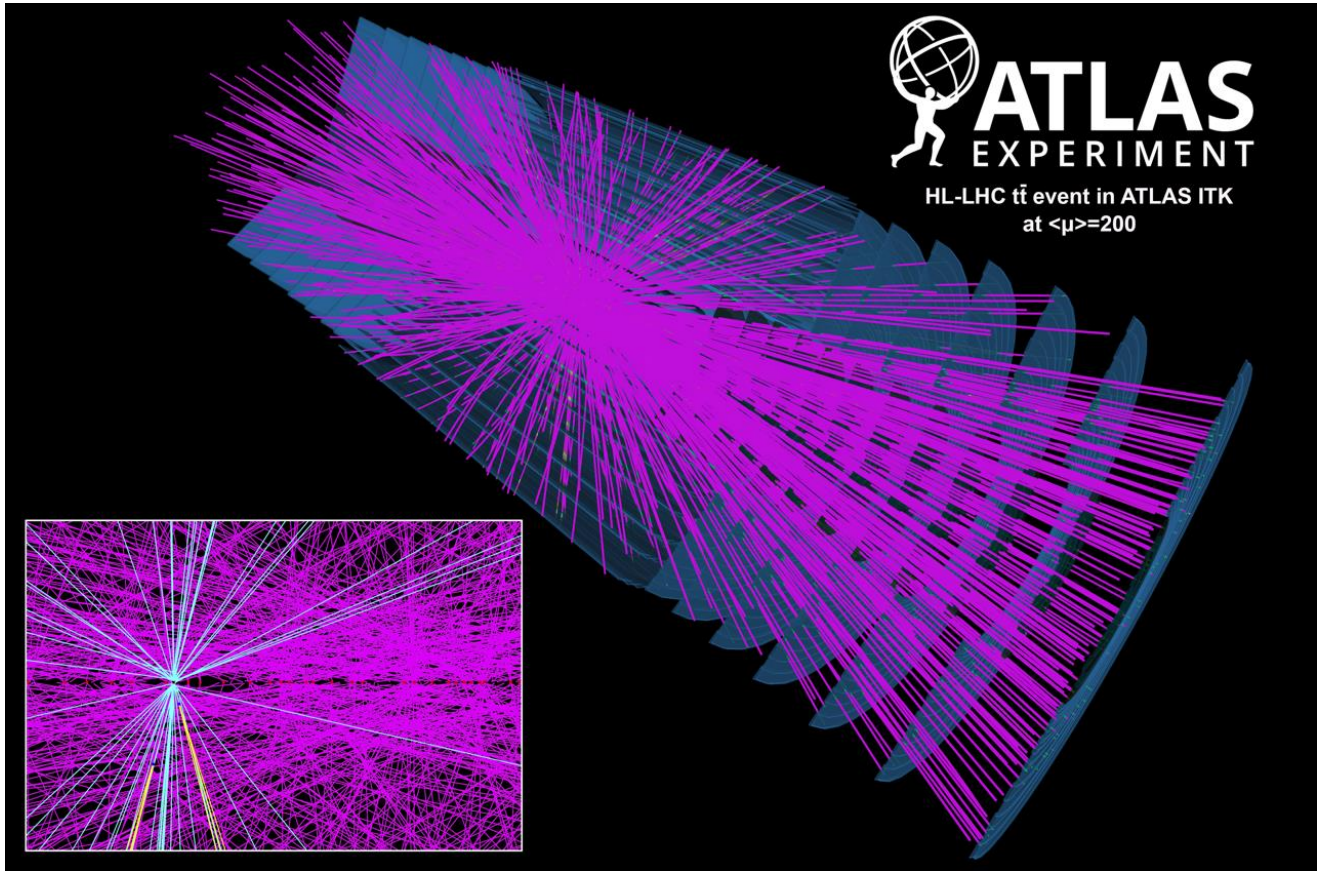
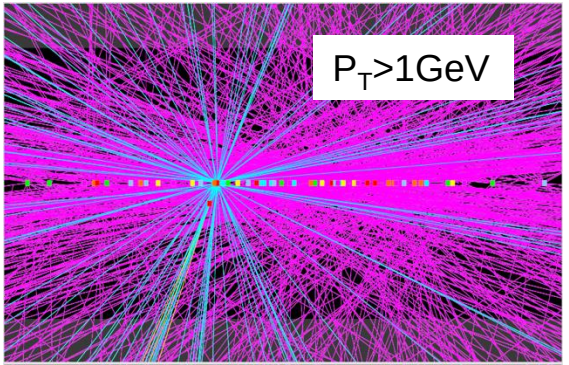
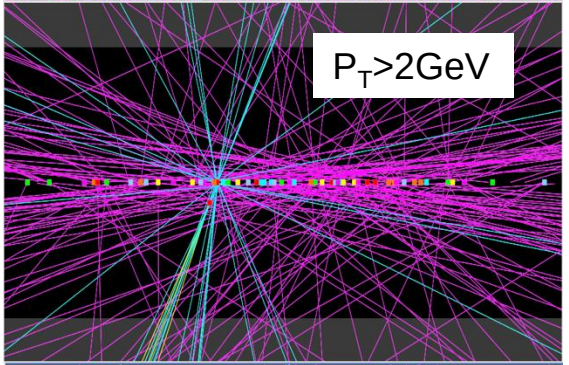
Outline

- Overview of ATLAS Phase-II TDAQ architecture(s)
- Overview of L1Track (and FTK++) pattern recognition strategy
  - Results using full simulation of ITk at <μ>=200
- Trigger performance studies
- ITk strips readout and latency estimates
- L1Track (and FTK++) hardware
- Conclusions and outlook

Tracker's view of the HL-LHC challenge







What drives the Ph-II TDAQ upgrades

- Physics:
  - Keep same thresholds as Run-1, lower if possible
  - Increase acceptance (esp. of barrel muon trigger system)

  Above requirements even more pertinent after Higgs discovery!

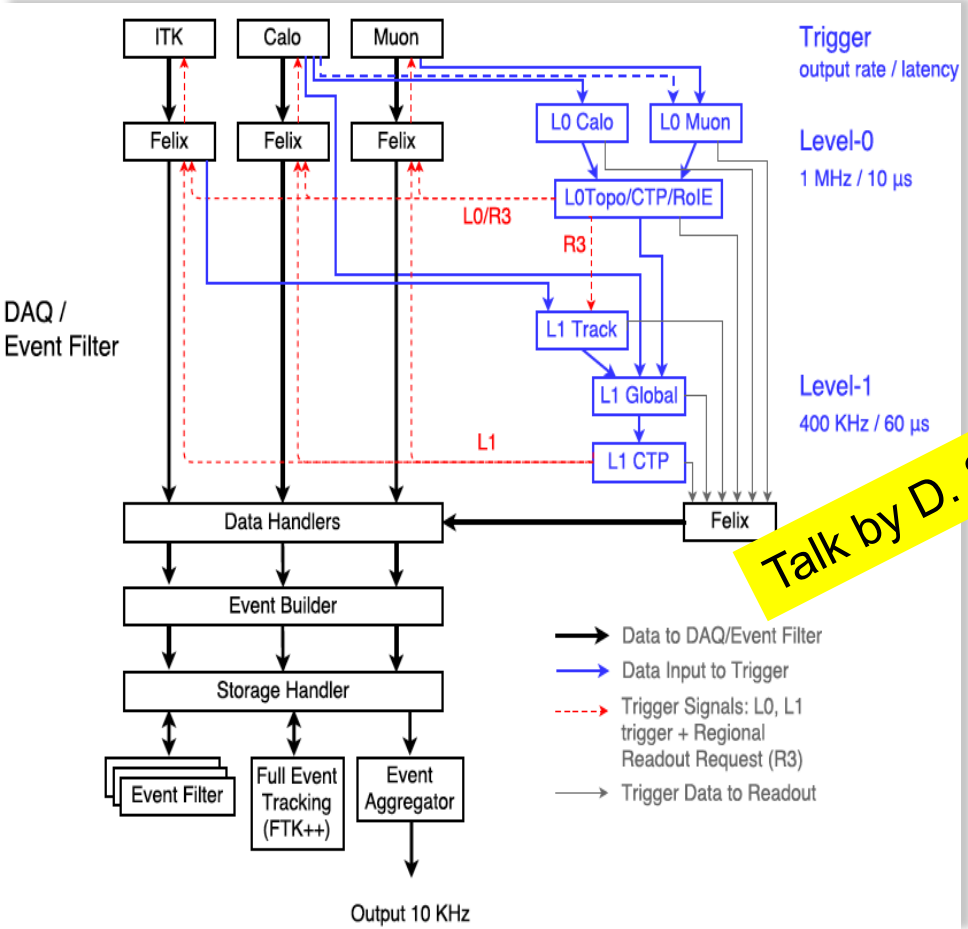
- Hardware: L0/L1 only choice given the constraints
  - Legacy MDT barrel electronics – lat… and readout bandwidth
  - ITk readout bandwidth (and a…ted services ➔ material)
  - (more recently) NSW re… bandwidth

  Talk by D. Sankey

- In the past year or so, above constraints alleviated or eliminated, so a single-level architecture at 1MHz seems possible

Overview of Ph-II TDAQ architectures

L0/L1 architecture

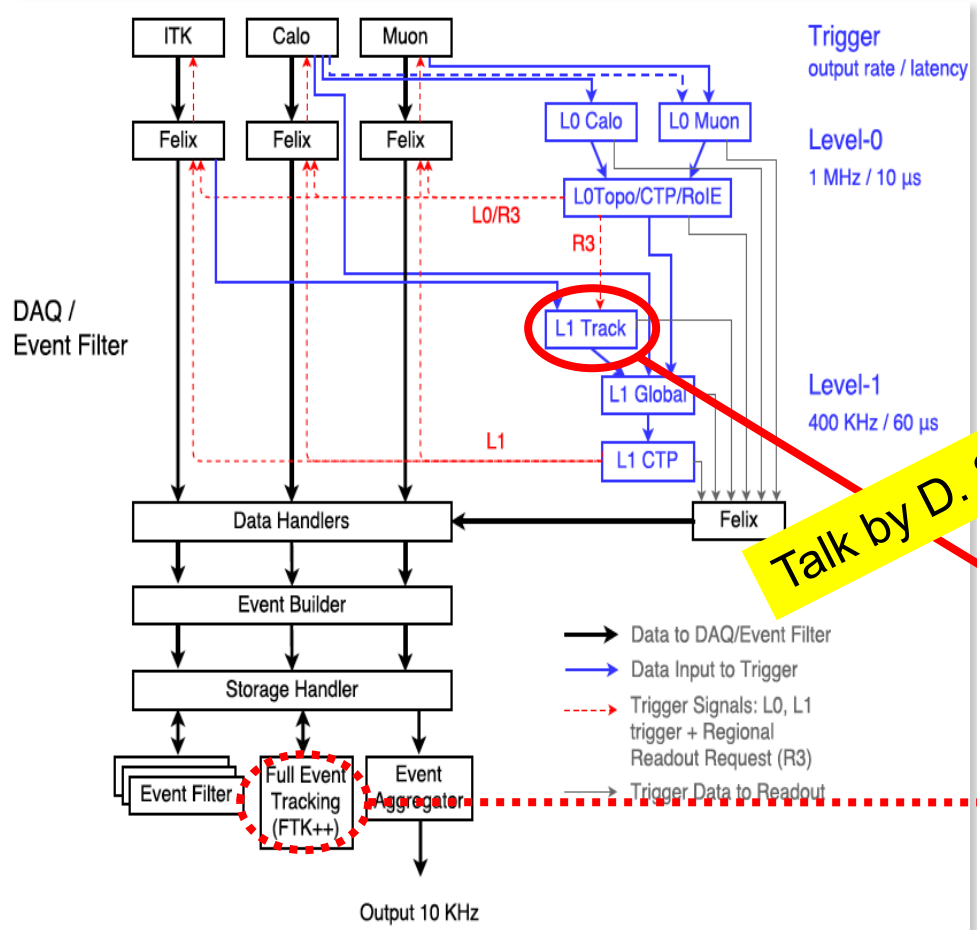


Talk by D. Sankey

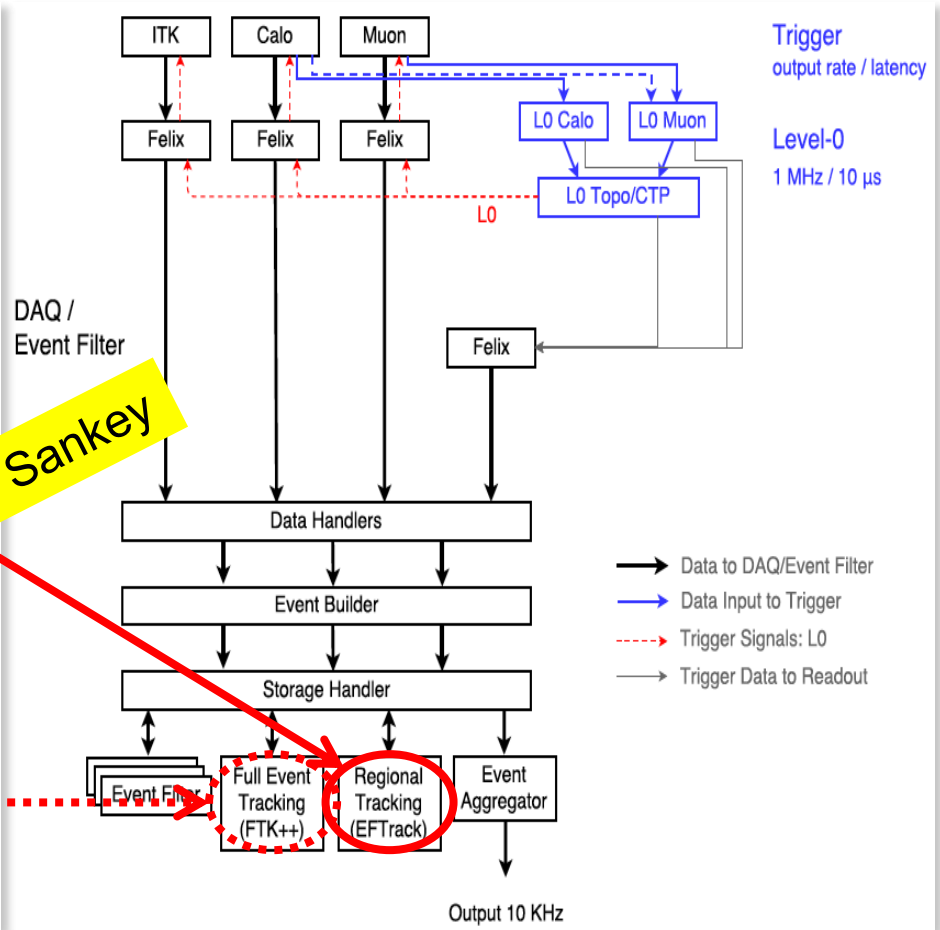
- Ph-I L1Muon/Calo become Ph-II L0Muon/Calo
  - Reduce rate: 40➔1MHz (6µs)
  - Provide info for regional ITk readout, feeding L1Track
- L1Track combined with more Calo/Muon info in L1Global
  - Reduce rate: 1➔0.4MHz (24µs)

Overview of Ph-II TDAQ architectures

L0/L1 architecture



Single-level architecture



Talk by D. Sankey

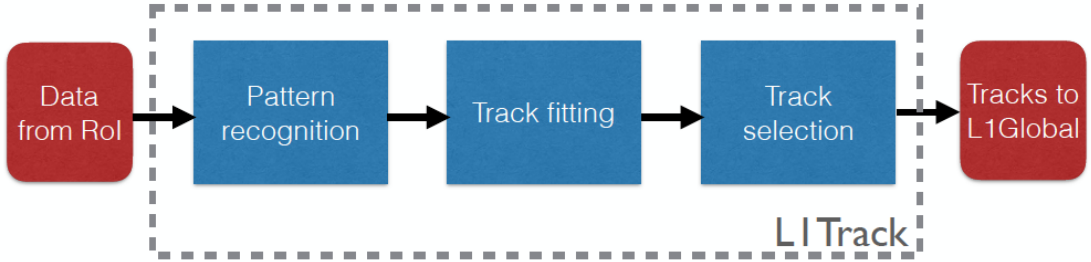
L1Track aims & requirements

- Aims/role:
  - Help to keep the single lepton p_T thresholds as low as in Run 1
  - Help multi-object triggers (esp. hadronic) by requiring consistency in z

- Requirements/targets
  - Factor ~5 rate reduction for MU20 and EM18 with signal eff. >~95%
  - Track z_0 resolution better than ~10mm
  - ITk (regional) readout + pattern recognition to fit within ~15μs
    - Most relevant in the L0/L1 trigger scheme

L1Track (& FTK++) Pat. Rec. strategy

Input rate: 1MHz
Regional readout
(max 10% of ITk)

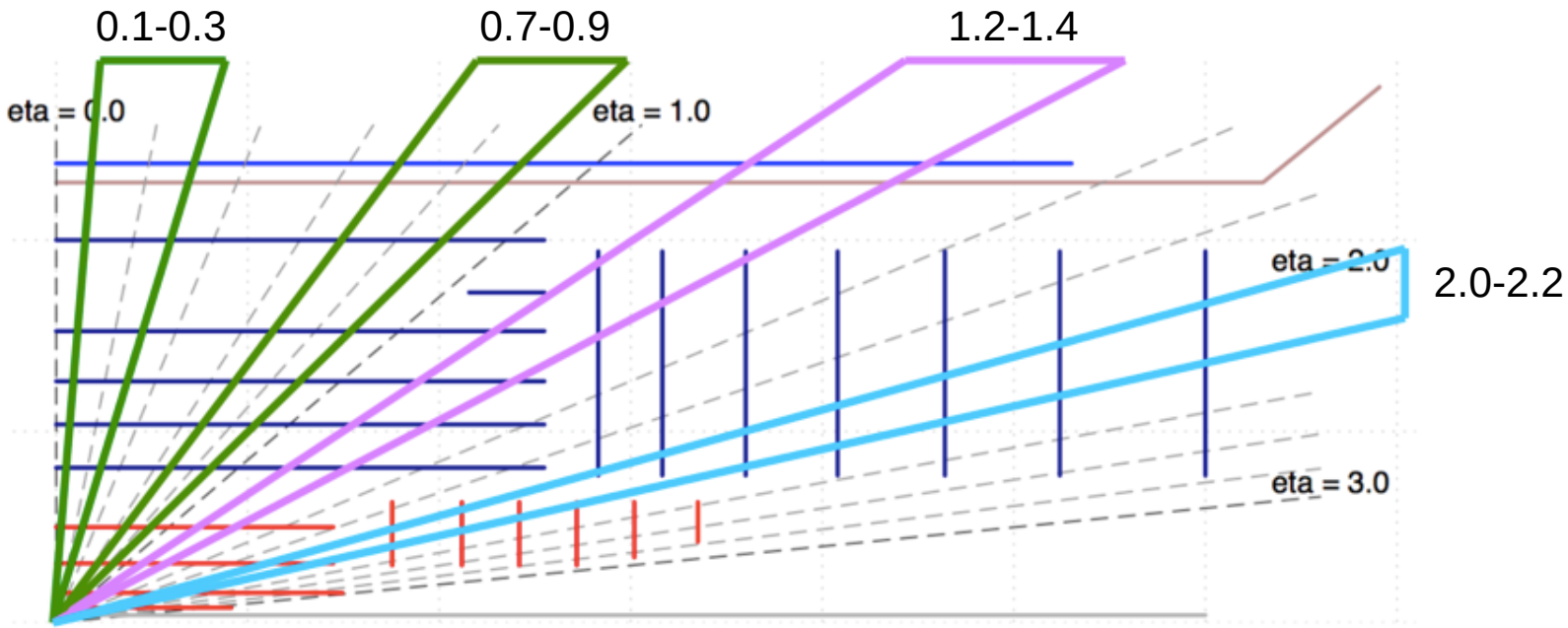


Talk by M. Beretta

- Pre-computed patterns formed by muon tracks stored in AM chips
  - Each pattern consists of local positions of superstrips (SSs) in different ITk layers
    - Can't use full granularity &all ITk layers (too many patterns)
  - SSs flow through AM Chips (8 16-bit buses)
  - Match when all (/most) hits of a pattern fire

L1Track pattern recognition studies

Tested performance in four 0.2x0.2 regions:



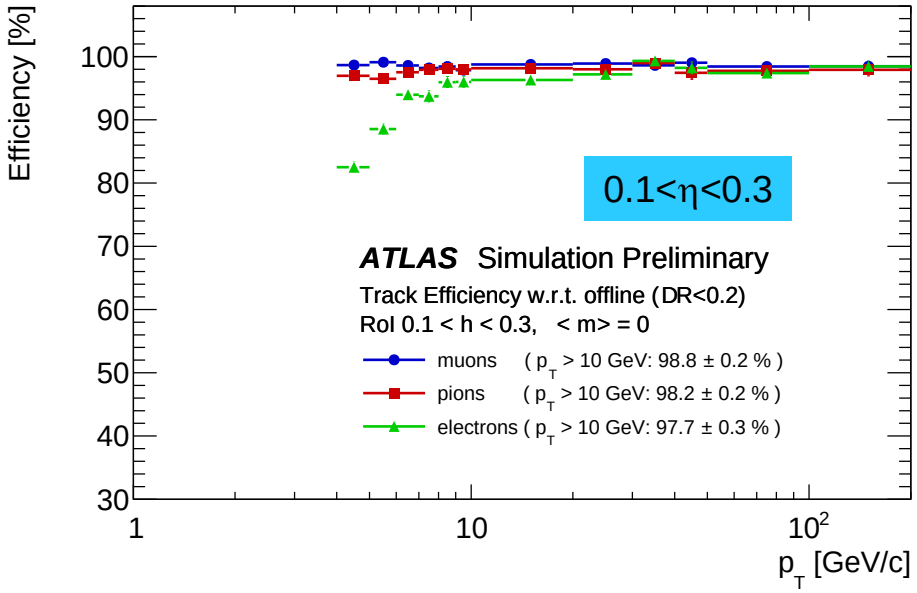
So far results with strip layers only, studies with pixel layers are ongoing

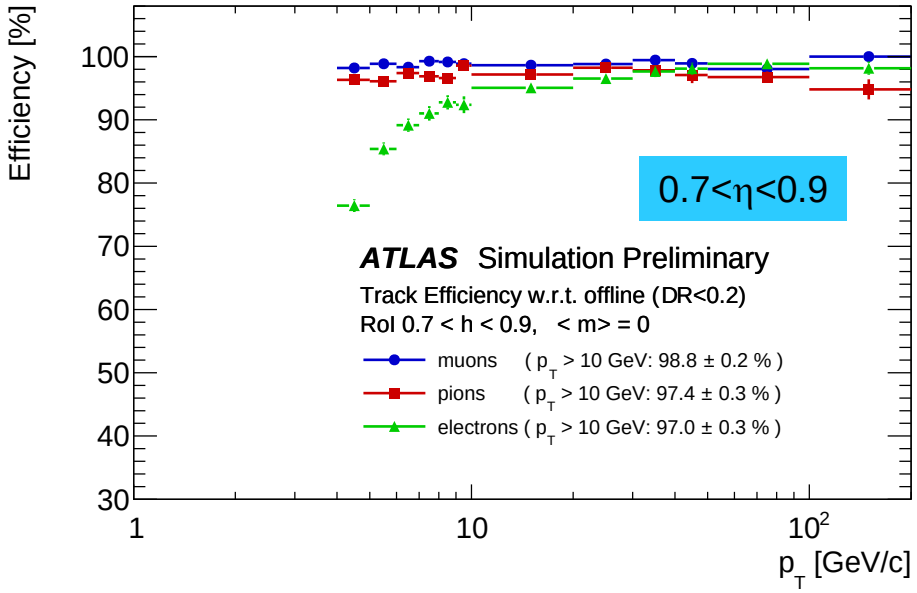
Pattern bank formation

- Used O(100M) muons per region
  - p_T range (4→400GeV) flat in $1/p_T$
  - Flat in $|d_0|$ (<2mm), $|z_0|$ (<150mm), phi (0.3-0.5) and η

- Target bank size is ~10^6 per 0.2x02 region
  - → ~10^9 for |η|<2.5 or ~$1.5x10^9$ for |η|<4.0,
  - Drives the size, hence the cost, of the hardware system

Overall track reconstruction performance



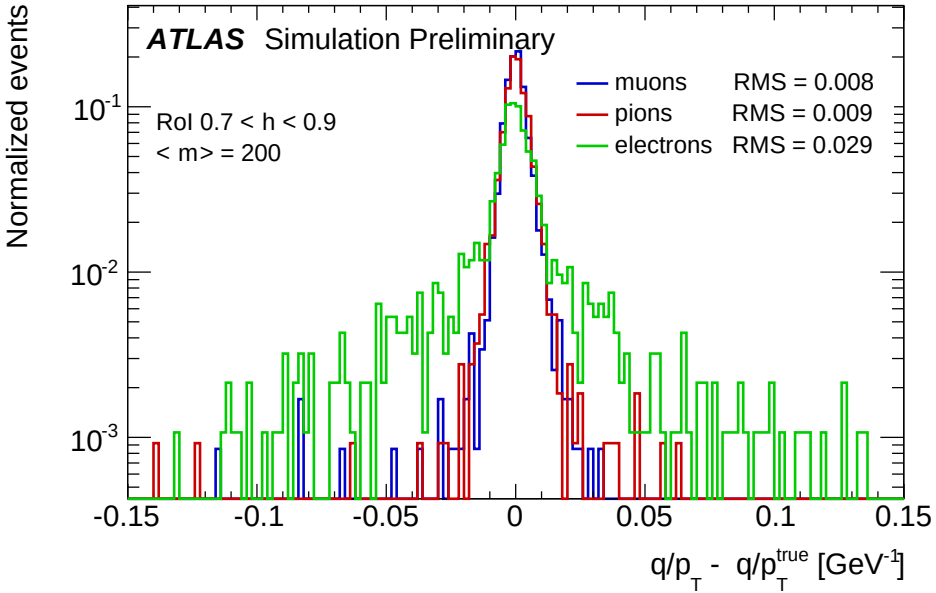


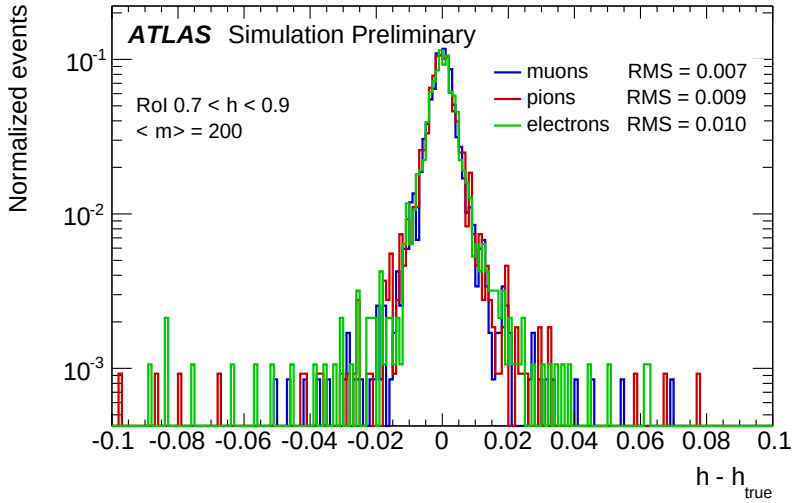
Efficiency wrt offline is very high for all types of particles

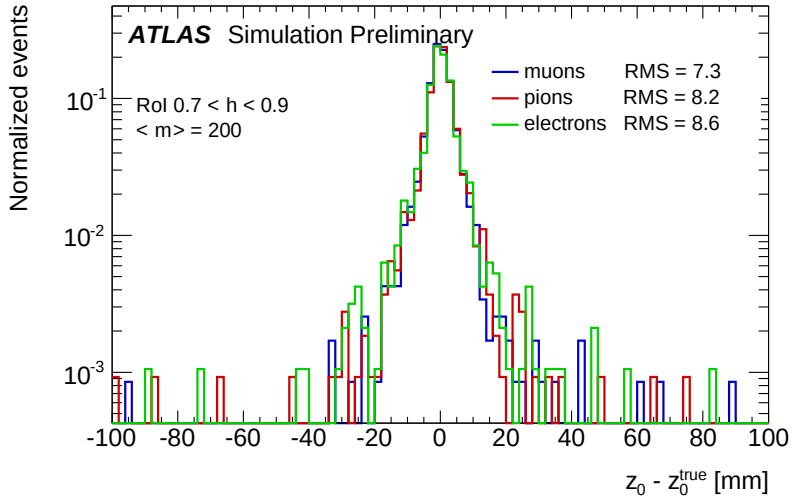
Electron efficiency drops below 10 GeV due to brem

Track parameter resolutions

Track parameter residual distributions (using only Strip layers):

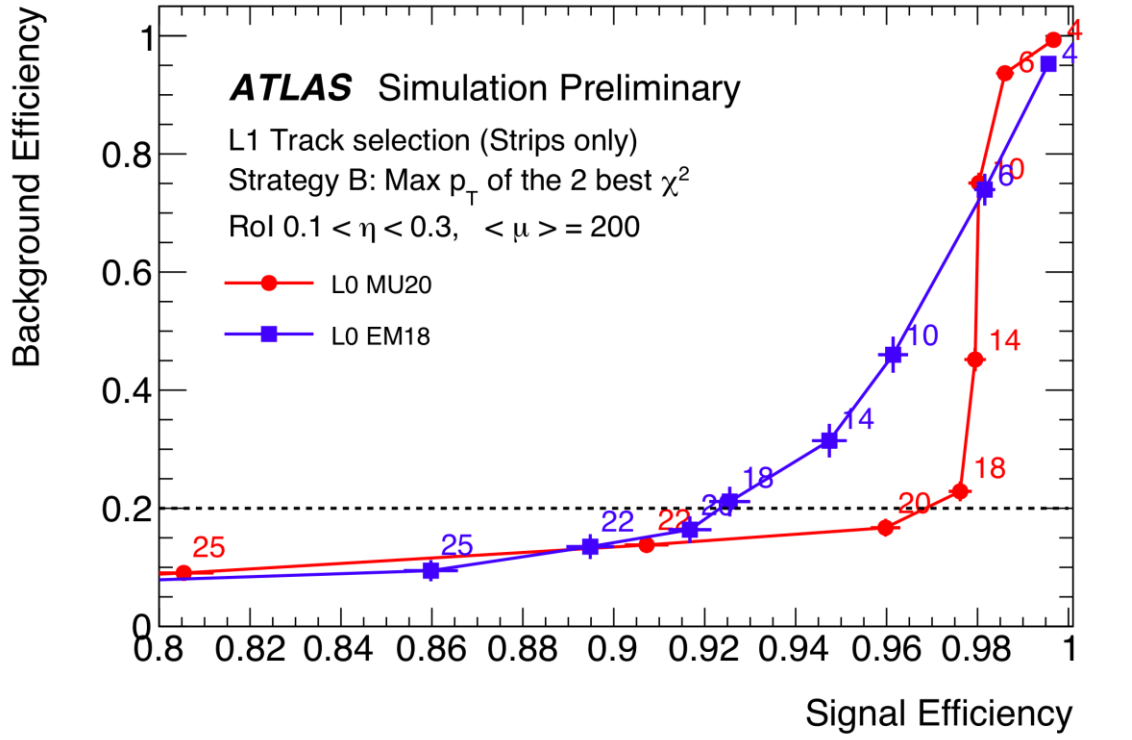






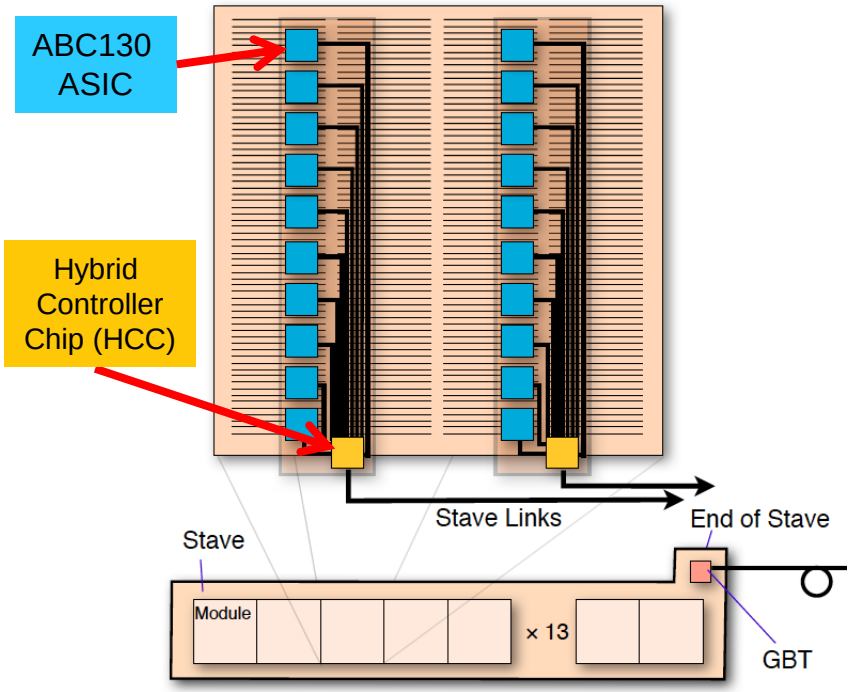
Performance in physics RoIs

- Achieved/approaching target of ~5x rejection for ~95% efficiency for single lepton triggers with simple selection algorithms, e.g.
  - from the two lowest χ^2 L1Track tracks use the one with highest p_T

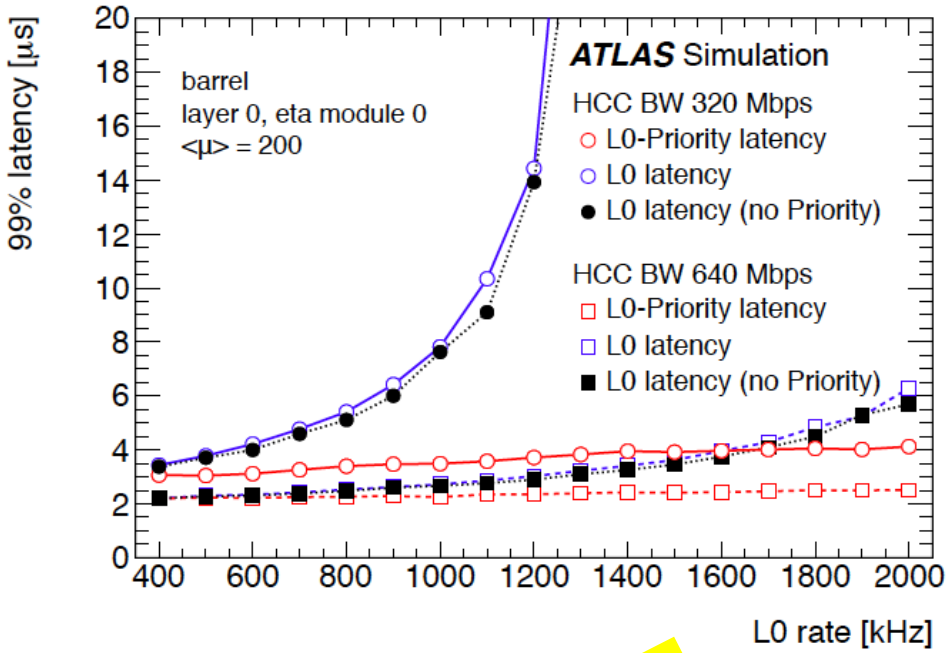


ITk Strips readout latency

Si wafer: 10x10cm



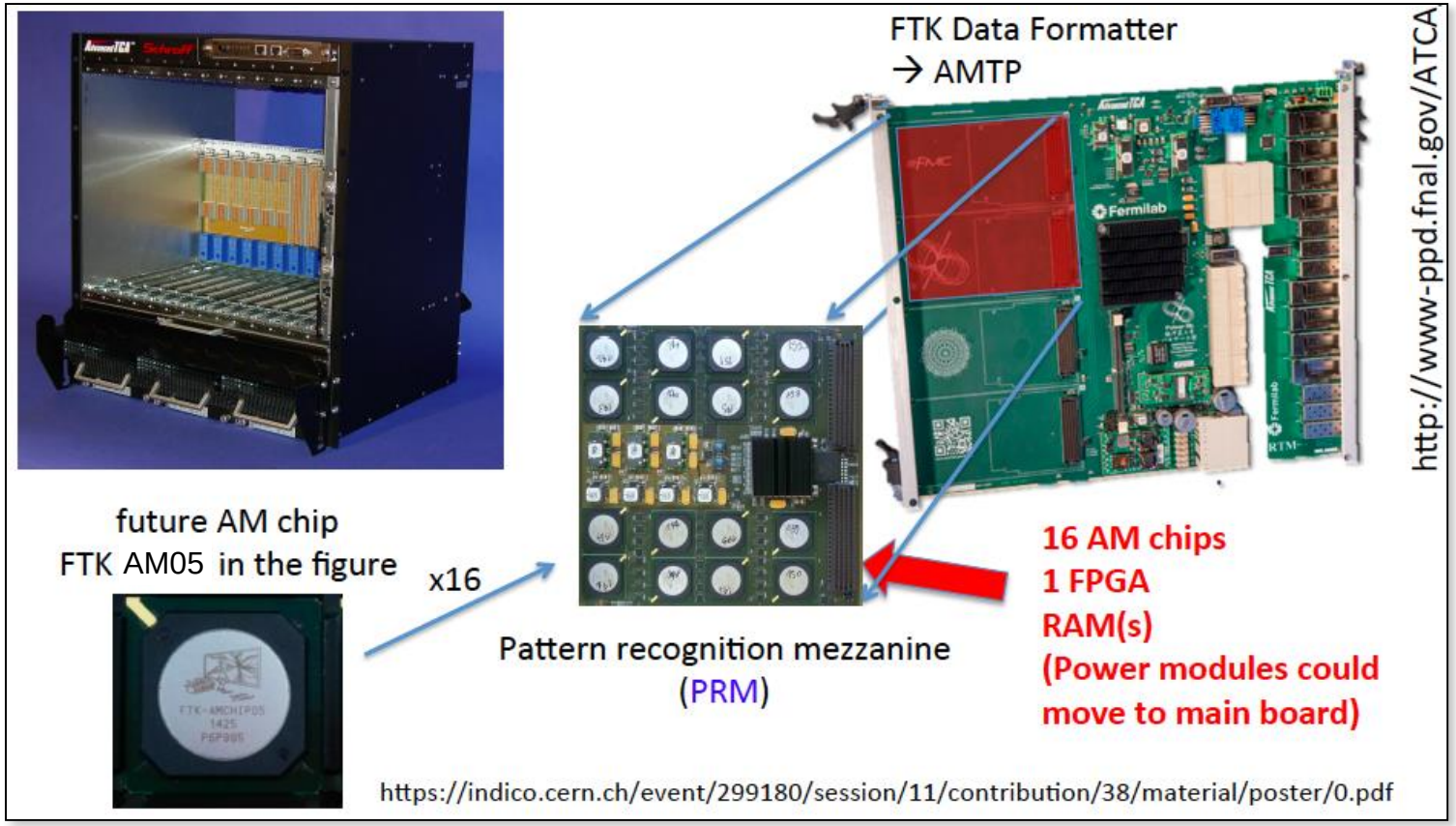
Discrete Event Simulation (<μ>=200):



Talk by A. Grillo

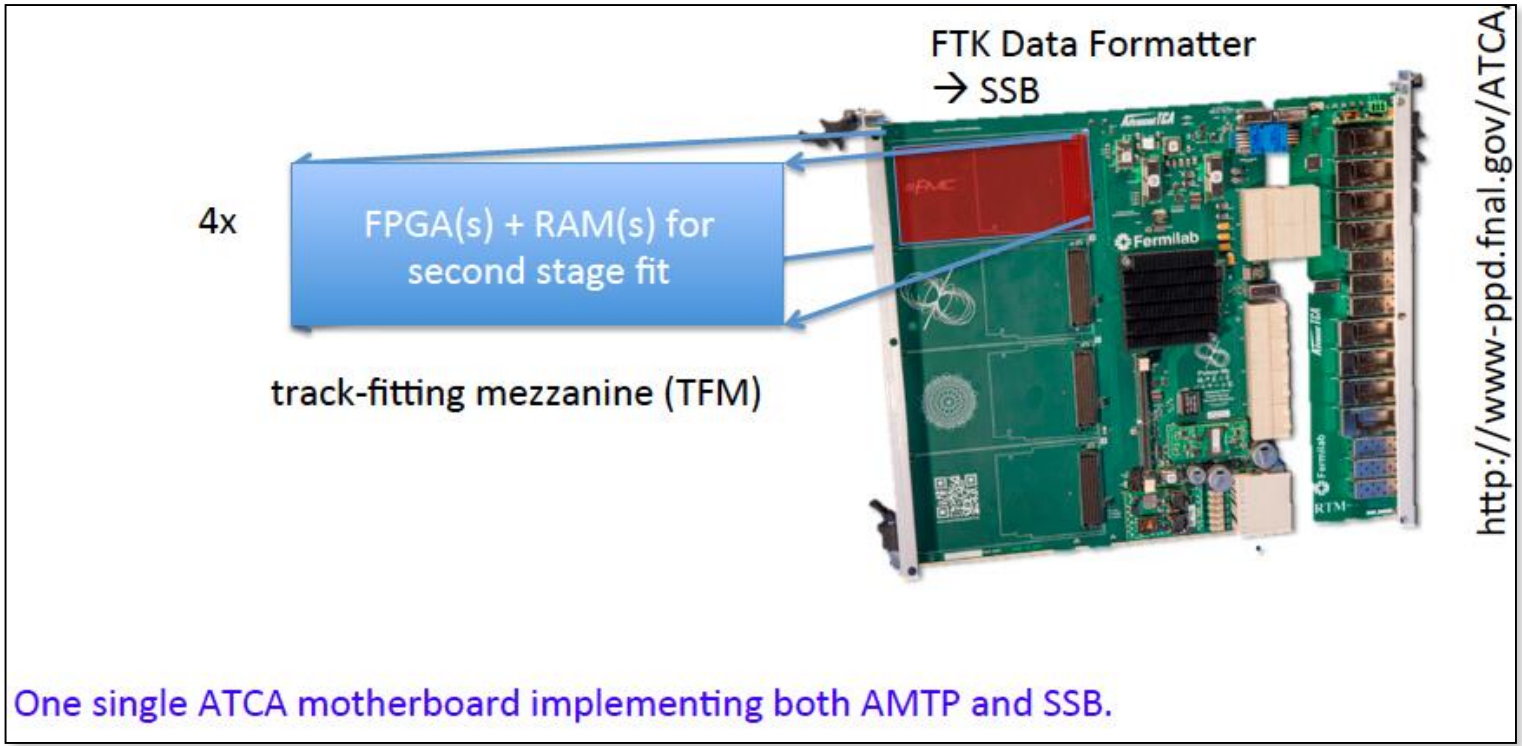
L1Track (and FTK++) hardware – I

- Main board: Associative Memory Tracking Processor (AMTP)



L1Track (and FTK++) hardware – II

- Second Stage Boards: for tracks found in the AM step, include unused Si layers and perform complete fit
  - Seems unnecessary for L1Track (but imperative for FTK++)



Size/Latency of L1Track hardware

- Size of off-detector system driven by
  - A) the number of patterns (hence AM chips) needed to do the job
    - 1M per RoI ➔ ~3×10^9 patterns for $|\eta|<4.0$ ➔ ~6k AM Chips
      - Assumes pattern banks are doublicated to satisfy latancy constraints
      - If latency studies show this to be unnecessary, big margin to reduce p_T threshold (or cost)
  - B) the number of AM chips that can be fitted in an AMTP board
    - 32 chips per board ➔ ~192 boards ➔ 16 crates (+4 crates for the SSB, if needed)

- Latency driven by
  - Speed of the AM chip (projected to be 200MHz in HL-LHC version)
  - Number of clusters in the busiest ITk layer to be propagated to AM chip
    - From simulation: number of clusters in busiest layer <250 ➔ latency < 1.5μs

R&D towards the TDAQ Ph-II TDR

- AM chip R&D
  - Prototyping 28nm technology (would give x4 in pattern capacity)
  - Exploring 3D integration
  - Work to reduce power consumption

- Dataflow and latency studies
  - ITk readout latency (important for L0/L1 design)
  - L1Track off-detector hardware latency

- Extend pattern recognition studies
  - Wider/full eta-phi range
  - Include pixel layers

- Detailed specification of the off-detector hardware

Summary

- The role of ID tracking will be more prominent at HL-LHC
- Since the ATLAS Phase-II LoI in 2013, we have demonstrated that an AM-based L1Track implementation can achieve the required trigger/physics performance in the L0/L1 architecture
- Lots more R&D needed to qualify the full system before the TDR, but no show-stoppers identified