ATLAS L1 Track Trigger
Overview and status of the R&D

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• Overview of ATLAS Phase-II TDAQ architecture(s)

• Overview of L1Track (and FTK++) pattern recognition strategy
  – Results using full simulation of ITk at $<\mu>=200$

• Trigger performance studies

• ITk strips readout and latency estimates

• L1Track (and FTK++) hardware

• Conclusions and outlook
Tracker’s view of the HL-LHC challenge
What drives the Ph-II TDAQ upgrades

• Physics:
  – Keep same thresholds as Run-1, lower if possible
  – Increase acceptance (esp. of barrel muon trigger system)

Above requirements even more pertinent after Higgs discovery!

• Hardware: L0/L1 only choice given the constraints
  – Legacy MDT barrel electronics – latency and readout bandwidth
  – ITk readout bandwidth (and associated services ➔ material)
  – (more recently) NSW readout bandwidth

• In the past year or so, above constraints alleviated or eliminated, so a single-level architecture at 1MHz seems possible
Overview of Ph-II TDAQ architectures

L0/L1 architecture

• Ph-I L1Muon/Calo become Ph-II L0Muon/Calo
  - Reduce rate: 40 → 1MHz (6μs)
  - Provide info for regional ITk readout, feeding L1Track

• L1Track combined with more Calo/Muon info in L1Global
  - Reduce rate: 1 → 0.4MHz (24μs)
Overview of Ph-II TDAQ architectures

**L0/L1 architecture**

- ITK
- Calo
- Muon
- L0 Calo
- L0 Muon
- L0Topo/CTP/ReIE
- L1 Topo/CTP
- L1 Global
- L1 CTP

**Single-level architecture**

- ITK
- Calo
- Muon
- L0 Calo
- L0 Muon
- L0 Topo/CTP

Talk by D. Sankey
L1Track aims & requirements

• Aims/role:
  – Help to keep the single lepton $p_T$ thresholds as low as in Run 1
  – Help multi-object triggers (esp. hadronic) by requiring consistency in z

• Requirements/targets
  – Factor $\sim$5 rate reduction for MU20 and EM18 with signal eff. $>\sim$95%
  – Track $z_0$ resolution better than $\sim$10mm
  – ITk (regional) readout + pattern recognition to fit within $\sim$15$\mu$s
    • Most relevant in the L0/L1 trigger scheme
• Pre-computed patterns formed by muon tracks stored in AM chips
  – Each pattern consists of local positions of superstrips (SSs) in different ITk layers
    • Can’t use full granularity & all ITk layers (too many patterns)
  – SSs flow through AM Chips (8 16-bit buses)
  – Match when all (/most) hits of a pattern fire
L1Track pattern recognition studies

Tested performance in four 0.2x0.2 regions:

- 0.1-0.3
- 0.7-0.9
- 1.2-1.4
- 2.0-2.2

So far results with strip layers only, studies with pixel layers are ongoing
Pattern bank formation

- Used $O(100M)$ muons per region
  - $p_T$ range ($4 \rightarrow 400\text{GeV}$) flat in $1/p_T$
  - Flat in $|d_0| (<2\text{mm})$, $|z_0| (<150\text{mm})$, phi (0.3-0.5) and $\eta$

- Target bank size is $\sim 10^6$ per 0.2x02 region
  - $\Rightarrow \sim 10^9$ for $|\eta|<2.5$ or $\sim 1.5 \times 10^9$ for $|\eta|<4.0$,
  - Drives the size, hence the cost, of the hardware system
Overall track reconstruction performance

**Efficiency wrt offline is very high for all types of particles**

Electron efficiency drops below 10 GeV due to brem
Track parameter residual distributions (using only Strip layers):

- ATLAS Simulation Preliminary
  - muons, RMS = 0.008
  - pions, RMS = 0.009
  - electrons, RMS = 0.029

- ATLAS Simulation Preliminary
  - muons, RMS = 0.007
  - pions, RMS = 0.009
  - electrons, RMS = 0.010

- ATLAS Simulation Preliminary
  - muons, RMS = 7.3
  - pions, RMS = 8.2
  - electrons, RMS = 8.6
Achieved/approaching target of ~5x rejection for ~95% efficiency for single lepton triggers with simple selection algorithms, e.g.

- from the two lowest $\chi^2$ L1Track tracks use the one with highest $p_T$. 
ITk Strips readout latency

Si wafer: 10x10cm

Discrete Event Simulation ($\mu = 200$):

ATLAS Simulation
HCC BW 320 Mbps
- L0-Priority latency
- L0 latency
- L0 latency (no Priority)

HCC BW 640 Mbps
- L0-Priority latency
- L0 latency
- L0 latency (no Priority)

99% latency [µs]

L0 rate [kHz]
L1Track (and FTK++) hardware – I

- Main board: Associative Memory Tracking Processor (AMTP)

future AM chip
FTK AM05 in the figure

x16

Pattern recognition mezzanine (PRM)

16 AM chips
1 FPGA
RAM(s)
(Power modules could move to main board)

https://indico.cern.ch/event/299180/session/11/contribution/38/material/poster/0.pdf
• Second Stage Boards: for tracks found in the AM step, include unused Si layers and perform complete fit
  – Seems unnecessary for L1Track (but imperative for FTK++)

One single ATCA motherboard implementing both AMTP and SSB.
Size/Latency of L1Track hardware

• Size of off-detector system driven by

  A) the number of patterns (hence AM chips) needed to do the job
  • 1M per RoI $\Rightarrow$ $\sim3\times10^9$ patterns for $|\eta|<4.0 \Rightarrow \sim6k$ AM Chips
    – Assumes pattern banks are doublcated to satisfy latency constraints
    – If latency studies show this to be unnecessary, big margin to reduce $p_T$ threshold (or cost)

  B) the number of AM chips that can be fitted in an AMTP board
  • 32 chips per board $\Rightarrow$ $\sim192$ boards $\Rightarrow$ 16 crates (+4 crates for the SSB, if needed)

  • Latency driven by
    – Speed of the AM chip (projected to be 200MHz in HL-LHC version)
    – Number of clusters in the busiest ITk layer to be propagated to AM chip
      • From simulation: number of clusters in busiest layer $<250 \Rightarrow$ latency $< 1.5\mu$s
R&D towards the TDAQ Ph-II TDR

• AM chip R&D
  – Prototyping 28nm technology (would give x4 in pattern capacity)
  – Exploring 3D integration
  – Work to reduce power consumption

• Dataflow and latency studies
  – ITk readout latency (important for L0/L1 design)
  – L1Track off-detector hardware latency

• Extend pattern recognition studies
  – Wider/full eta-phi range
  – Include pixel layers

• Detailed specification of the off-detector hardware
Summary

• The role of ID tracking will be more prominent at HL-LHC

• Since the ATLAS Phase-II LoI in 2013, we have demonstrated that an AM-based L1Track implementation can achieve the required trigger/physics performance in the L0/L1 architecture

• Lots more R&D needed to qualify the full system before the TDR, but no show-stoppers identified