ATLAS Phase 2 MDT Electronics

ACES Workshop 2016
9th March 2016

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On behalf of the
ATLAS Muon Collaboration

Outline

- Motivation
- Present MDT readout system
- Scheme for phase 2 muon readout and high p_t trigger system
- Possible alternative system re-using NSW hardware
- Demonstrator hardware and firmware
  - Slow control and readout ("CSM prototype study")
  - Mezzanine card for readout & trigger studies
  - Implementation of track finding
- Track finding algorithm and performance
- Hardware matrix and possible scenarios for 2016/2017
- Conclusions

Motivation for New MDT Hardware

New ATLAS phase 2 trigger scheme:

- Only 2 trigger levels: L0 and HLT (high level trigger).
- L0 key properties: 1 MHz max. rate, 6 – 10 µs latency. (current L1: 100 kHz, 2.5 µs)

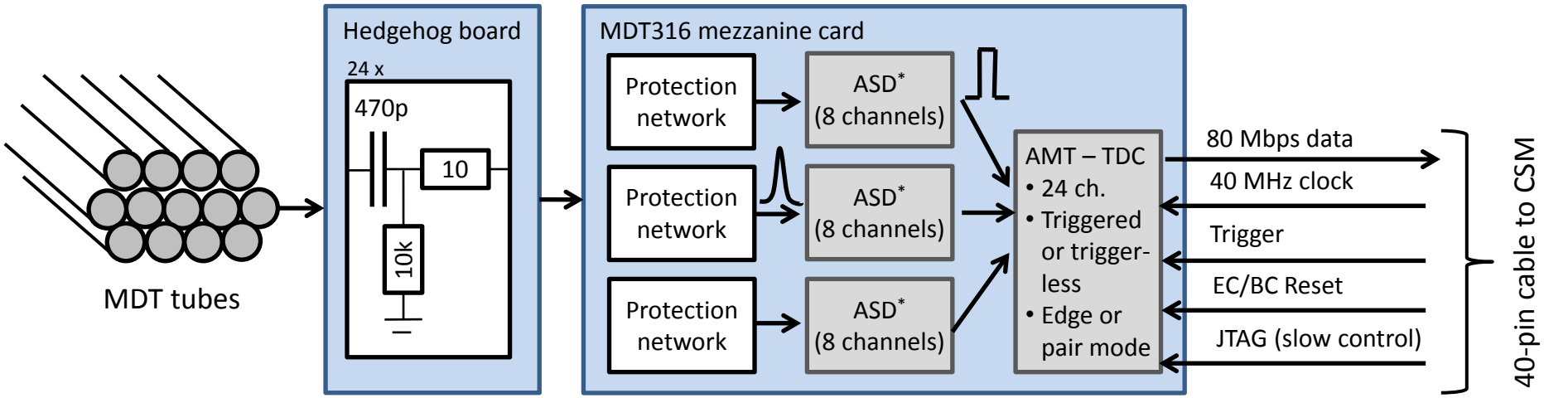
Due to longer latency, the use of precision MDT data for a high p_t L0 muon trigger becomes feasible. Consequences:

⇒ Send all data off detector in untriggered mode (low latency).

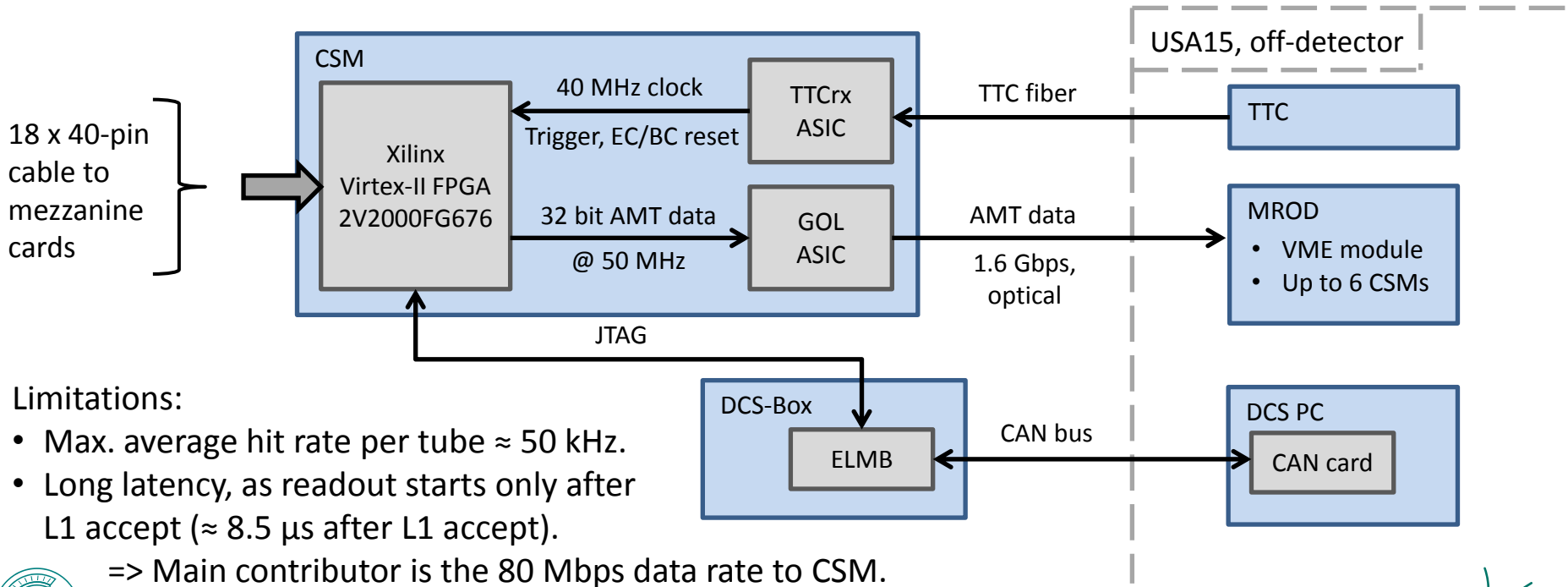
⇒ New MDT front-end and readout / processing hardware.

⇒ Possible alternative concept re-using hardware from the new small wheel (NSW) electronics.

Present Muon Front-End: Readout Data Only



* Amplifier-Shaper-Discriminator: Analog input, digital output.

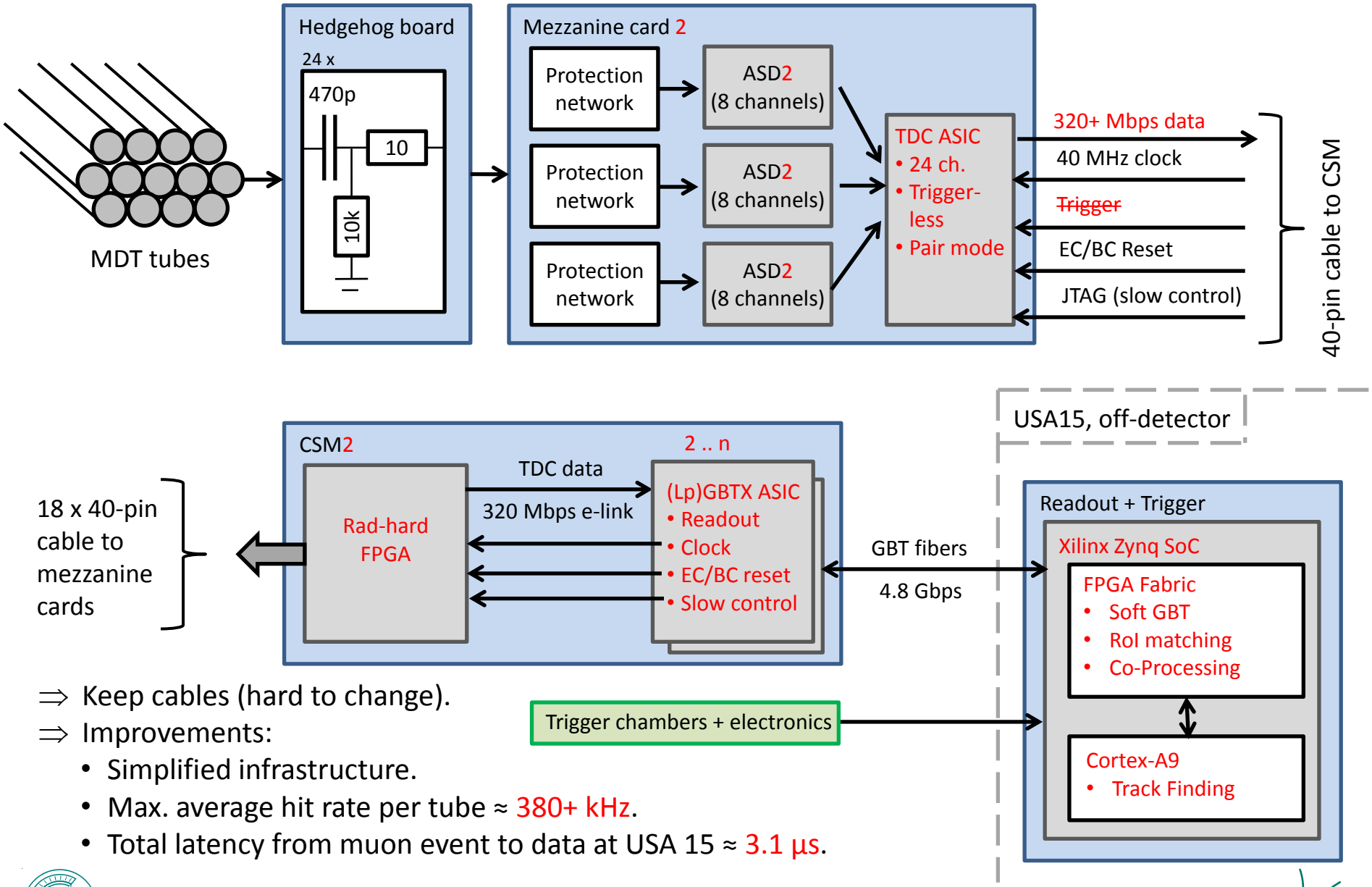


Limitations:

- Max. average hit rate per tube ≈ 50 kHz.
- Long latency, as readout starts only after L1 accept (≈ 8.5 µs after L1 accept).

=> Main contributor is the 80 Mbps data rate to CSM.

Phase 2 Muon Front-End: Readout + L0 Trigger Data

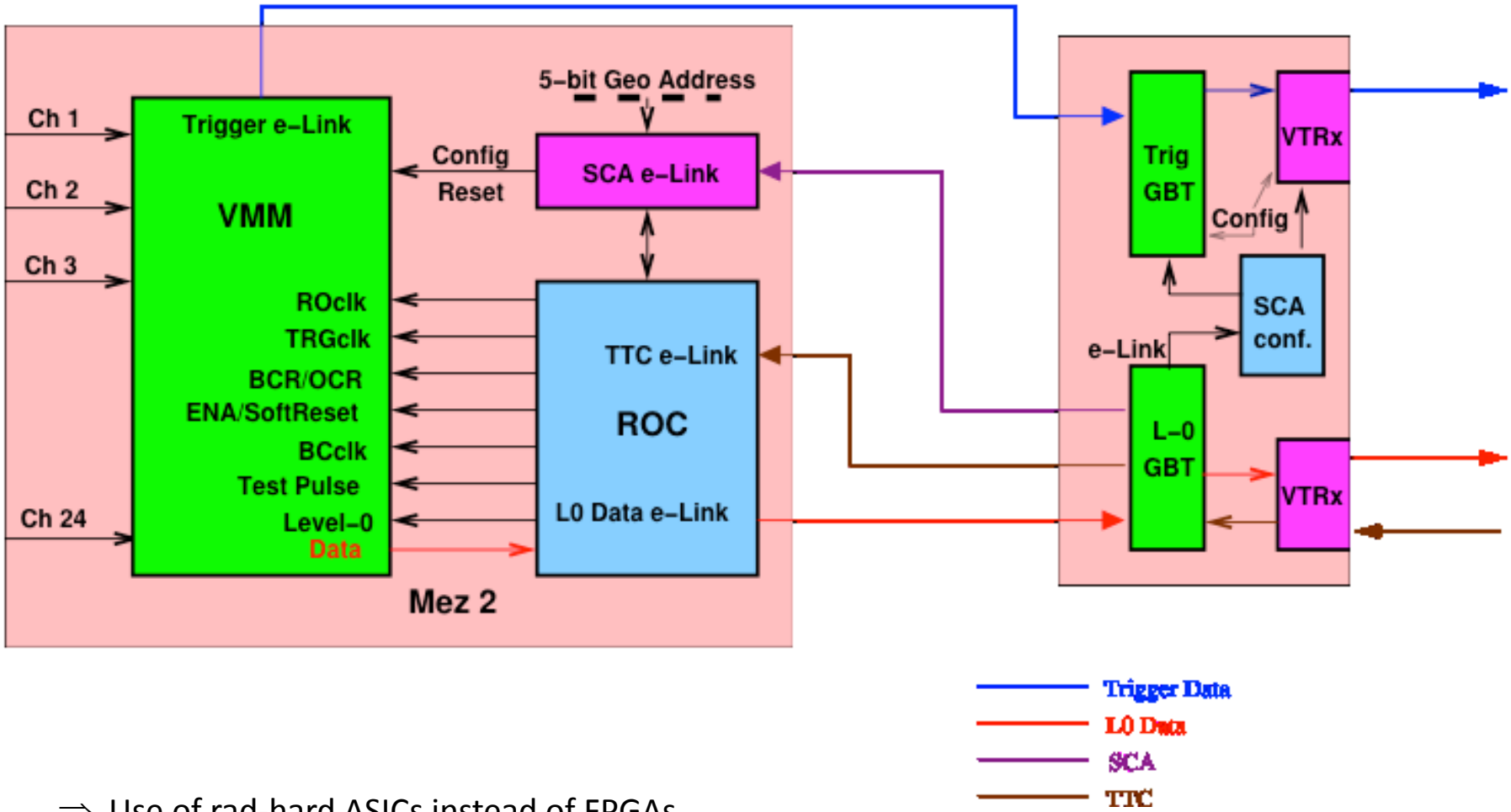


⇒ Keep cables (hard to change).

⇒ Improvements:

- Simplified infrastructure.
- Max. average hit rate per tube ≈ 380+ kHz.
- Total latency from muon event to data at USA 15 ≈ 3.1 μs.

Alternative System Re-Using NSW Hardware



⇒ Use of rad-hard ASICs instead of FPGAs.

⇒ For details, please see the poster of Mr. Venetios Polychronakos:
"The use of the ATLAS New Small Wheel front end Electronics for the HL-LHC MDT upgrade"

Data Latency: Tube -> ASD -> TDC -> CSM -> Optical Fiber -> Receiver/Processor

Phase 2 trigger-less data transfer (for both readout and L0 trigger):

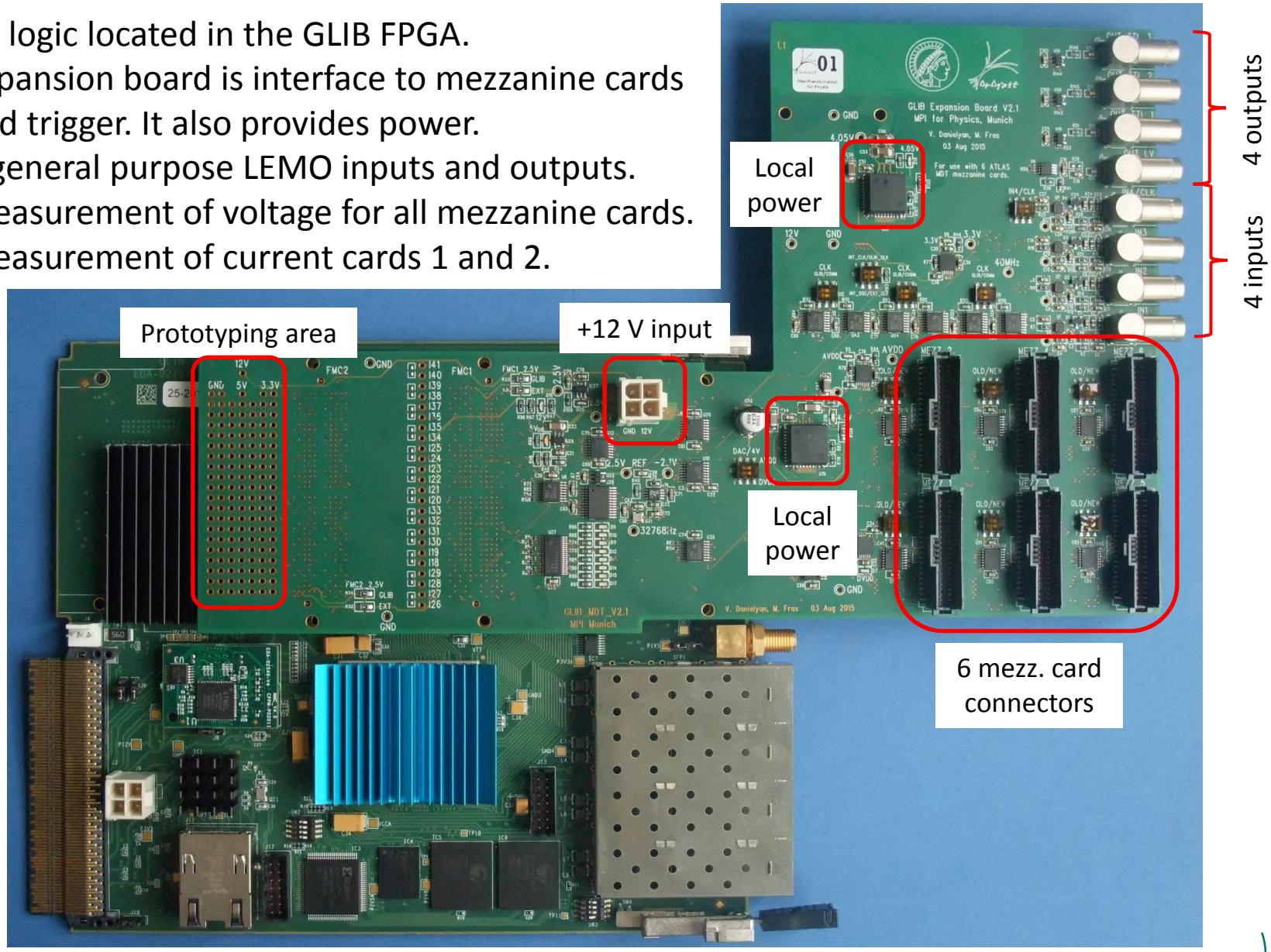
• Physical drift time in tubes	700 ns	tube physics
• Data processing	300 ns	estimation, round-robin mux @ 80 Mhz
• Transfer Mezz. -> CSM	880 ns	320 Mbps, 32 + 3 bits/word, 8 words
• CSM data processing	250 ns	estimation, round-robin mux @ 80 Mhz
• GBT encoding/decoding	430 ns	simulation, non lat-opt soft GBT
• Optical fiber to USA15	500 ns	100 m fiber, 5 ns/m
	≈ 3.1 µs	

Present system with triggered readout:

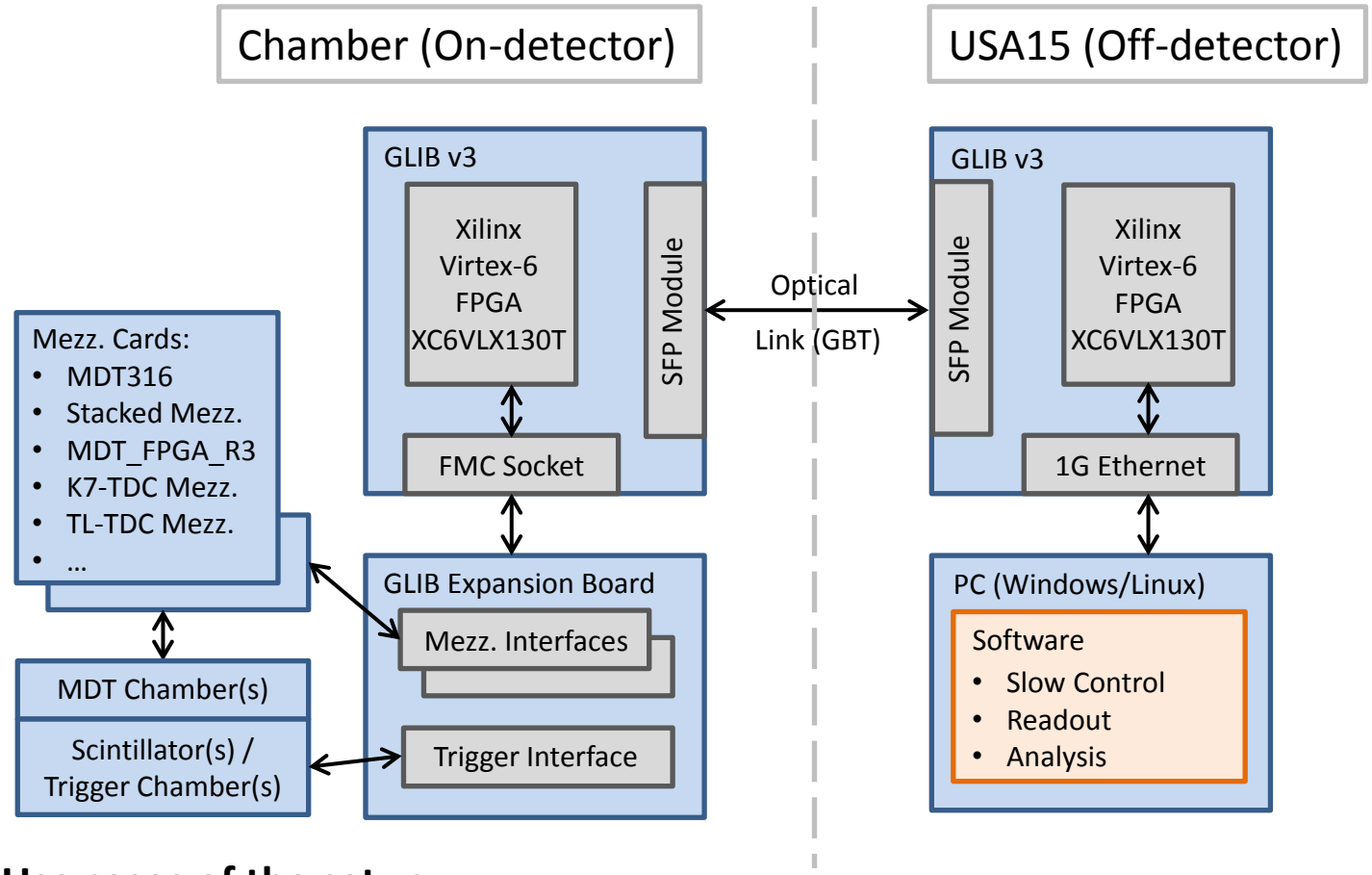
• Event to L1 trigger	2,050 ns	from ATLAS L1-Trigger TDR
• Transfer Mezz. -> CSM	7,000 ns	80 Mbps, 32 + 3 bits/word, 2 x 8 words
• CSM data processing	500 ns	estimation, round-robin mux @ 40 Mhz
• GOL encoding/decoding	400 ns	estimation
• Optical fiber to USA15	500 ns	100 m fiber, 5 ns/m
	≈ 10.5 µs	

Readout & Trigger Demonstrator – GLIB v3 + Expansion Board V2.1 (6 Channel Version)

- All logic located in the GLIB FPGA.
- Expansion board is interface to mezzanine cards and trigger. It also provides power.
- 4 general purpose LEMO inputs and outputs.
- Measurement of voltage for all mezzanine cards.
- Measurement of current cards 1 and 2.



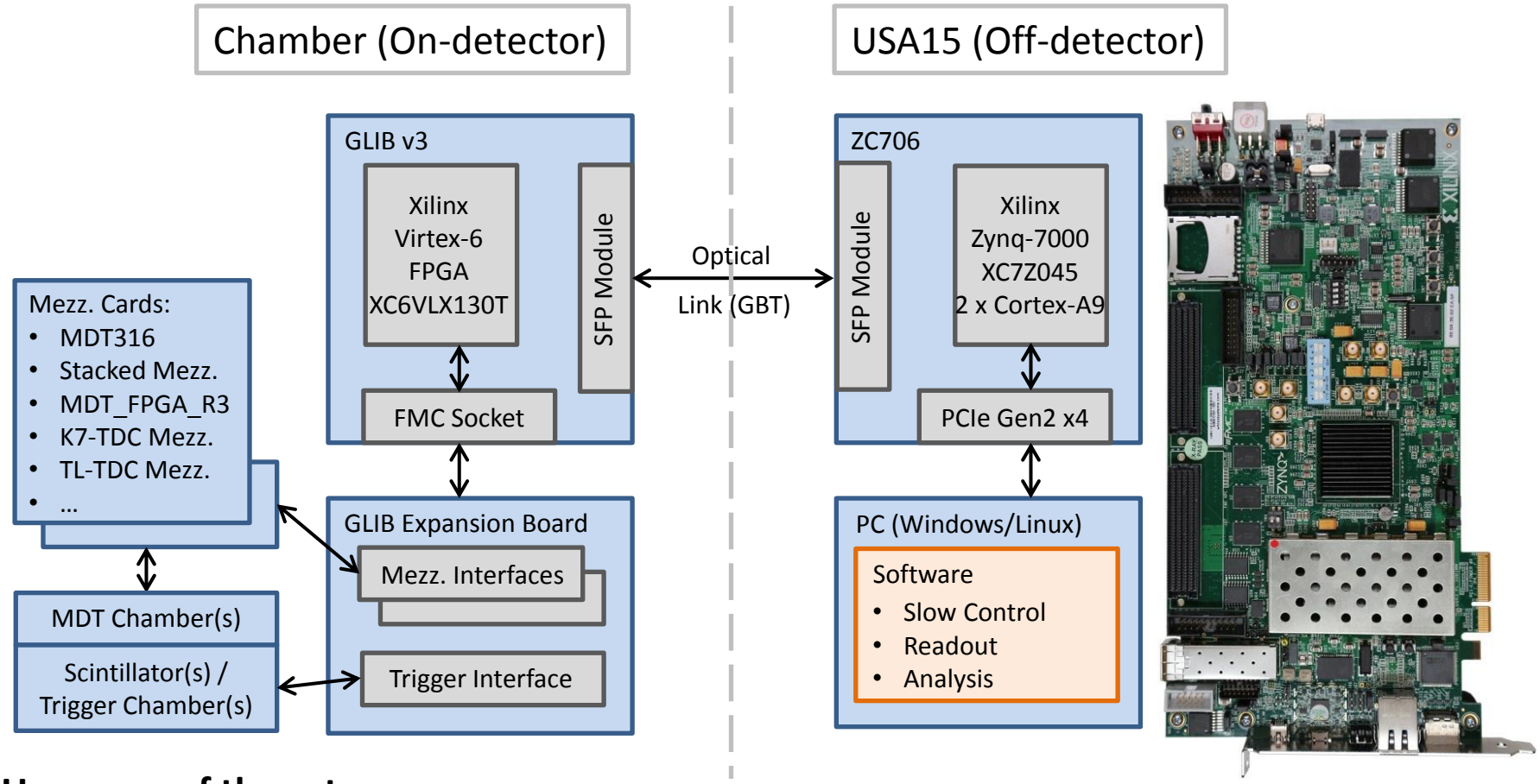
Full MDT Readout & Trigger Demonstrator Scheme Using two GLIB v3 Boards



Use cases of the setup:

- Prototype of new CSM with GBT optical interface for read-out + slow control (GBT).
- Light-weight test system for “old” (MDT316) and “new” (MDT_FPGA_R3 for trigger development, stacked mezzanine card for 15 mm tubes) and “future” (with Kintex-7 Soft-TDC or new TDC ASIC) mezzanine cards.

Full Readout & Trigger Demonstrator Scheme Using the GLIB v3 and Xilinx ZC706 Zynq Board

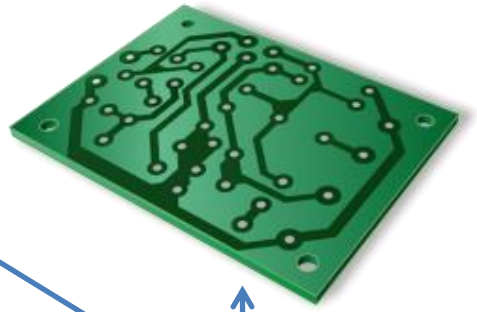


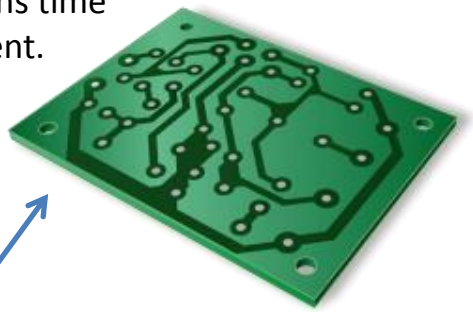
Use cases of the setup:

- Implement and test track-finding algorithm on ARM Cortex-A9 CPU.
- Test optical link for data read-out and slow control (GBT prototype).
- Fast data transfer via PCI express Gen2 x4, up to 2000 MB/s.
- Future prototyping of Advanced Buffer Logic (ABL) / Hit Extractor.

Mezzanine Cards and GLIB FMC Expansion Board for Readout & Trigger Demonstrator

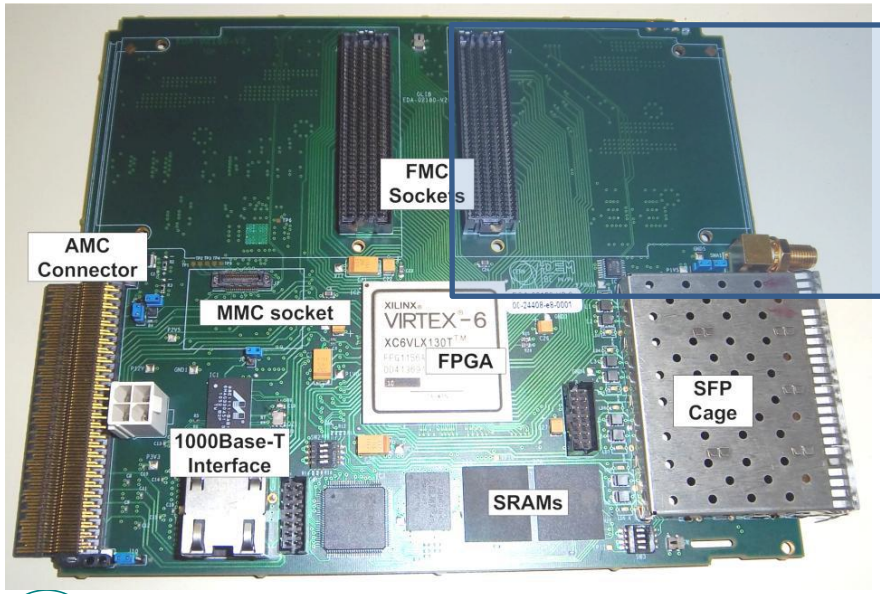
Kintex-7 card with soft TDC, 24 channel, 0,78 ns time resolution. Prototype for TDC ASIC development. Currently under development!





Future mezzanine card with rad-hard ASD2 and TDC ASIC.

MDT_FPGA_R3 mezzanine card with HPTDC and FPGA. It can generate trigger (fast TDC) data.
⇒ **To be replace by Kintex-7 card!**

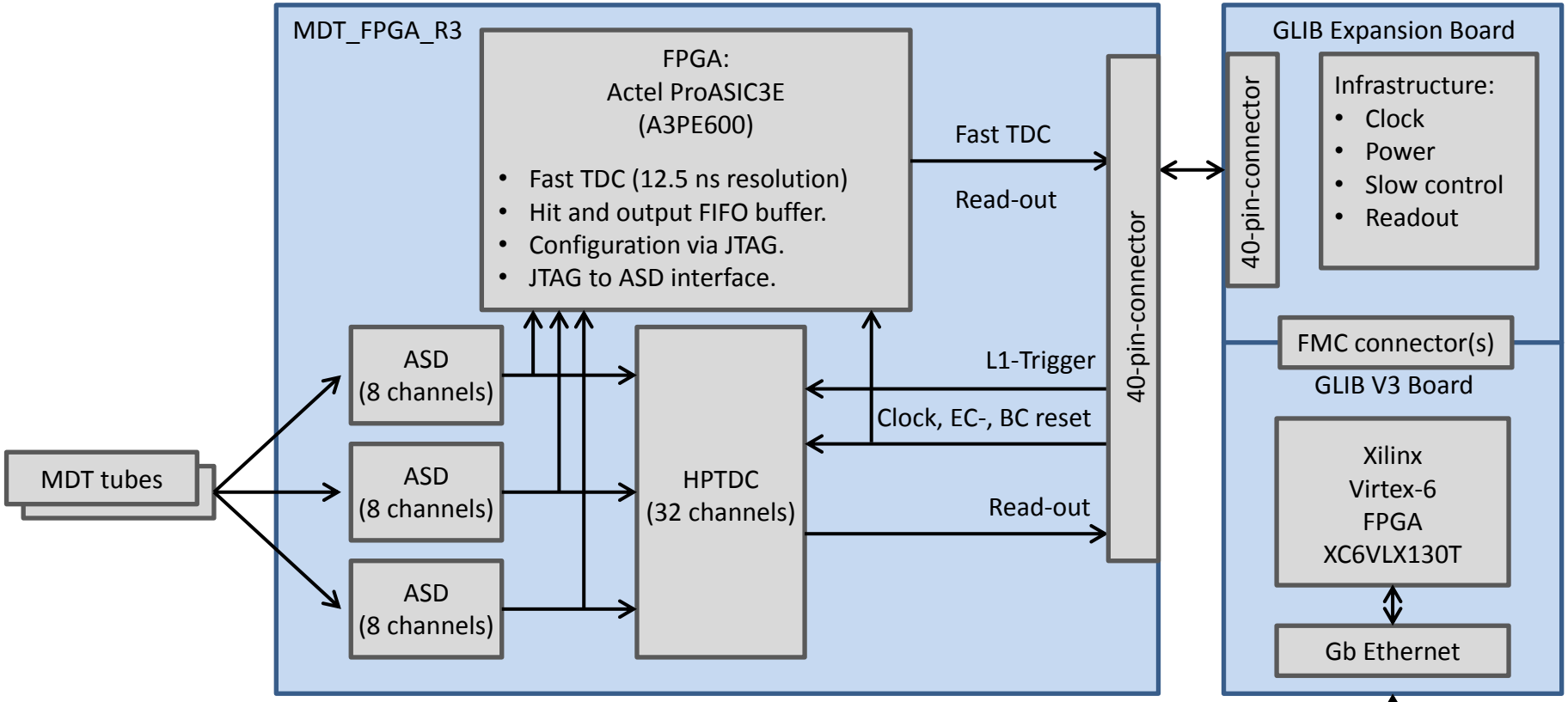


GLIB FMC Expansion Board

- Power Supply
- LHC clock, L1 trigger
- Scintillator(s) / Trigger Chamber(s)
- Trigger Logic

- Connect mezzanine cards with or without trigger feature.
- Control and read out via Gb Ethernet or fiber (GBT).
- Demonstrator for new CSM incl. MDT trigger.
- First prototype of data pre-processing for track finding.
- Demonstrator for GBT link.

Mezzanine Card for Trigger Data Generation (MDT_FPGA_R3)



Triggered (HPTDC) and trigger-less data (A3PE600 FPGA).

Use cases of the setup:

- Study function of fast TDC and data transmission/preprocessing.
- Collect data at GIF++ and test beam.

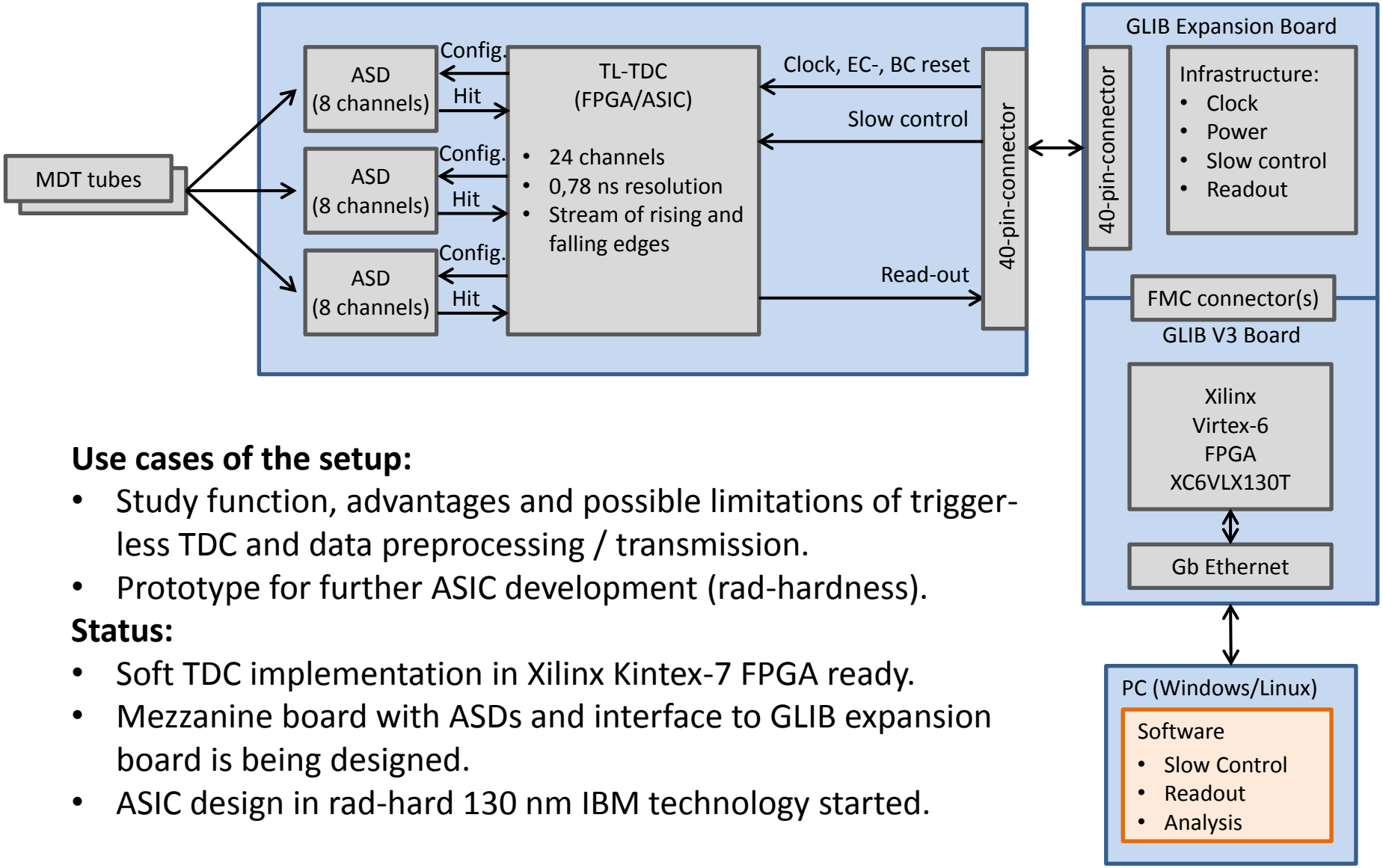
Status:

- Firmware of mezzanine card FPGA ready and tested.
- Data collected at GIF++ facility in August and October 2015.

PC (Windows/Linux)

Software
- Slow Control
- Readout
- Analysis

Future Mezzanine Card for Trigger-less Readout



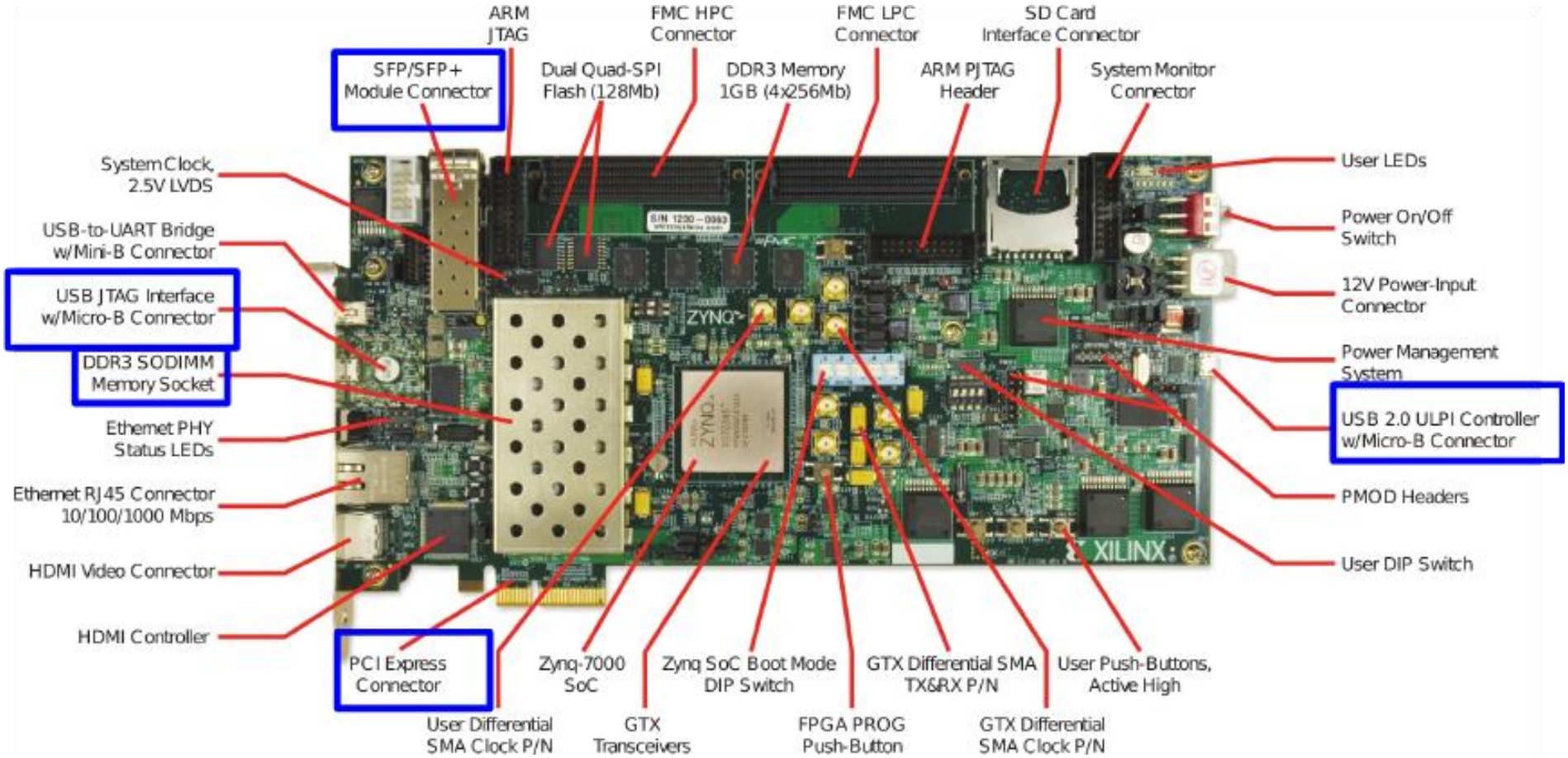
Use cases of the setup:

- Study function, advantages and possible limitations of trigger-less TDC and data preprocessing / transmission.
- Prototype for further ASIC development (rad-hardness).

Status:

- Soft TDC implementation in Xilinx Kintex-7 FPGA ready.
- Mezzanine board with ASDs and interface to GLIB expansion board is being designed.
- ASIC design in rad-hard 130 nm IBM technology started.

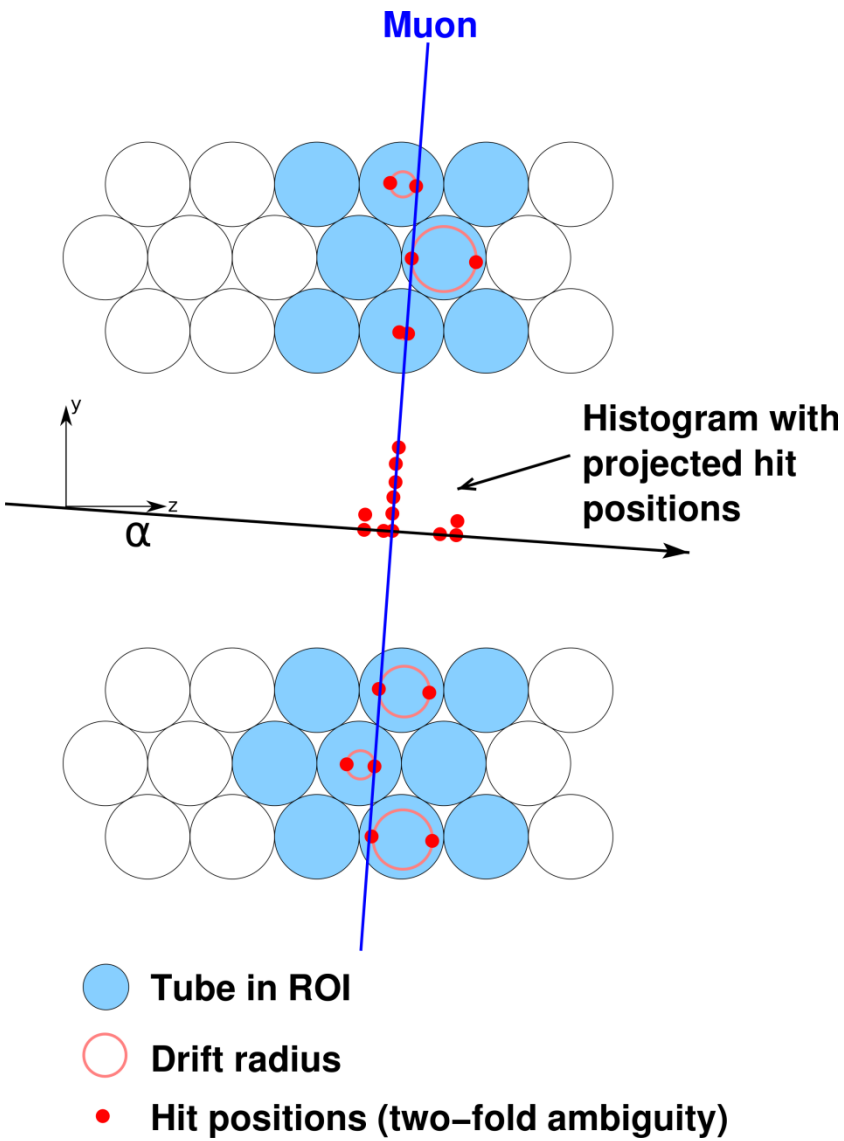
Xilinx Zynq-7000 Evaluation Board ZC706 for Track Finding Implementation



Xilinx Zynq-7000 (XC7Z045 All Programmable FFG900 -2 SoC) :

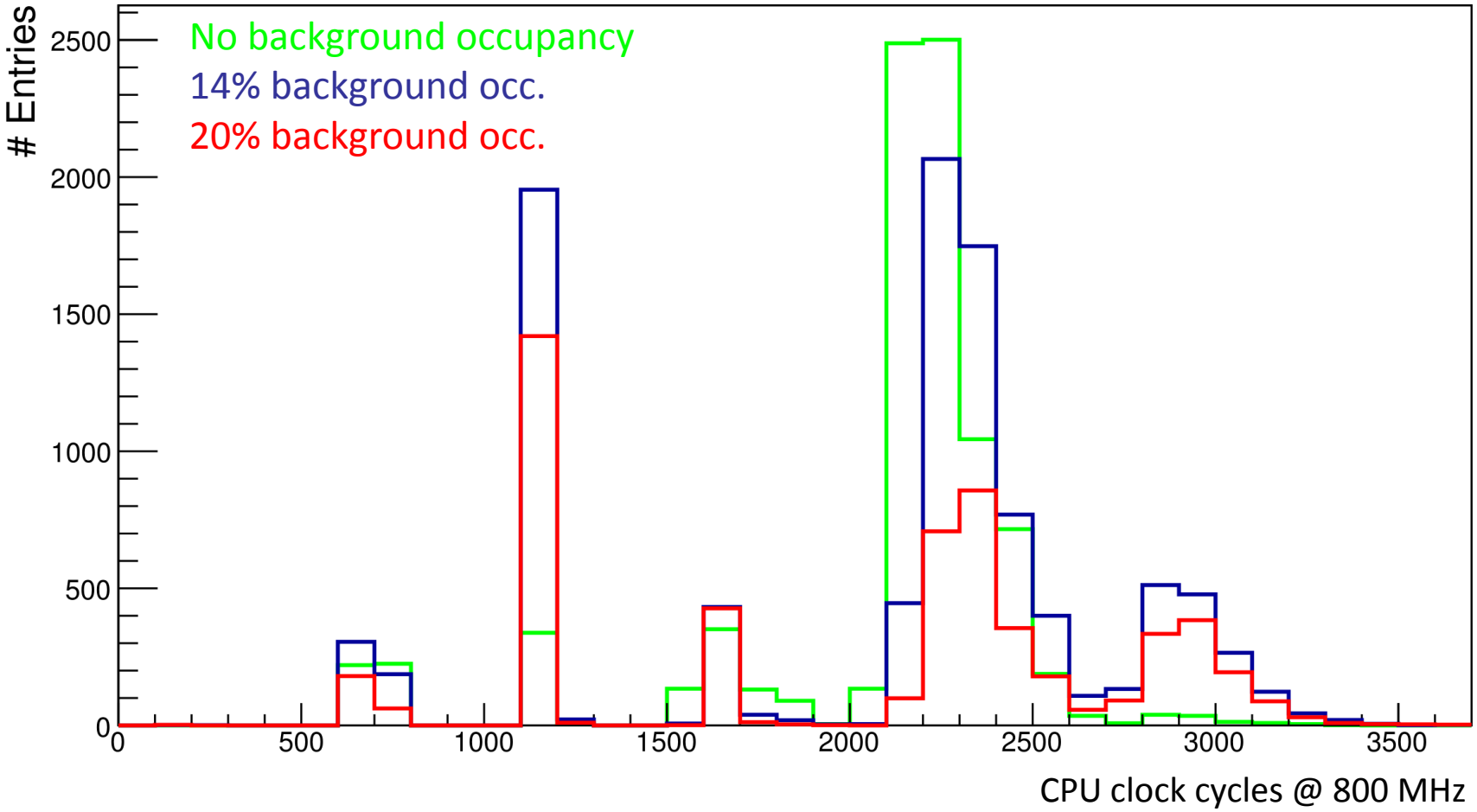
- FPGA (Kintex-7 equivalent): 350k logic cells, 19.1 Mb block RAM, 900 DSP slices
- Dual-core ARM Cortex-A9 CPU (32kB L1 Cache) @ 800MHz (1 GHz with speed grade -3)
- Interfaces: USB for debug, PCIe for PC link, SFP+ for optical link (GBT) to front-end.

Implementation of a Fast Track Finding Algorithm



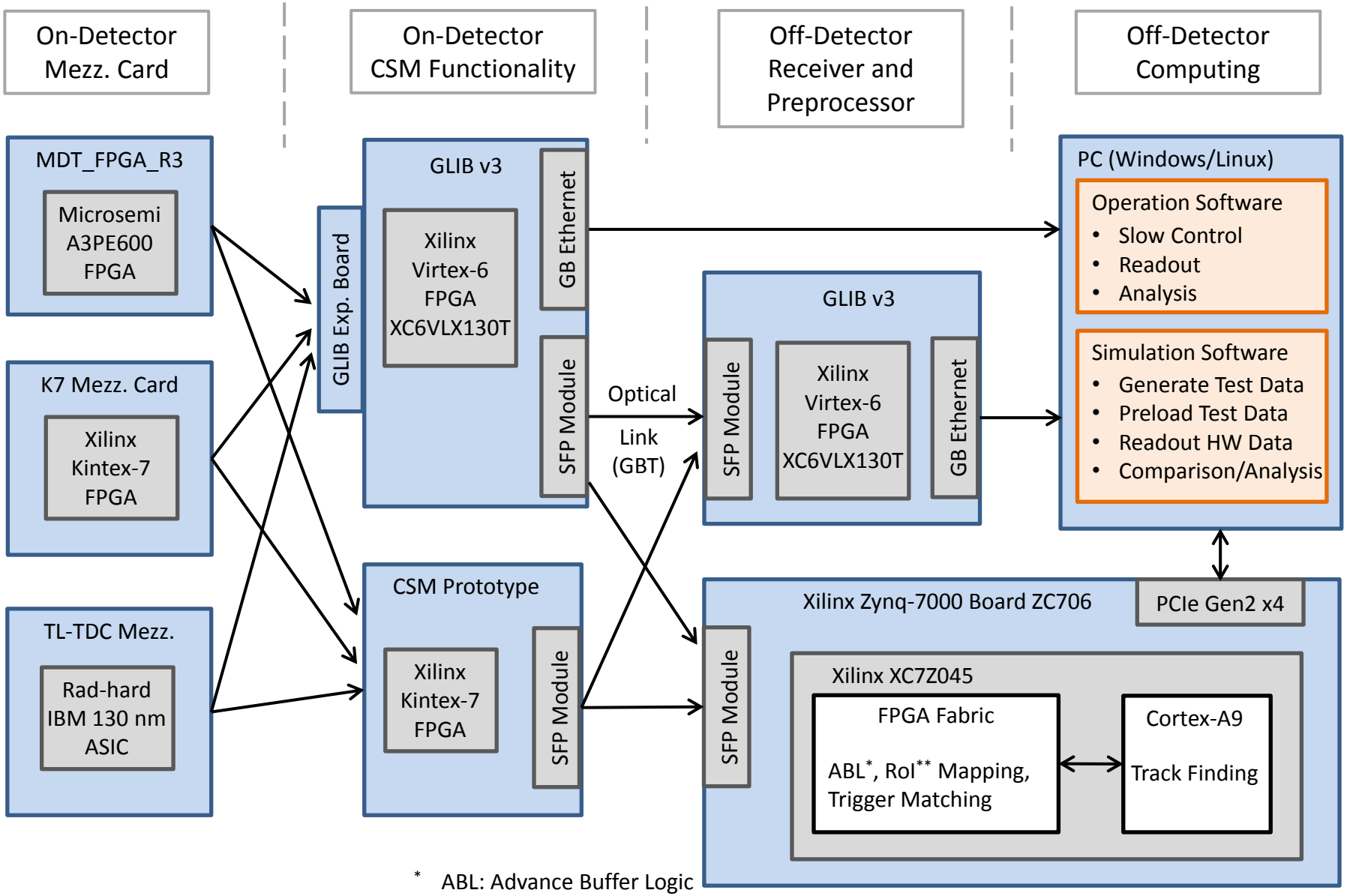
- Track finding with drift tube chambers is based on track information of primary trigger chambers (region of interest and angle).
- Algorithm uses Hough-Transform with fixed angle for pattern recognition and then performs linear fit.
- FPGA part is used for buffers, CPU for floating point operations.
- Implementation in ARM Cortex-A9 assembly language in order to make use of the media engine of the CPU.

Processing Duration for Muon Track Reconstruction



- Data taken at the CERN GIF (γ-irradiation).
- Track can be reconstructed in less than 3500 clock cycles (4.375 µs).
- Processing time can be further reduced by using second CPU core and FPGA for parts of the algorithm.

Outlook: Readout & Trigger Demonstrator – Hardware Matrix



* ABL: Advance Buffer Logic
** RoI: Region of Interest

Readout & Trigger Demonstrator – Scenarios for 2016/2017

Possible scenario for summer 2016:

- MDT_FPGA_R3 board with Fast TDC:
  Proposed new output format, serial speed 320 Mbps, unused bits filled with zeros.
- Control and readout via Gb Ethernet using GLIB v3 + expansion board.
- No optical link for data transmission.

Likely scenario for summer 2016:

- Like above, but:
- Control via Gb Ethernet using GLIB v3 + expansion board.
- Data transmission using an optical link (possibly 3,125 GB/s) between two GLIB v3 boards, data readout via GB Ethernet.

Likely scenario for fall 2016:

- Like above, but:
- Data transmission using an optical link between a GLIB v3 and the Xilinx ZC706 board, data readout via PCIe Gen2 x4.

Desirable scenario for end of 2016/beginning of 2017.

- Like above, but:
- Usage of Kintex-7 mezzanine card with soft TDC.
- Control of front-end electronics via the Xilinx ZC706 board.

Conclusions

- Combined trigger-less MDT data transfer for readout and L0 high p_t muon trigger in ATLAS phase 2.
- Readout and slow control via optical fiber (GBT).
- Improved latency to achieve high p_t muon trigger of 6 µs.
- Demonstrator hardware partially ready:
  - "CSM prototype" based on the GLIB + expansion board. This will be replaced by a real CSM board, preferably fitting on the CSM motherboard.
  - Mezzanine card with HPTDC and Fast TDC in Microsemi ProASIC FPGA used for first studies.
  - A Kintex-7 mezzanine card with soft TDC is mandatory for a realistic test. This will be an important prototype for the final TDC ASIC development.
  - Xilinx ZC706 board will be used as GBT receiver and data processor for readout and track finding.
- Performance studies of algorithms for track reconstruction.

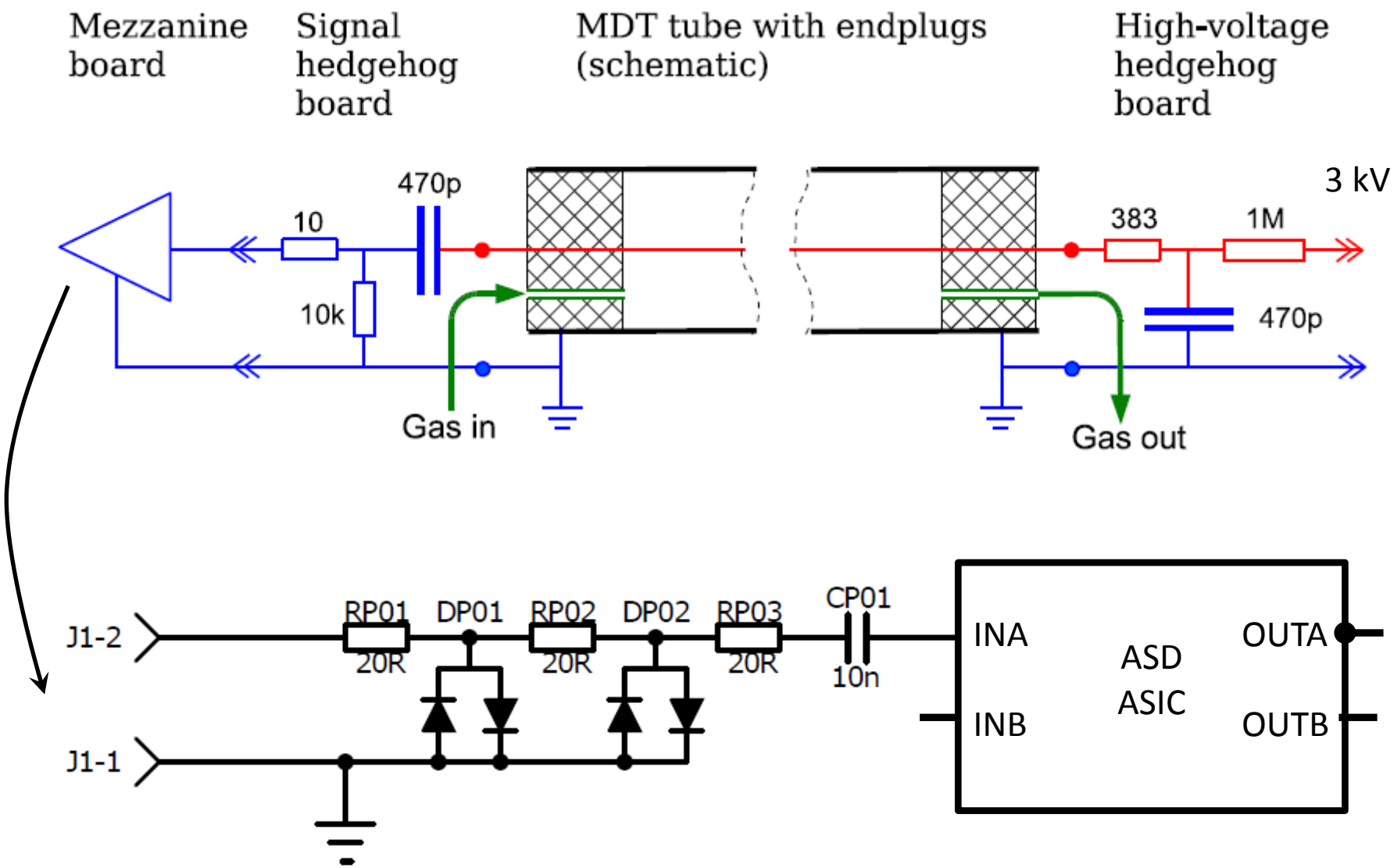
Thank You for Your attention!

Questions or remarks?

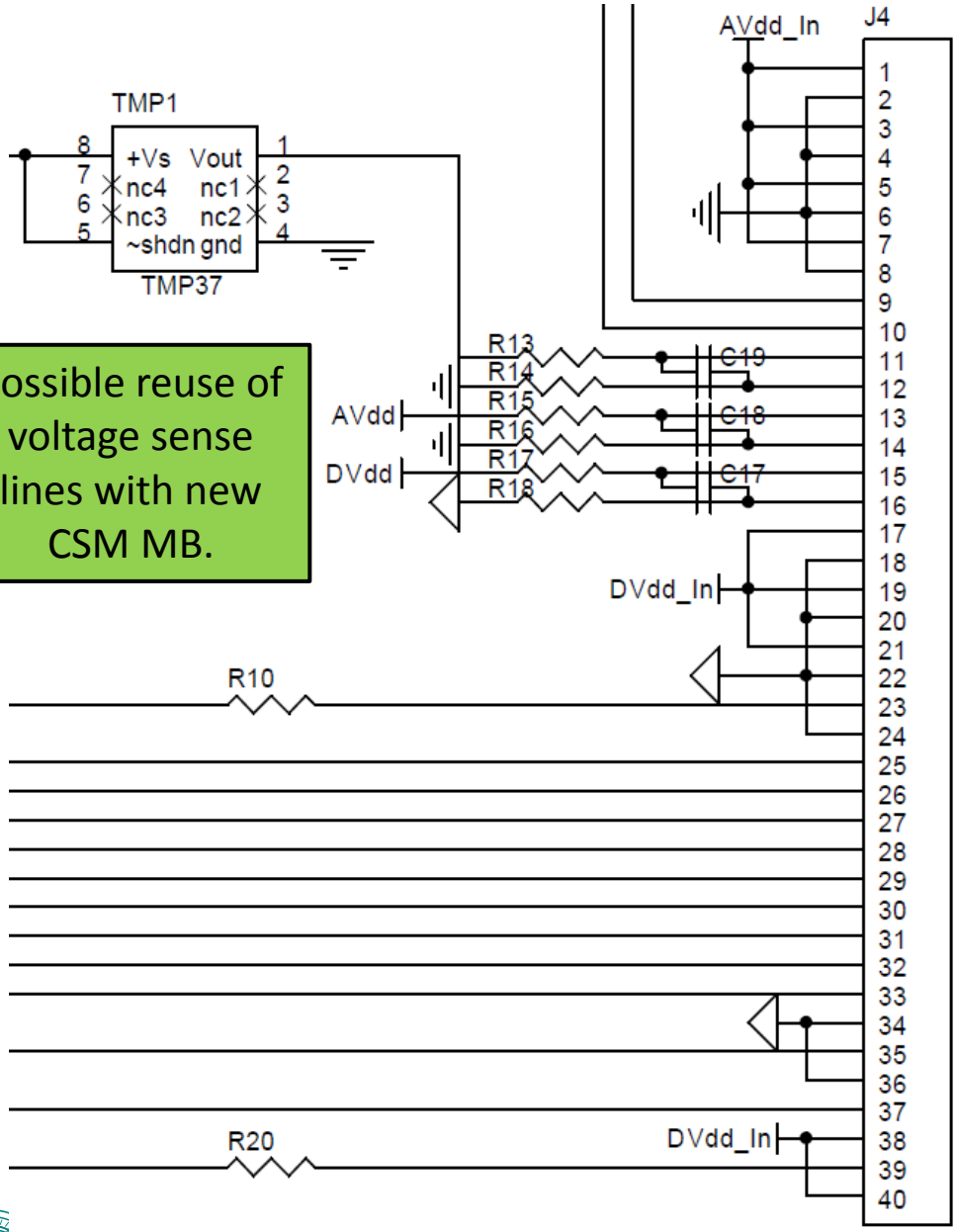
Thanks for Your attention!

Backup Slides

MDT Tube with Readout and HV Side



Mezzanine Card Connector Pinout on MDT316 and MDT_FPGA_R3



MDT316 – MDT_FPGA_R3

Possible reuse of voltage sense lines with new CSM MB.

Cal. => Trig Ctrl (in)

Temp. Sense * => SDat 2 (out)

3 extra pairs available, if temperature sensing and generation of calibration pulse is done on the mezzanine card.

SDat

SClk

ENC

Strobe => Trig SDat (out)

TMS

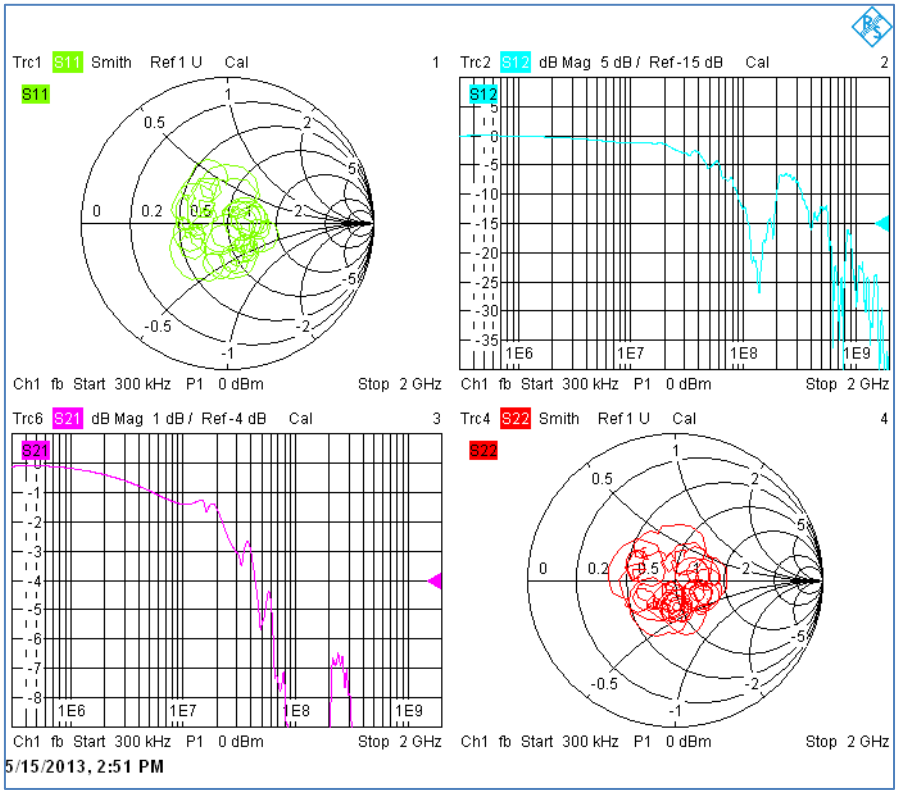
TCK

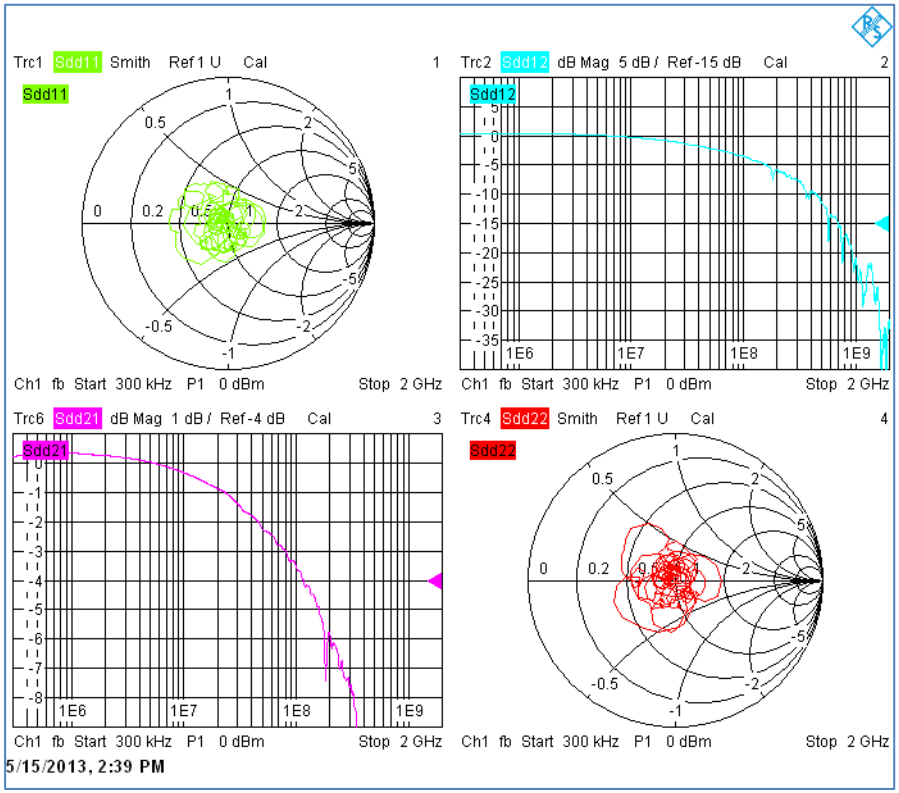
TDI

TDO

* no diff. routing

40-pin Flat Cable, 5.00 m – S-Parameter Measurement



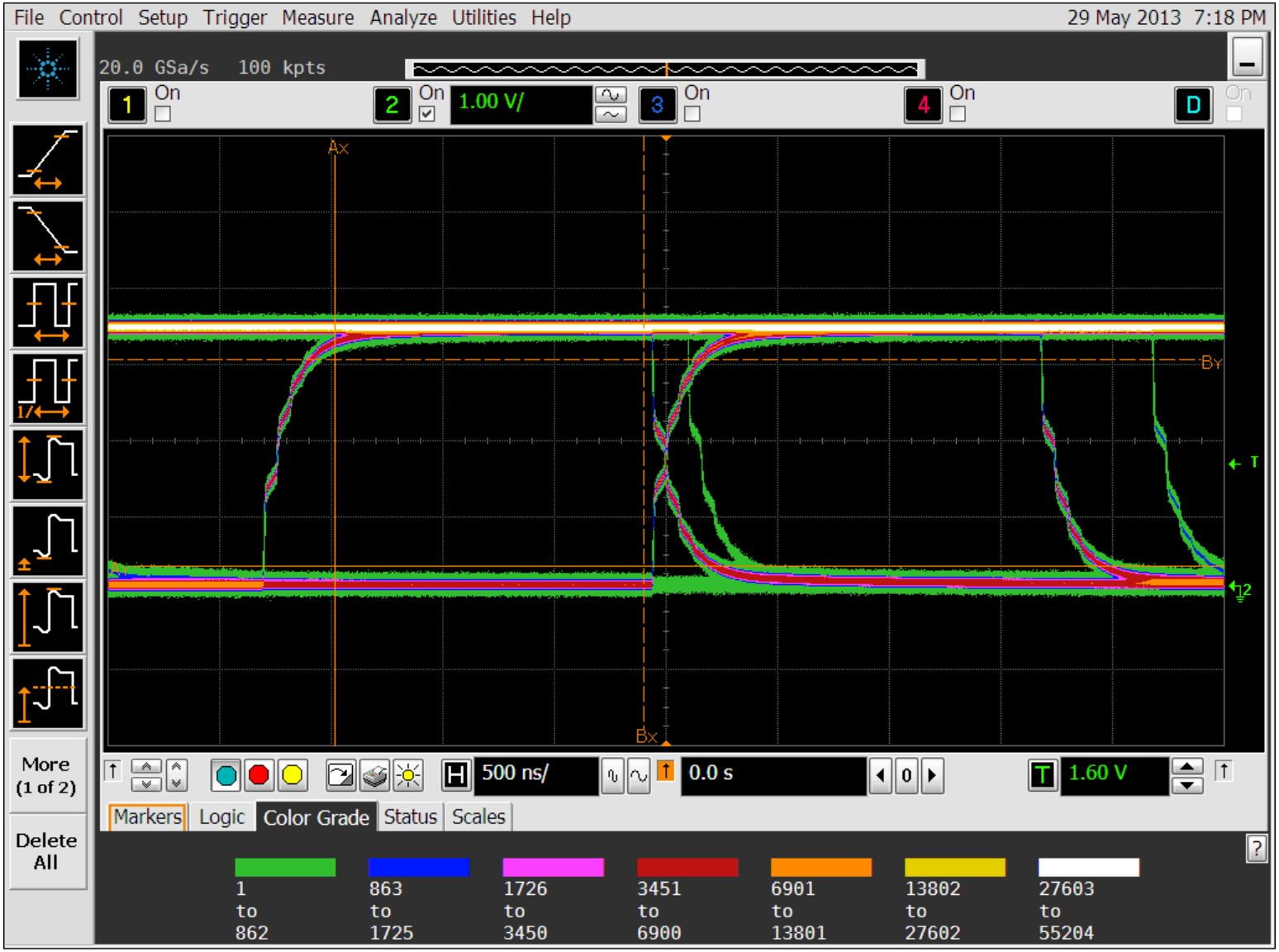


Single-ende: -3dB @ 40 MHz

Differential: -3dB @ 80 MHz

40-pin Flat Cable, 5.00 m, 80 Mbps Differential Eye-diagram

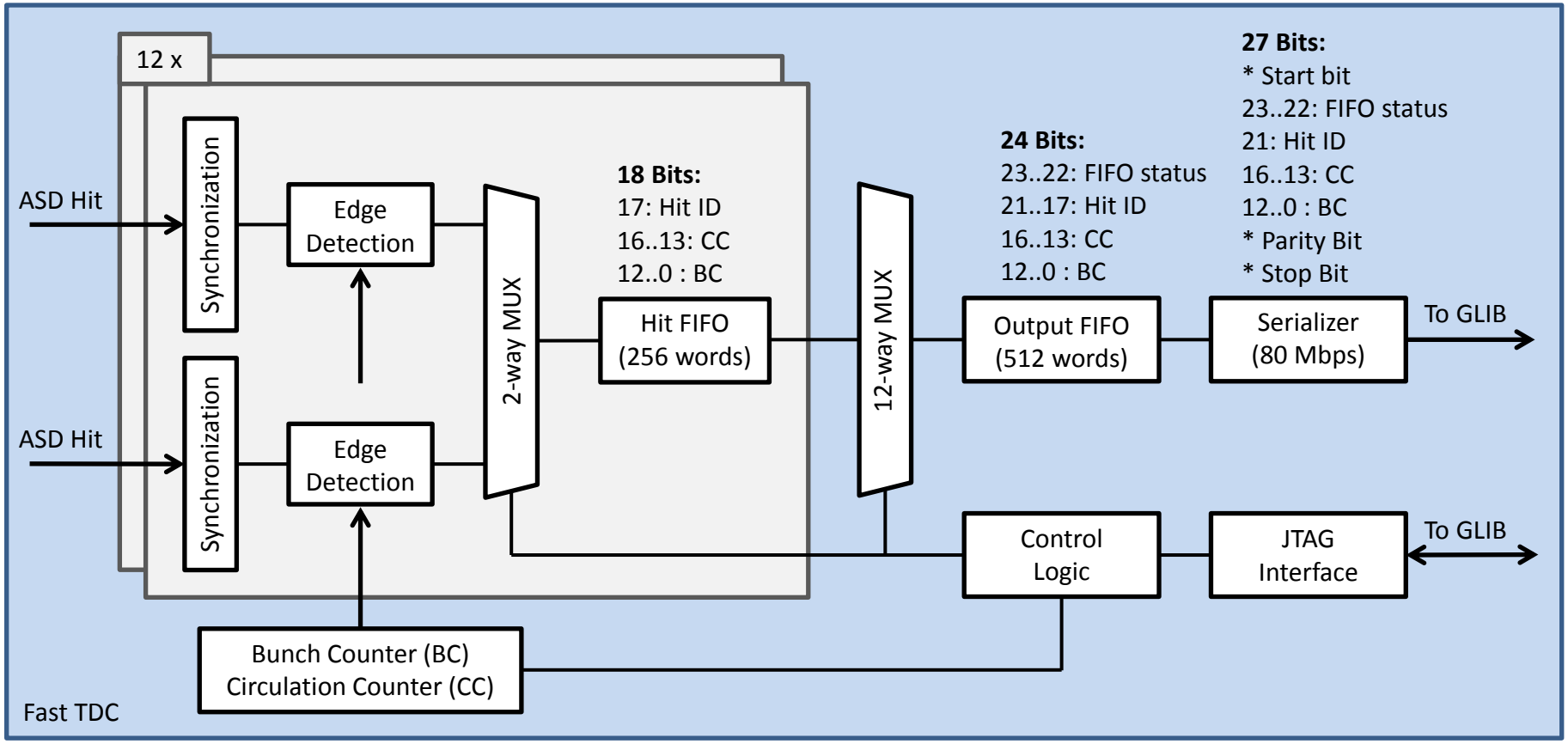
40-pin Flat Cable, 5.00 m, Single-ended JTAG Signals



Fast TDC on the MDT_FPGA_R3 Mezzanine Card inside Actel ProASIC3E

Features:

- 12.5 ns resolution on rising edges, no dead-time.
- Trigger-less operation: Transmit all data @ 80 Mbps (320 Mbps on 2 lines planned).
- 256 word hit FIFO (shared between 2 channels), 512 word output FIFO.
- Tunable FIFO sizes (via JTAG) and other features for monitoring and debugging.



New MDT TDC (MDT_FPGA_R3, Kintex-7, TL-TDC ASIC) – Serial Data Format

Features:

- Transmit all data to the GLIB exp. board: @ 80 or @ 320 (2 lines á 160) Mbps.
- Proposed serial data format with 35 bits: 32 bit user data, 3 bits of overhead

  * Start bit

  31..29: 3 FIFO or other status bits (overflow, error, …)

  28..25: Hit ID, i.e. ASD channel 0..23 (+ 8 possible status/debug words)

  24..20: Pulse length, 1 BC resolution, 0 .. 775 ns range

  19..17: Circulation counter, extends search time to > 800 µs

  16..5: Coarse time, up to 4095 BC = 102,3 µs

  4..0 Fine time, BC / 32 = 0,78 ns

  * Parity bit

  * Stop bit

⇒ Supports an average hit rate per tube of up 380 kHz.

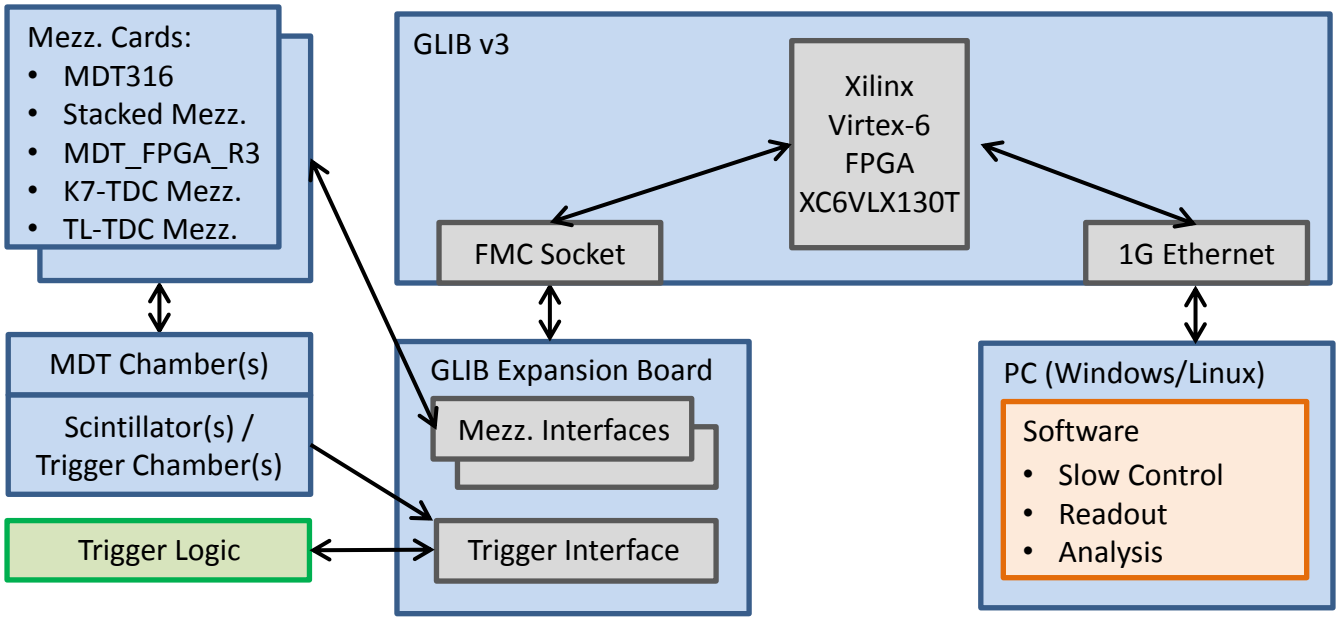
⇒ Max. average hit rate per tube of up to 570 kHz with 3 serial lines.

⇒ 160 Mbps seem to be feasible with the current cables.

⇒ No special encoding and/or signal integrity measures necessary, i.e. simplified TDC ASIC design and flexibility in technology.

⇒ Fits the default native 32 bit word size of the GLIB.

Readout & Trigger Demonstrator Simplified Scheme Using the GLIB v3



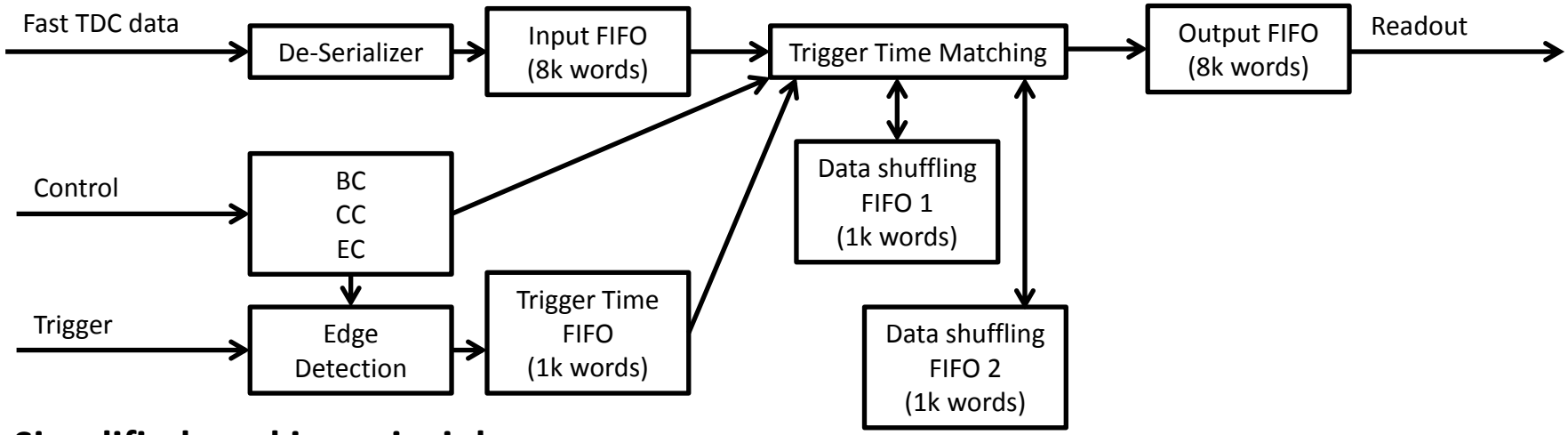
Use cases of the setup:

- Light-weight test system for up to 6 mezzanine cards.
- Prototype for gathering data for readout, track-finding and trigger algorithm.

Status:

- 2 channel and 6 channel expansion boards ready.
- Firmware and software development for all current MDT mezzanine cards done (MDT316, MDT_FPGA_R3 with Fast TDC, stacked mezzanine card for 15 mm tubes).
- Setup has been successfully used with 2 cascaded 6-channel cards, i.e. 12 mezzanine cards in total, at the GIF++ facility of CERN in August and October 2015.

Trigger Matching Scheme of Fast TDC Data on the GLIB FPGA



Simplified working principle:

- Get all data from input FIFO and store them in data shuffling FIFO 1.
- Read fast TDC data word by word from data shuffling FIFO 1.
- While reading, check the timestamp of the data word. According to the result, it is:
  - Copied to the second shuffling FIFO or discarded (if too old).
  - Copied to the output FIFO (if it is within the specified match window).
- Start over with shuffling FIFO 1 and 2 swapped.

Features:

- Matching window of max. -BC_rollover .. +BC_rollover, i.e. -4095 * 25ns .. +4095 * 25ns.
- Programmable time for discarding data of 0 .. +BC_rollover.
- Programmable time for proceeding to the next trigger event of 0 .. +BC_rollover.
- Output words can be selected similar to HPTDC: header, trailer, data, status, debug
- Detailed monitoring of FIFO statistics and flags.