ATLAS CALORIMETERS BACK-END ELECTRONICS AT HL-LHC

09/03/2016

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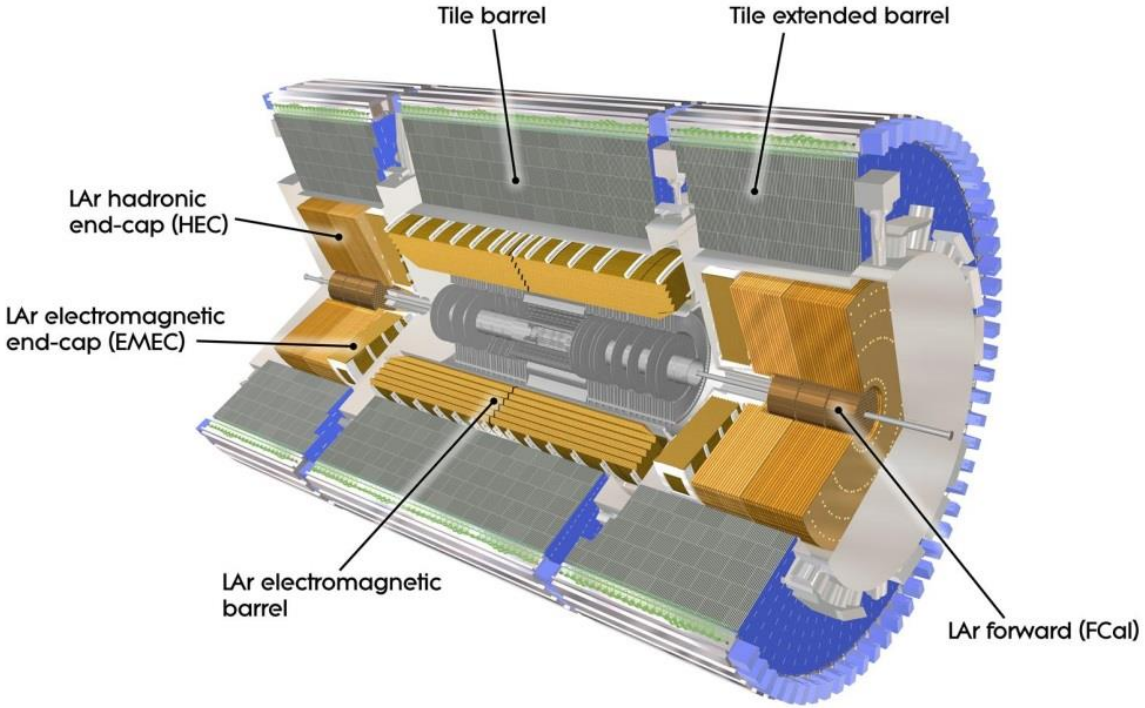
On behalf of the ATLAS collaboration

Outline

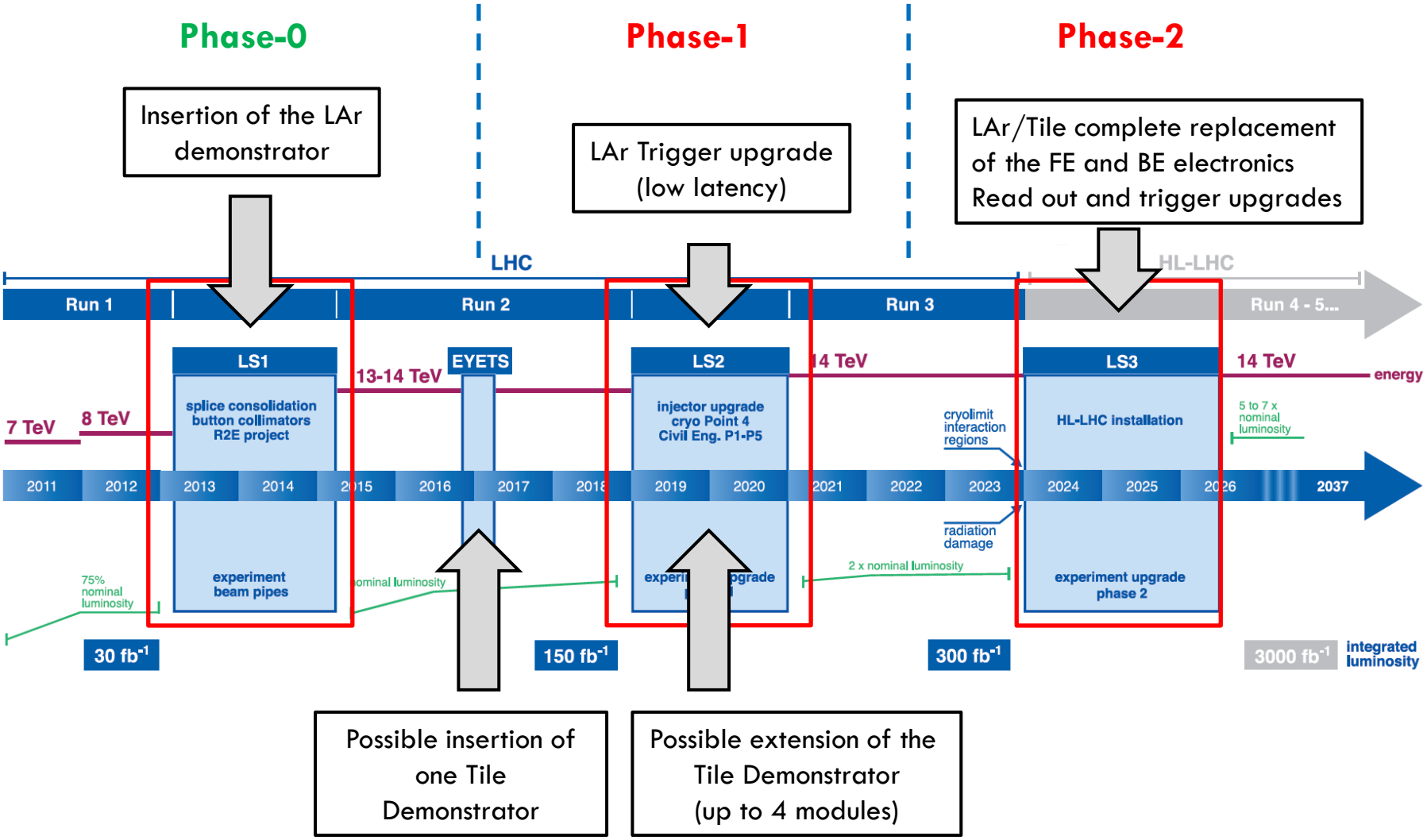
- Calorimeters upgrade
- Upgrade plans
- LAr back-end upgrades
  - Phase I and Phase II
- Tile back-end upgrades
  - Demonstrator and Phase II
- Conclusions

Calorimeters upgrade

- Full digital trigger architecture – Phase I
  - Higher granularity and improved resolution to the Level0/1 trigger processors
  - Level 0: 1 MHz trigger rate → Phase II
- New readout strategy – Phase II
  - All samples will be transmitted to the back-end electronics every bunch crossing
  - Major replacement of the front-end and back-end electronics



Upgrade plans



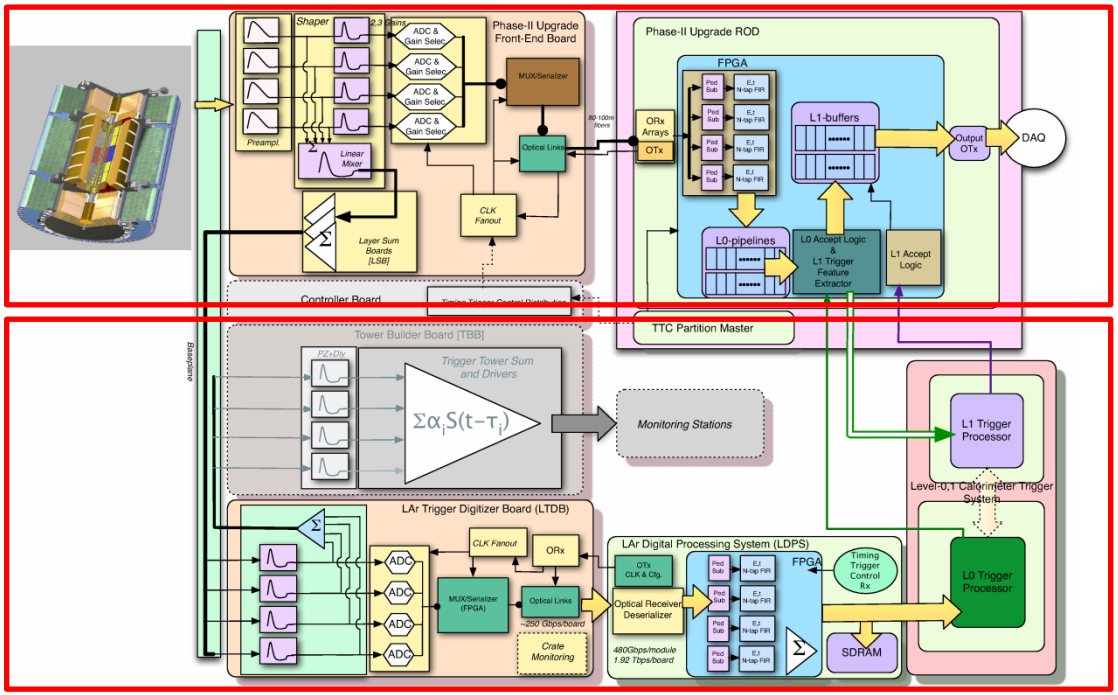
LAr back-end upgrades

LAr back-end upgrades

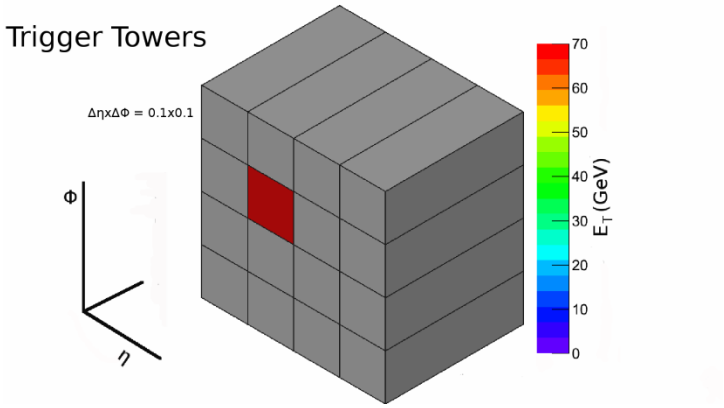
- Phase I: Trigger system upgrade
  - Installation of the new digital trigger path with L1Calo system
- Phase II: Back-end electronics system will be optimized for high pile-up data taking
  - Replacement of the back-end readout electronics: LAr Pre-Processor (LPPR)
    - New digital filtering algorithms for energy reconstruction
  - Implementation of new trigger interfaces with L0 and L1 trigger systems

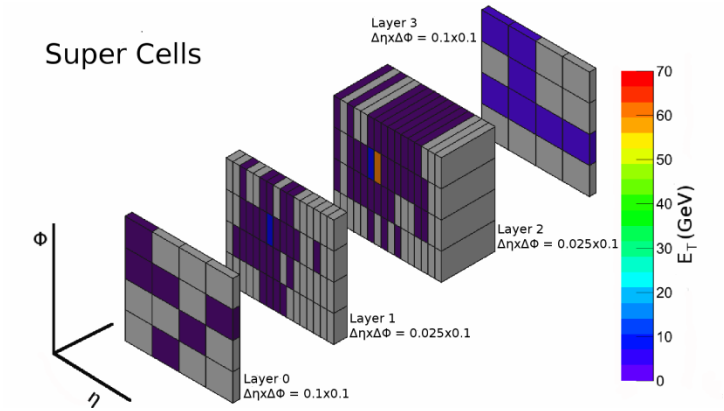
Phase II (DAQ)

Phase I (Trigger)



LAr Phase-I upgrade

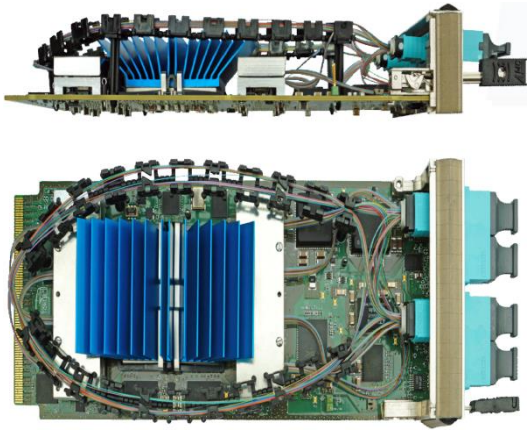




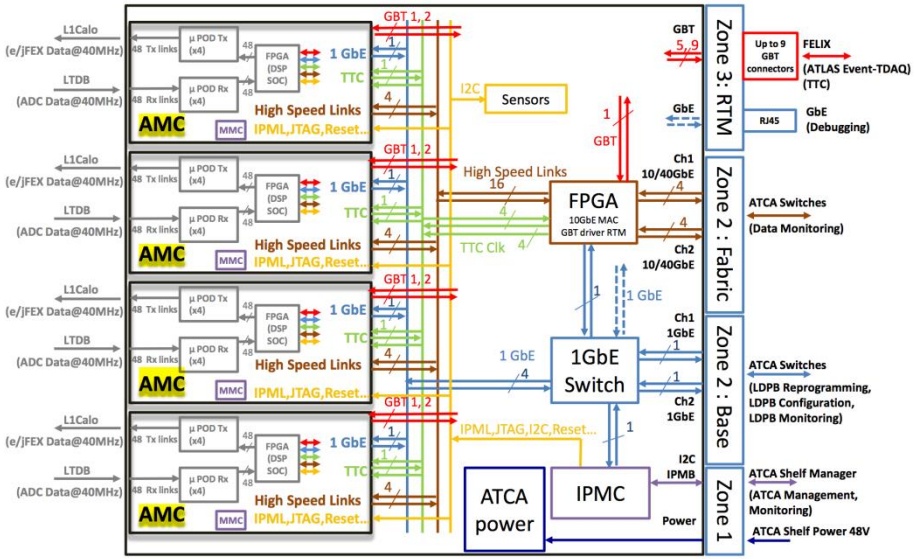
- LAr trigger electronics upgrade planned for ~2019
  - Order of magnitude increase in granularity to Level 1 trigger
- Level 1 trigger system will receive new sums for each layer with higher granularity: Super-Cells
- Study and implementation of new algorithms at Level 1
- Super-Cells are digitized at 12bits@40 MHz
- Complete redesign of the L1Calo interface
  - LAr Digital Processing System (LDPS)
- Sums are processed by the LDPS and sent to three feature extractors (FEXs)
  - eFEX, jFEX and gFEX

LAr Digital Processing System – Phase I

- Digital signal processing on Super-Cells in real time
  - Precise E_T measurement
  - Pile-up suppression
  - Bunch crossing assignment
- LDPS receives digital data at 25 Tbps
- Transmits processed data to L1Calo system at 41 Tbps
- Total of 32 LAr Digital Processing Blades (LDPB) compose the LDPS
  - Handles ~1100 Super-Cells in average
- Hardware
  - ATCA carrier blade each with 4 AMC cards
  - Each AMC contains an Altera Arria 10 FPGA
  - 4 TX MicroPODs + 4 RX MicroPODs
- Sucessful link test done with gFEX + FELIX last month
- No hardware update is expected for Phase II



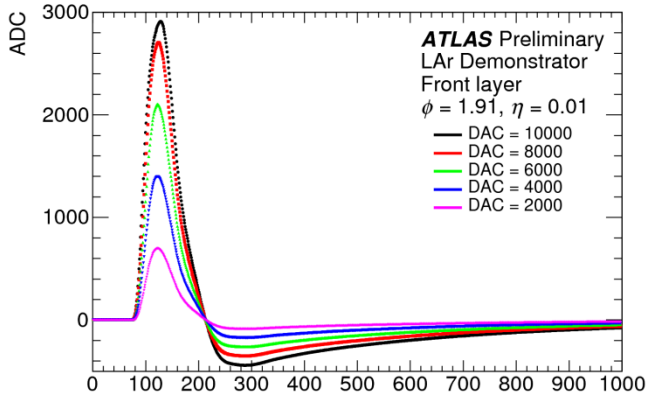
LATOME AMC board



LDPB prototype demonstrator – Phase I

- Pre-prototype of the LDPB for the LAr demonstrator
  - Fully compliant ATCA blade
- Two Front FPGAs (Altera Stratix IV)
  - Receives digitized data from one LTDB
  - Stores data in circular buffers with a depth of 2.5 μs
  - Format them in ATLAS RAW Event Fomat
- One Back FPGA (Altera Stratix IV)
  - Readout through10 Gbps Ethernet network
    - Data readout with Fabric Interface using IPbus protocol
- Optical communication with front-end
  - 40 optical RX links@ 4.8 Gbps, 8B10B encoding
  - Continuous data stream of 320 Super-Cells from one LTDB
- Interconnectivity between FPGAs
  - 8 RX/TX links up to 8.5Gbps, XAUI protocol@3.125 Gbps
  - 16 LVDS links up to1.6Gbps between FPGAs
- 2 boards were installed in USA15 during summer 2014 for the **LAr demonstrator**
- Tested during data taking 2015 with calibration system and with collision data

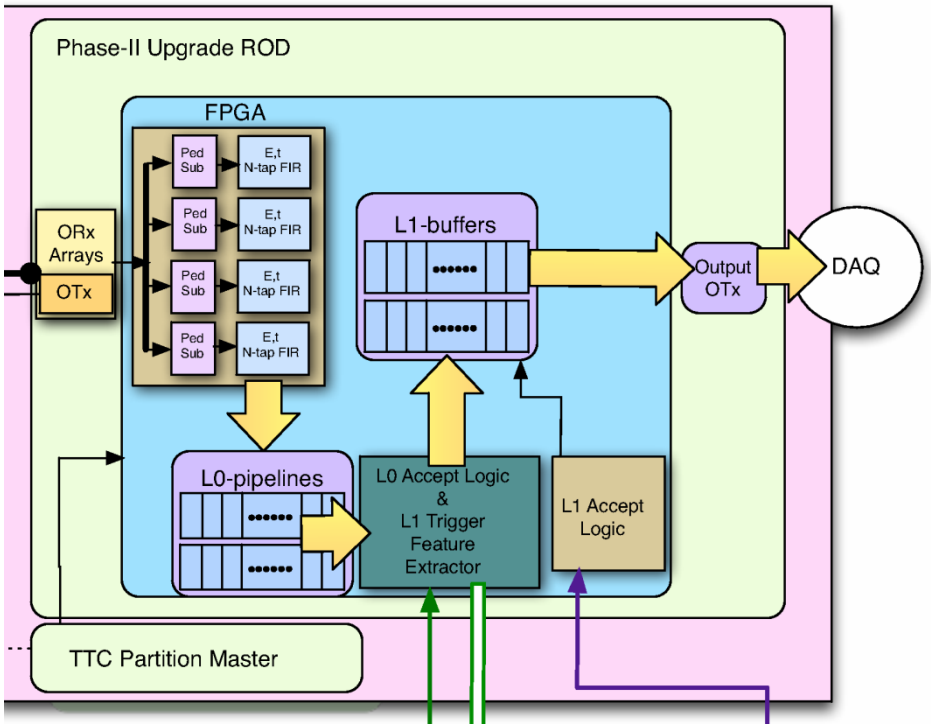
LDPB prototype (ABBA)



Pulse shapes of a Super Cell for injected calibration pulses

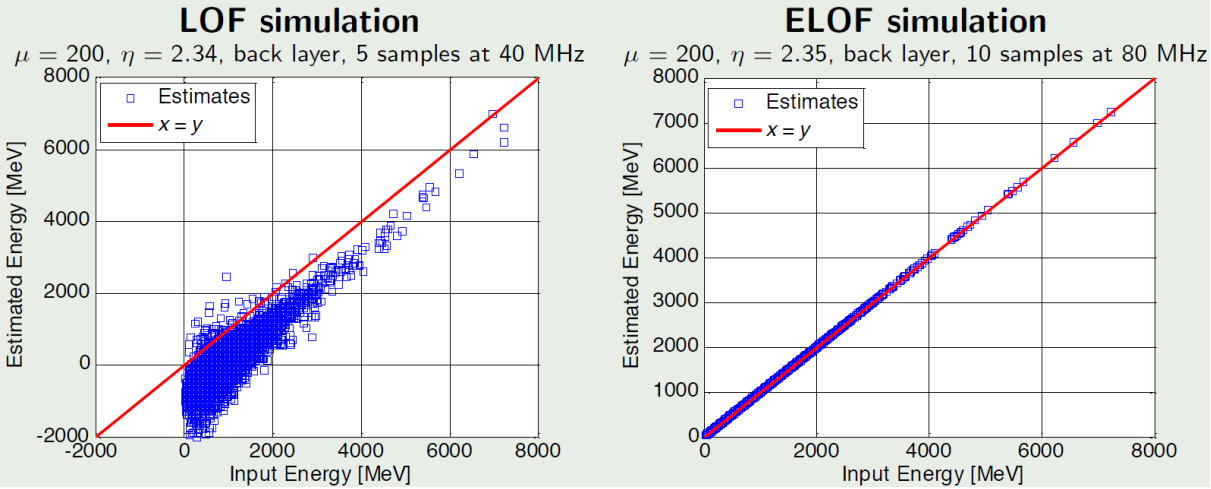
LAr Pre-PRocessor – Phase II

- Natural evolution of the LDPS developed for Phase I
  - Faster input links – LpGBT
  - Fiber re-mapping plant
- 60/120 LPPR boards in ATCA format
- Each LPPR will host 4 high performance FPGAs with 120 high speed input links
  - Xilinx Virtex UltraScale / Altera Stratix 10
  - Each FPGA will handle around 1 Tbps
- Implementation of the L0 buffer
- Processing algorithms
  - Energy and time reconstruction
- Interfaces to L1Global trigger system and to FELIX system
- R&D ongoing
  - Fully functioning prototypes are scheduled by 2017



Digital filtering studies – Phase II

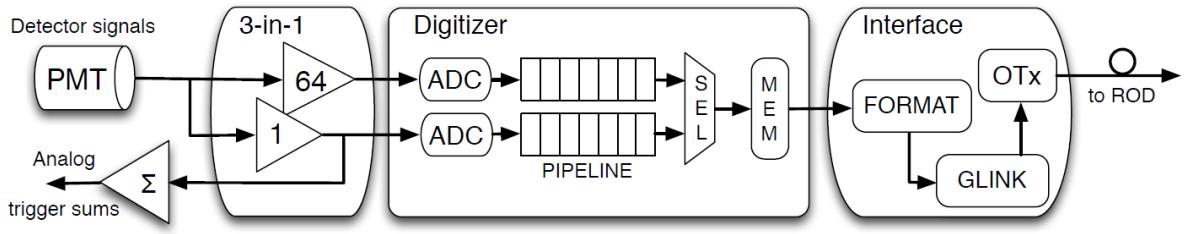
- Digital filtering choice are being studied
  - Sampling frequency of Super-Cells at 40MHz/80 MHz
- Potential pile-up filtering algorithm: **Extended Linear Optimal Filtering**
  - Optimizes the noise on the energy measurement in extreme pile-up conditions
  - Sequence detection algorithm
    - Uses 10 samples at 80 MHz(5 BC)
  - Showing promissing results
    - Good linearity and resolution
    - Implementation in FPGAs is complex but possible



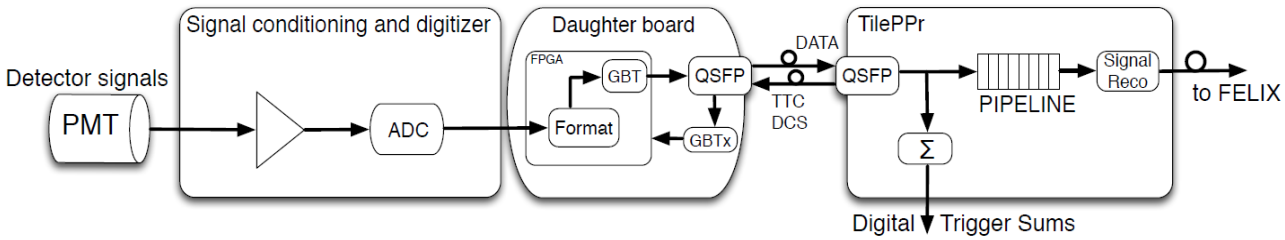
Tile back-end upgrades

Tile Calorimeter Phase II

Current front-end electronics



Upgraded front-end *Upgraded back-end*

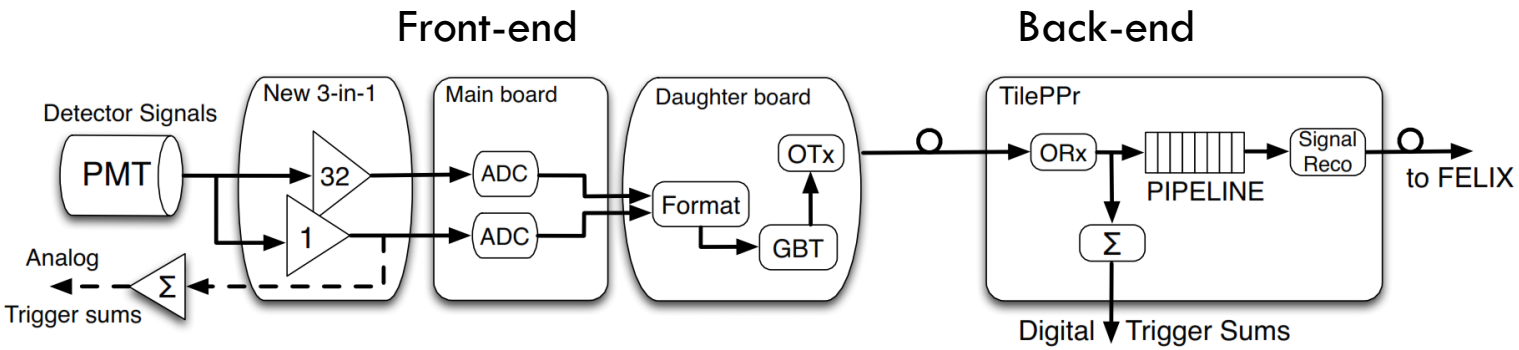


	Present	Phase II
Total BW	~205 Gbps	~40 Tbps
N. Fibers	256	4096
BW/module	800 Mbps	320 Gbps
Nb. boards	32	32
Nb. crates	4 (VME)	4 (ATCA)
In BW/board	6.4 Gbps	1.25 Tbps
Out BW / $board_{DAQ}$	2.56 Gbps	40 Gbps
Out BW / $board_{L1/L0}$	Analog	500 Gbps

- Complete replacement of the back-end electronics during the LS3
  - New readout strategy to provide digital trigger information at low latency for L0/L1
  - Pipelines, derandomizers buffers, DCS and TTC interface moved to the back-end electronics

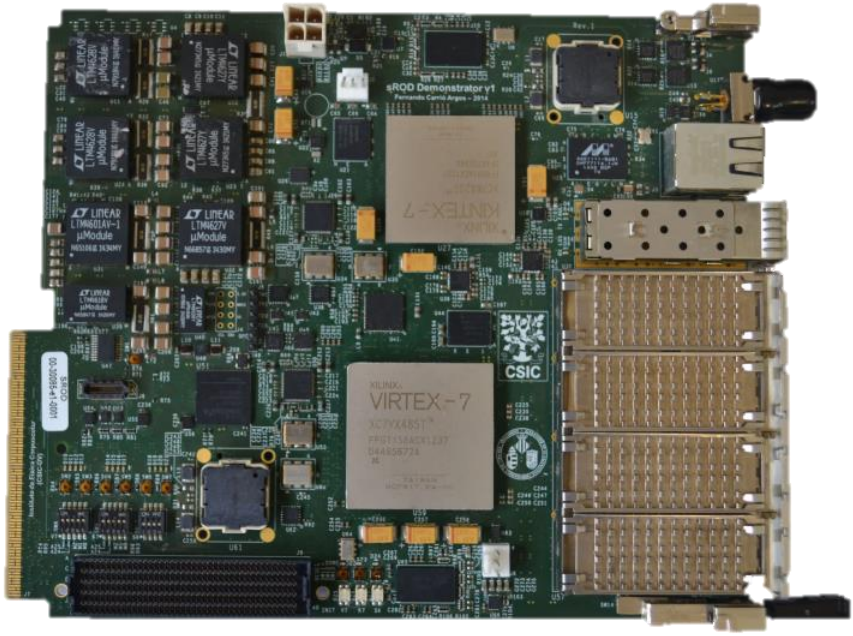
Demonstrator project and plans

- Evaluation the new readout schema and trigger system interfaces
  - TileCal demonstrator module is operative in our lab at CERN
- Plans for the demonstrator project
  - Test beam 2015 (7th October – 21th October) and 2016 (June and September)
  - Possible insertion of one demonstrator module into the ATLAS at the end of 2016
  - Insertion of more modules during LS2 depending of the demonstrator results and performance
- Readout architecture for Phase II but keeping backward compatibility with the current system
  - Tile Pre-Processor will interface the current TTC system (or FELIX) with the new front-end electronics
  - Back-end electronics will send Level 1 selected events to the current RODs
  - Provide analog trigger signals to the present L1Calo system

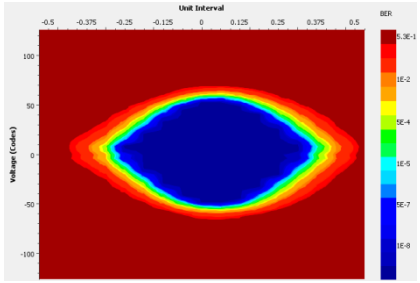


TilePPr prototype - Demonstrator

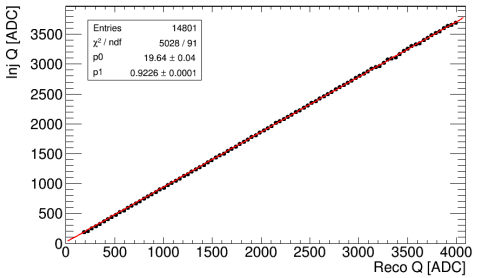
- Represents 1/8 of the final TilePPr module for Phase II
- Double mid-size AMC form factor
  - ATCA carrier / µTCA
- Virtex 7 + 4 QSFPs (Readout)
  - Readout and operation of 1 complete TileCal module
  - TTC/DCS distribution to the FE
  - Interface with FELIX system
  - Energy and time reconstruction algorithms
- Kintex 7 + Avago MiniPOD TX (Trigger)
  - Evaluation of the interfaces with L0/L1Calo and latencies between systems
  - Trigger data preprocessing algorithms
- DDR3 memories, FMC, GbE ports, PCIe, ...
- System has been succesfully tested
  - BERT showed no errors during 115 hours
  - $5 \cdot 10^{-17}$ for a confidence level of 95%
  - 16 links at 9.6 Gbps with PRBS31 pattern



TilePPr prototype



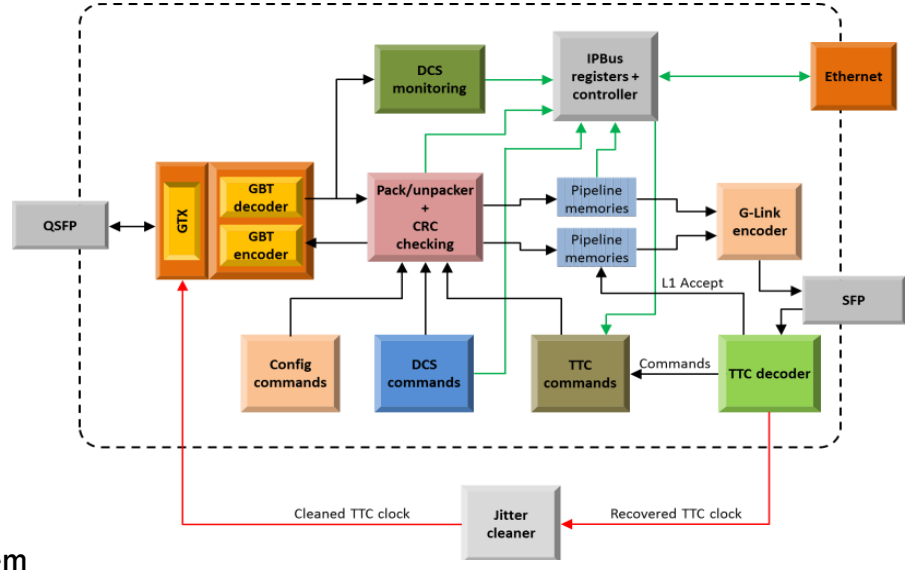
Eye diagram at 9.6 Gbps (GTX)

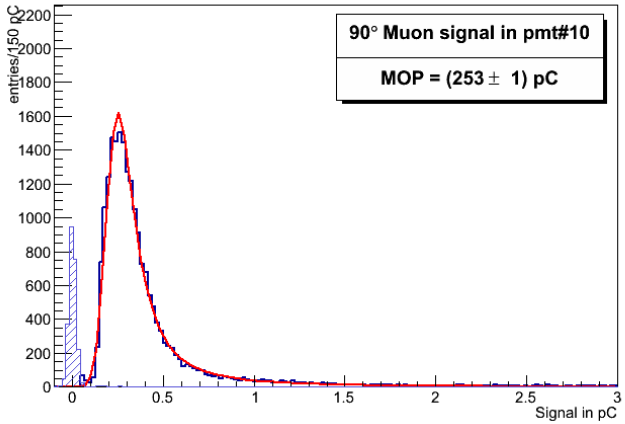


Charge injection linearity test

TilePPr Firmware - Demonstrator

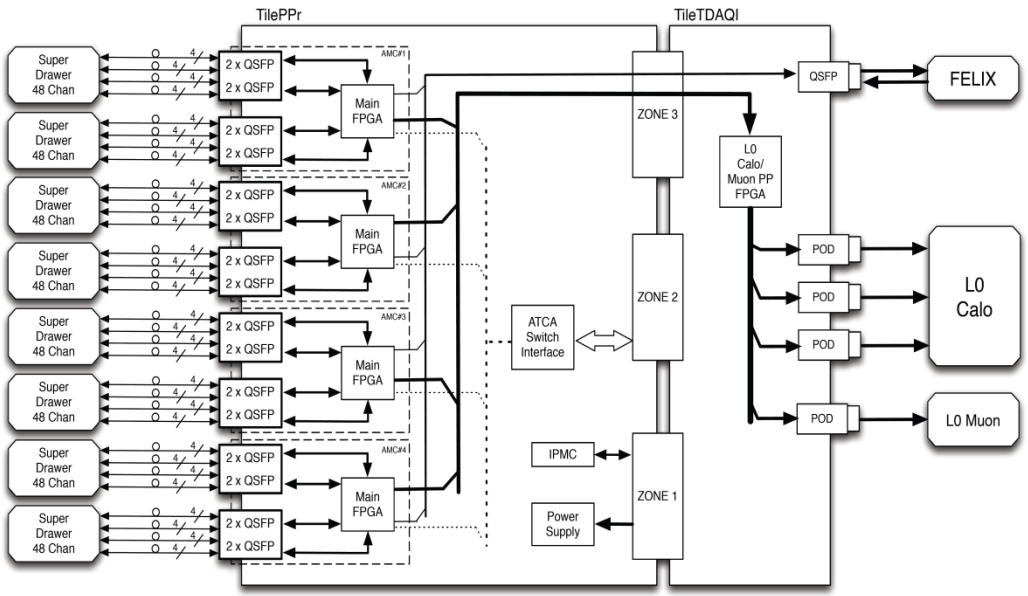
- Developed in parallel of hardware
  - Xilinx VC707 evaluation board
  - 2 x QSFP FMC boards (4 QSFPs)
- 16 asymmetric GBT links
  - 9.6 Gbps for the uplink: readout path
  - 4.8 Gbps for the downlink: TTC / DCS
- Pipelines memories (up to 12.5 µs)
  - Samples with 2 gains x 48 channels → 1 TileCal module
- TTC decoding + G-Link encoder
  - Receive L1A, commands from the legacy TTC system
  - Sent event data to the current RODs after a L1A
- No energy and time reconstruction algorithms in the TilePPr at this moment
  - Performed by current RODs
- IPbus protocol for control and readout with GbE
  - Moving to PCIe or FELIX system for readout
- Firmware validated during last October at test beam





Muon energy distribution (Test beam)

Tile Pre-Processor – Phase II upgrade



- Final design based on the experience with the TilePPr demonstrator
- 32 TilePPr boards in ATCA format
  - ATCA carrier + 4 AMCs
  - Xilinx Kintex UltraScale
  - Implementation of L0 buffers
  - Real-time energy and time reconstruction algorithms
- 32 TileTDAQ-I
  - Rear Transition Module (ATCA)
  - Xilinx Kintex UltraScale
  - Preprocessed trigger data
  - Interface with L0Calo, L0Muon and FELIX system
- R&D ongoing
  - Fully functioning prototypes are expected by 2017

Conclusion

- Complete re-design of LAr/Tile back-end electronics for Phase II
  - New trigger and readout strategies with new trigger algorithms
  - No buffers in the front-end electronics → all data readout at LHC frequency
- LAr will install the new LAr Digital Processing System (LDPS) during the Phase I (~2019)
  - Selection of the technologies for LPPR in phase II will be made based on the experience gained
- LAr/Tile back-end electronics R&D for HL-LHC is well established
  - Tile: prototype of the TilePPr is ready and operative
    - A first firmware approach is full developed
    - Possibility of insert one TileCal demonstrator module at the end of 2016
  - LAr: New LPPR will naturally evolve from Phase I LDPS
    - Digital filtering algorithms are being studied to deal with the high pile-up
  - Final prototypes for Phase II are envisaged by 2017 (Technical Design Review)