Front End Electronics Developments for the ATLAS calorimeters at HL-LHC

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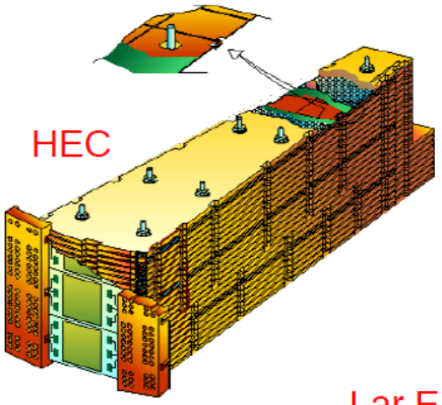
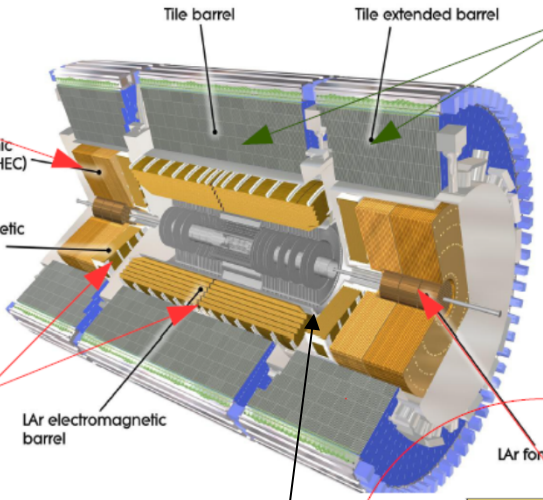
on behalf of the ATLAS collaboration

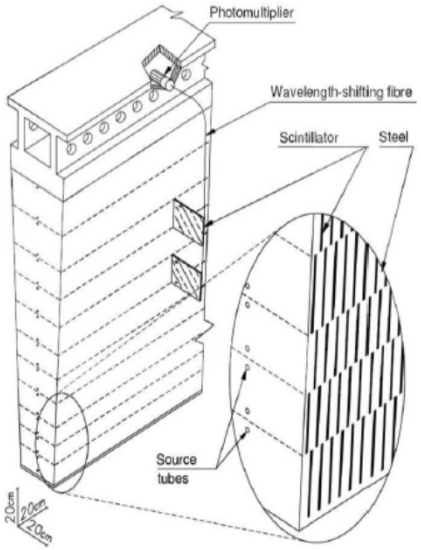
Outline

- ATLAS Calorimeters upgrade for HL-LHC
- New Front End requirements
- Tile Front End developments
- Liquid Argon Front End developments
- Conclusion

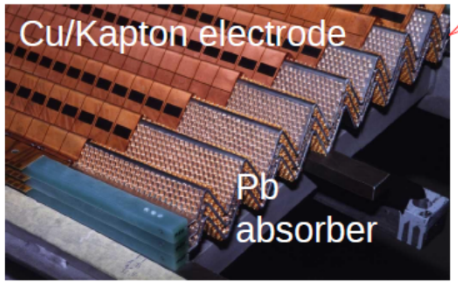
Calorimeters upgrade



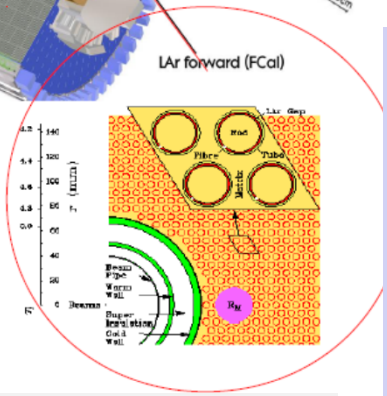




Lar EM



FCAL



LAr EM, LAr HEC and Tile calorimeters not expected to be degraded with high Luminosity
→ Only read-out to upgrade
Today's talk

High Granular Timing Device (Silicon sensors)

FCAL upgrade still under discussion :
-SFCAL with smaller gap/ granularity (decision June 2016)
- Warm MiniFCAL if needed to protect FCAL and improve FCAL performance

Electronics upgrade motivations

Current electronics is still running well but

1- Electronics was conceived for 1000 fb-1* and lower peak luminosity

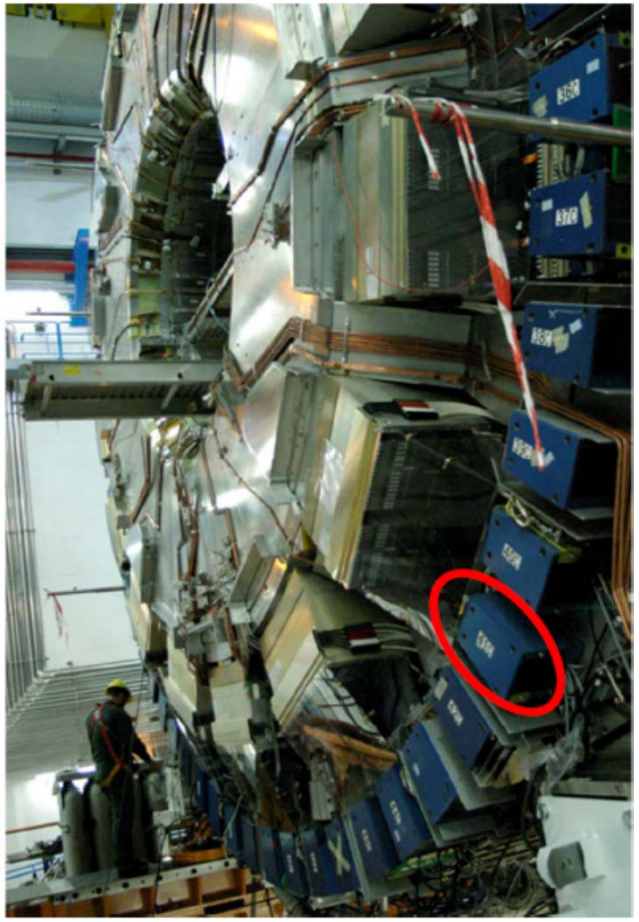
→radiation hardness (<100 kRad in LAr) and trigger latency/rate

HL-LHC 10 μs at L0 /1 MHz

60 μs at L1/400 kHz (now 3 μs/100 kHz)

Trigger granularity increased at L1 in phase I but goal is full granularity for Phase II at trigger level and L0

2- Ageing and/or obsolete components and only a few spares (DMILL chips for instance)

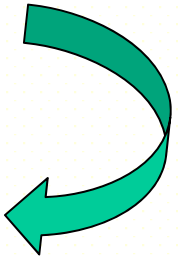


** HEC GaAs cold preamps tests show they can accept 3000 fb-1*

Still R&D and quite some questions opened

Technology (/radiation tolerance)
- COTS (Tile)
- CMOS (130 & 65 nm)
- SiGe bipolar (180 nm)

Integration :
Full Electronics System On Chips (FESOC) or different ASICs



Dynamic range/max current
Number of gains (continuity)
7-12-14 bits ADC

High Luminosity optimisation :
- Analog shaping & vs more digital filtering
  → 40 / 80 MHz

Synergy with other developments
Schedule and cost…..

HL-LHC Front End requirements : LAr/Tile

1. Maintain similar performance as current readout with optimisation for high pileup and same power consumption

   as pile-up dominated, might relax a bit electronics noise in some layers,

   e.g Lar EM ~100-150 nA (30 MeV) @ Cd=1 nF (10 mA &150 mW/channel)

   Tiles : 12 fC noise and few nC signal max

2. Should measure correctly highest energy rare events

   Retune dynamic ranges in some regions

   e.g EM calorimeter strip from 1mA to 2 mA in Endcap (in 1996 ID services X_0 not well defined…)

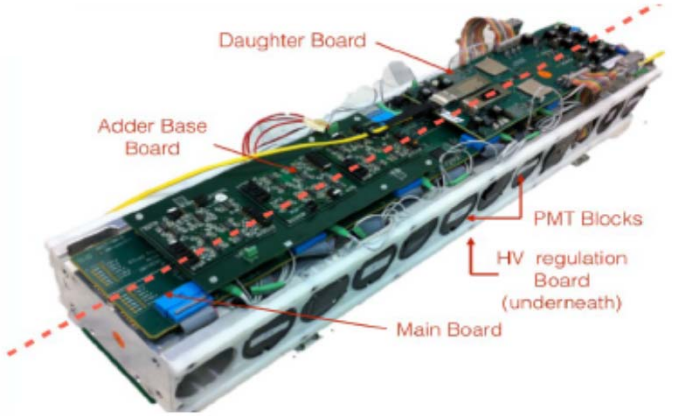
3. Shaping and digitization (40 MHz or above) need still be optimized (similar global architecture for Lar and Tile but less demanding conditions in Tile)

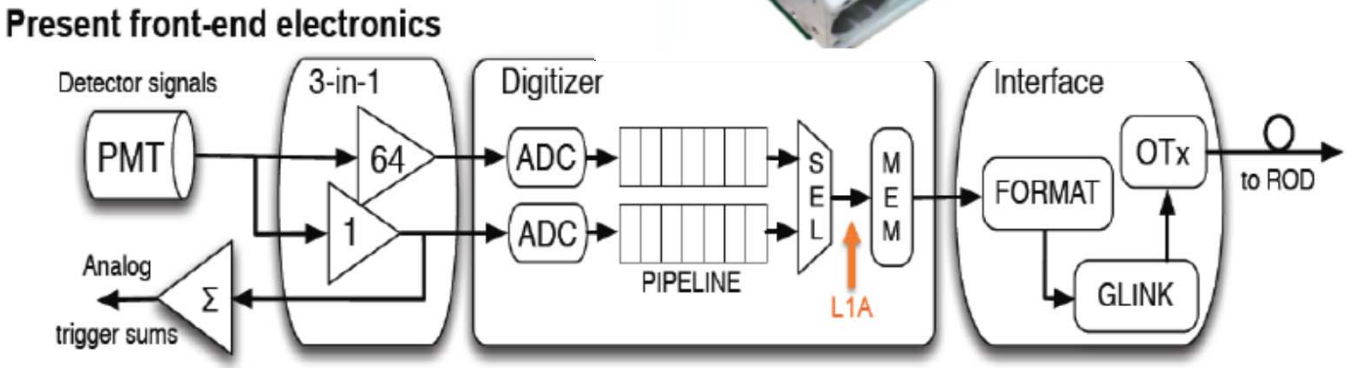
4. Ship full granularity channel data at 40 MHz from Front End to Back End

TILE FRONT END DEVELOPMENTS

Tile Front End developments

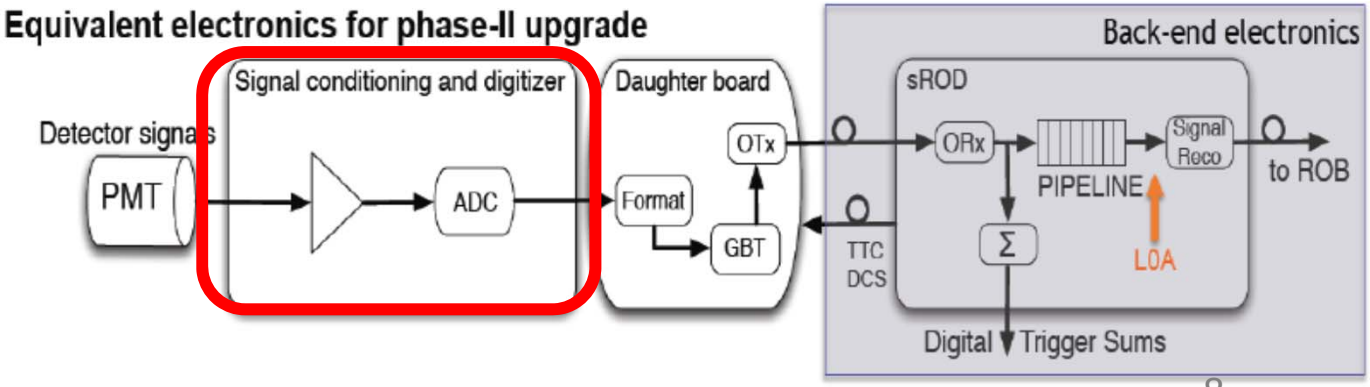
New drawers : 1) simplify, reduce maintenance needs (redundancy in power supply,
4 independent mini-drawers/module (12 PM) instead of one now (48 PM),
2) Improved radiation tolerance & performance





3 options for FE :

- 3 in 1 improved board
- QIE ASIC
- FATALIC ASIC

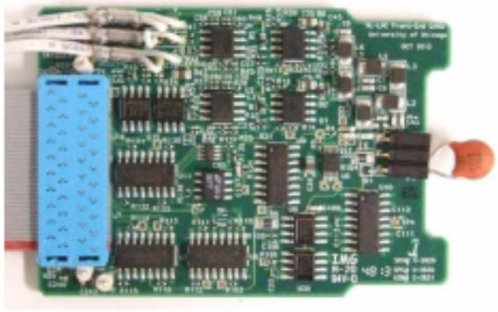


Might have better noise with ASIC, but more ranges needed to achieve dynamics

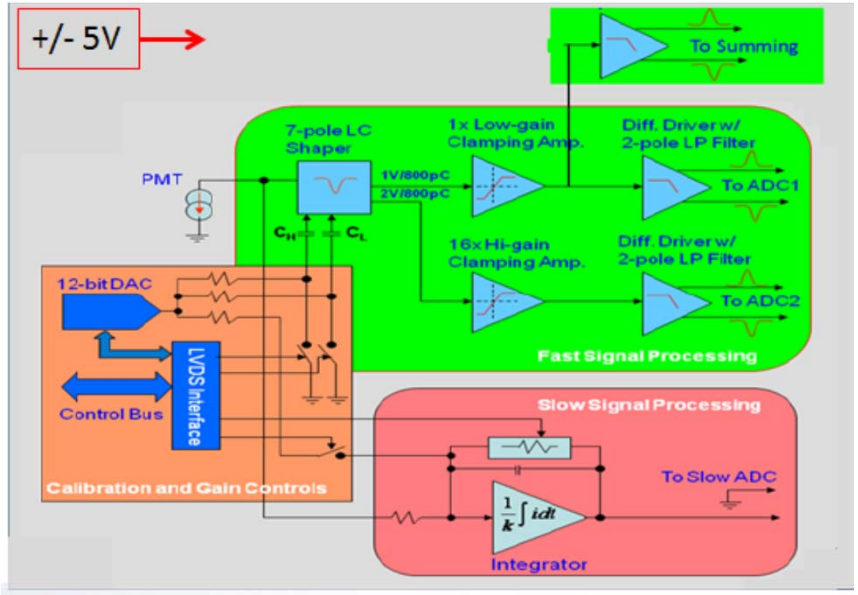
3 in 1 improved Tile FEB (University of Chicago)

Improved version of current 3 in 1 FEB
Using discrete component with :

- better linearity (/10)
- better radiation tolerance
- +/- 5V power supply



7-pole passive shaper
High and Low gain output (32/1) to achieve 16-17 bits dynamics
Charge injection + integrator to read Cs data
Signal digitized on main board with commercial ADC (12 bits 40 MHz) transferred serially to daughter board at 600 MHz
Expected performance well known



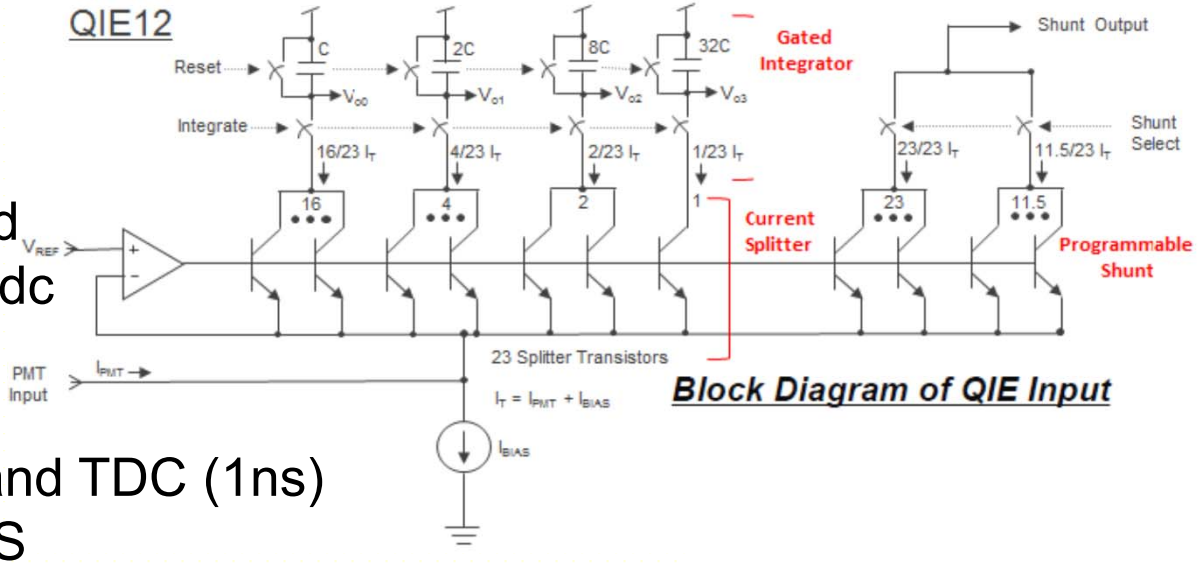
QIE ASIC : charge integrator and encode
Argonne National Laboratory

Current splitter with gated integrator

- No pulse shaping
- Pseudo log response

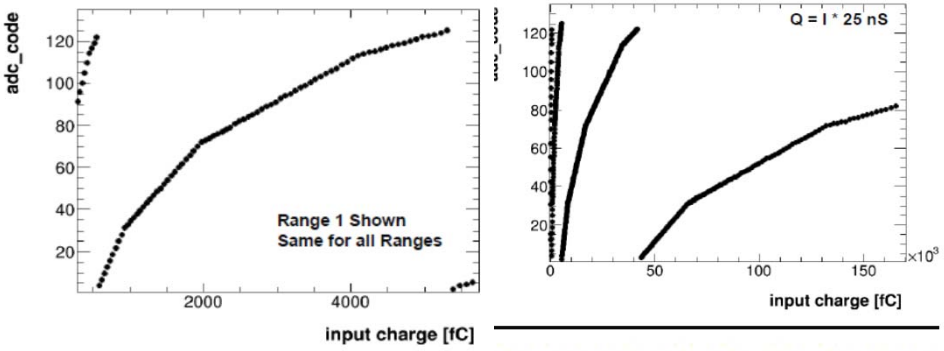
- 18 bits dynamics achieved with 4 gain and 7-bits flash adc
- lsb at 1.5-3 fC
- power 360 mW/ch
- Internal charge injection and TDC (1ns)
- SiGe process from MOSIS

Overview of the QIE12

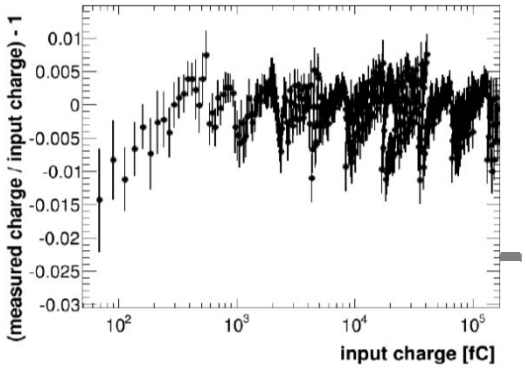


Block Diagram of QIE Input

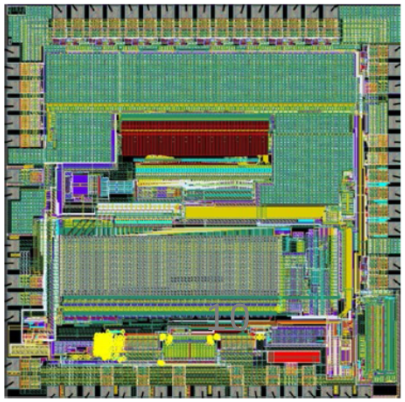
ADC Transfer Function



Linearity Residuals

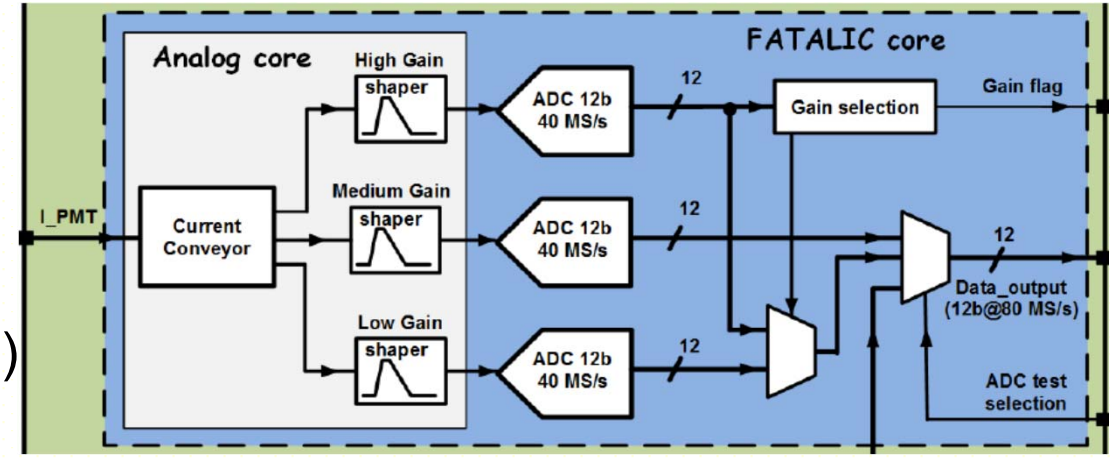


QIE12 Chip layout



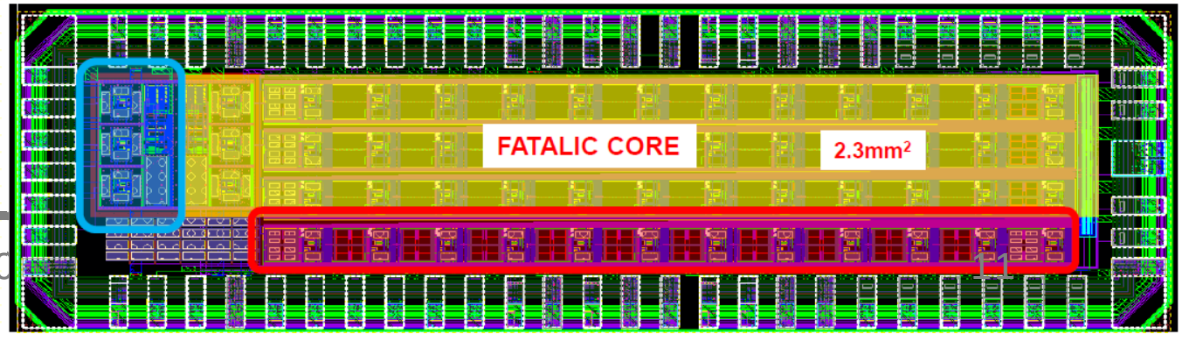
FATALIC ASIC
LPC Clermont Ferrand

16 bits dynamics range achieved with 3 ranges
- PMT signal read by current conveyor and duplicated in 3 outputs
- RC unipolar shaping (tp=22ns)



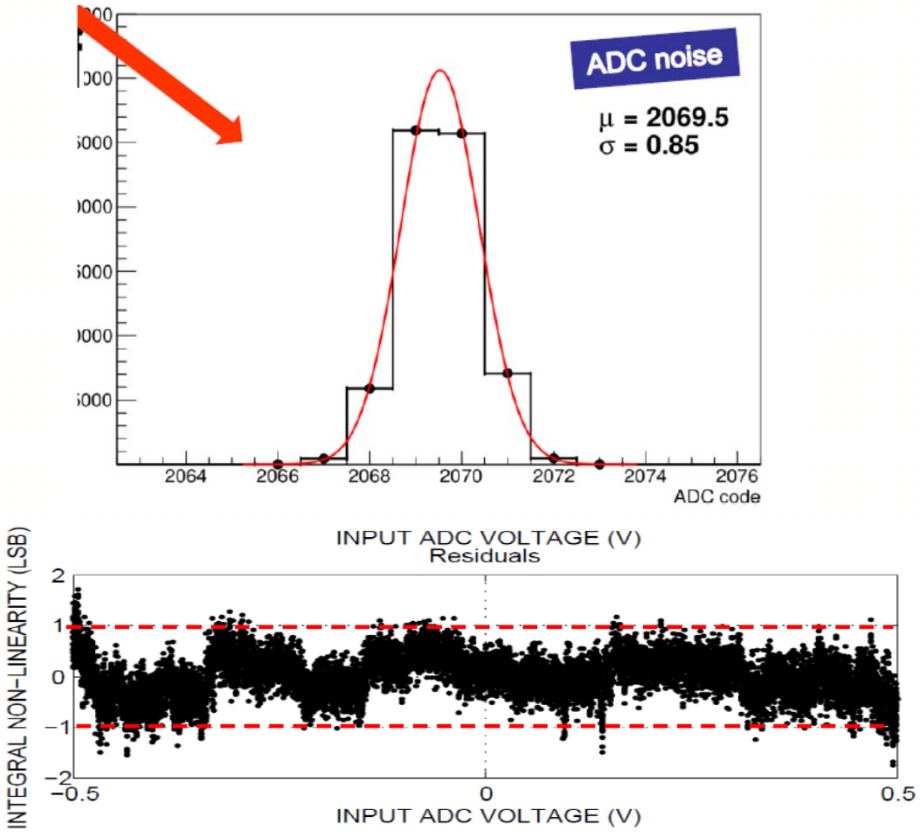
- one 12 bits 40 MS/s ADC per channel (1.5 bit/stage pipeline ADC architecture)
- Gain selection to transmit Medium + (High or Low)
- 80 Mb/s output data multiplexing
- 205 mW/channel with 1.6 V single power

IBM CMOS130 nm technology



FATALIC ASIC : a few performance

ADC alone

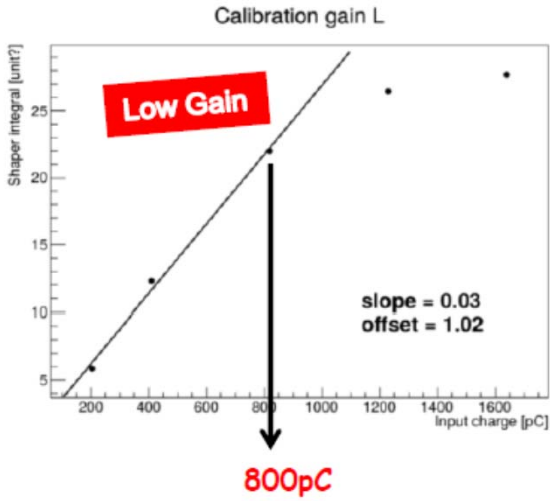


→ **11 bits precision ADC**

Complete channel

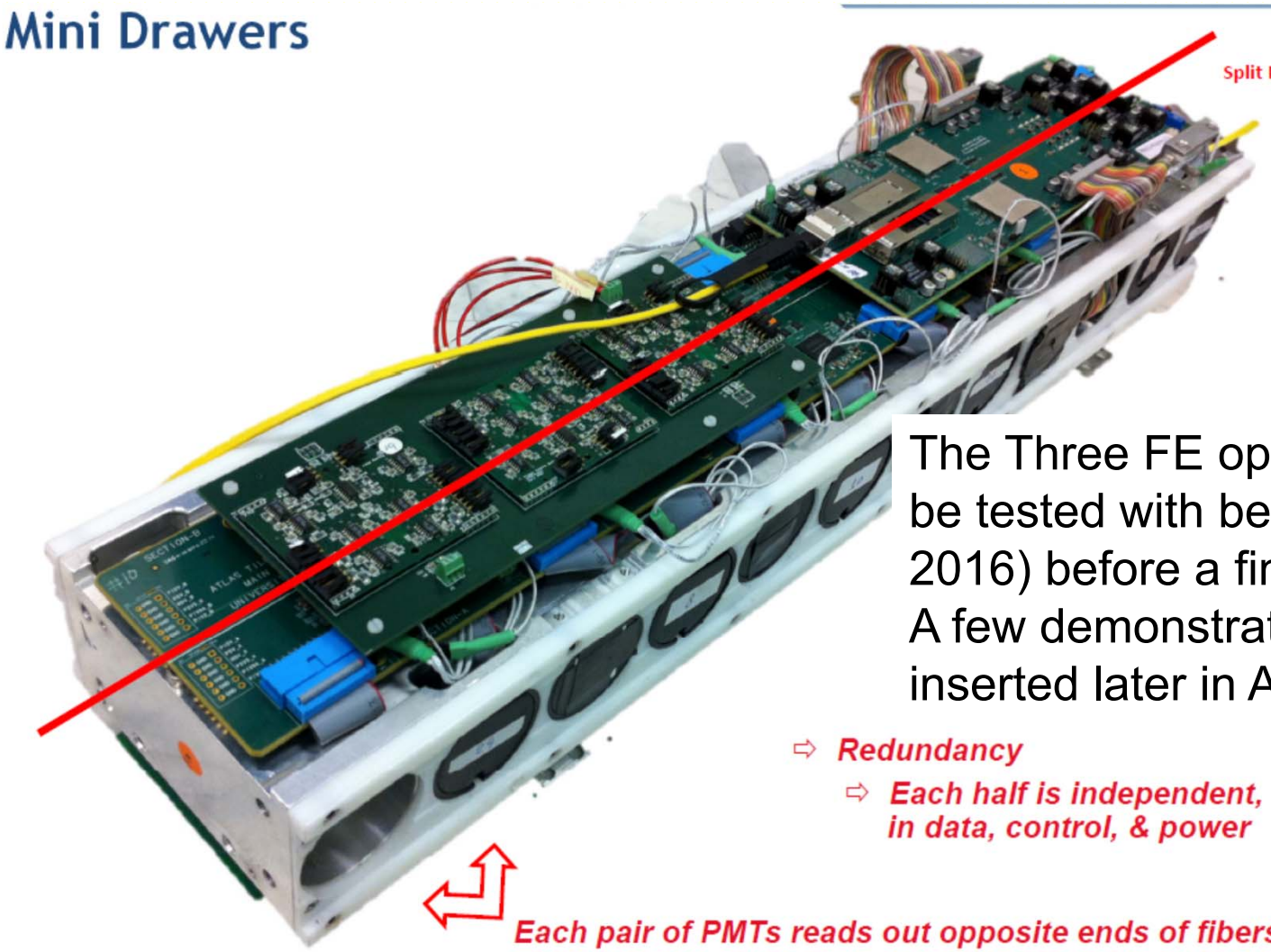
3 lsb (10 fc) rms noise in High gain

Linearity ok in high/medium range
Limited dynamic range in low gain
(800 instead of 1200fC)



Parasitic resistor on a power rail
→ Corrected in FATALIC4b used in beam test

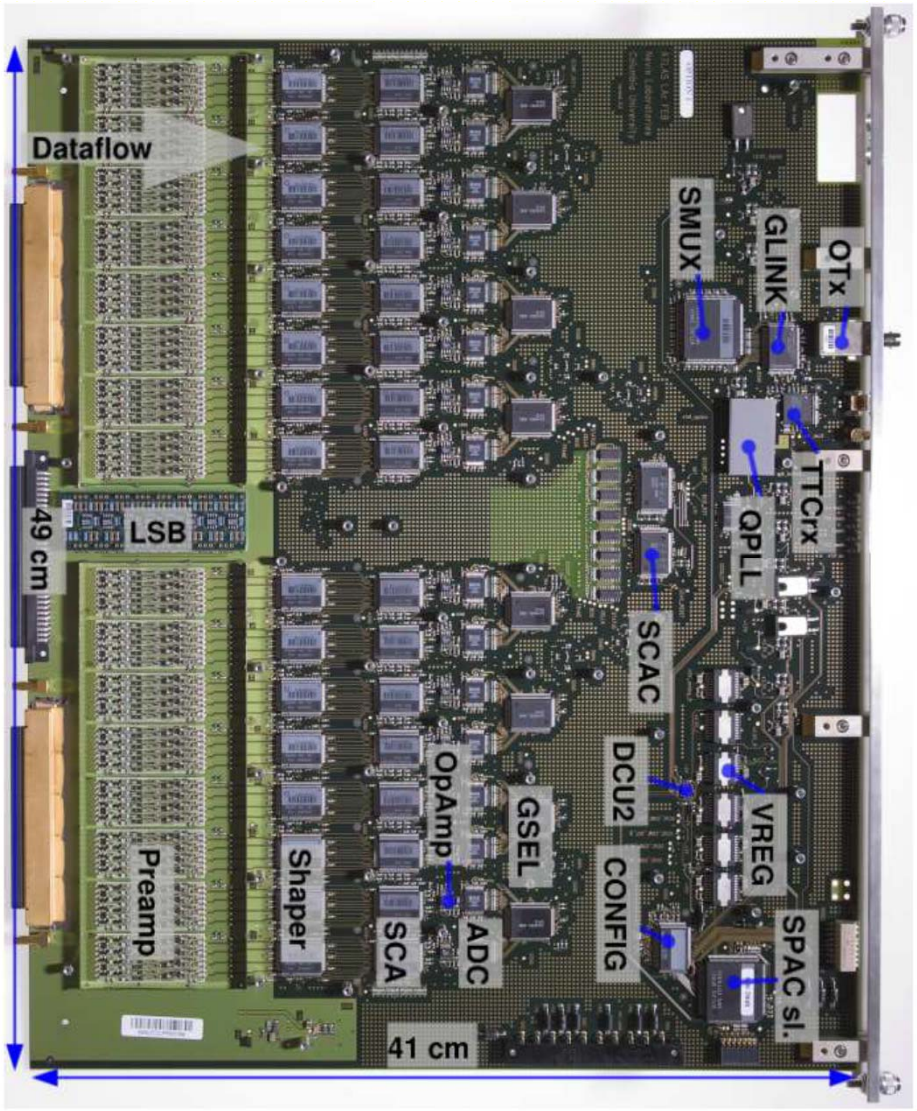
First complete mini drawer prototype



The Three FE options expected to be tested with beam (end 2015 and 2016) before a final choice
A few demonstrators will also be inserted later in ATLAS

LIQUID ARGON
FRONT END DEVELOPMENTS

Current read-out : LAr calorimeters



128 channels FE boards with :

- Mezzanine boards with "0T" preamplifiers using smc discrete components for EM/FCAL (1/5-10 mA dynamic 50/25 Ω)
- CR-RC^2 shaper (τ=13 ns) with 3 gains output 0.8/8/80 + trigger
- Analog storage in DMILL SCA
- 12 bits 5MHz ADC + gain selection
- serializer + GLINK/OTx

128 channels calibration boards with large current OPAMP/DAC and digital chip in DMILL technology

~~+ Controller board~~

Front End requirements : LAr specific

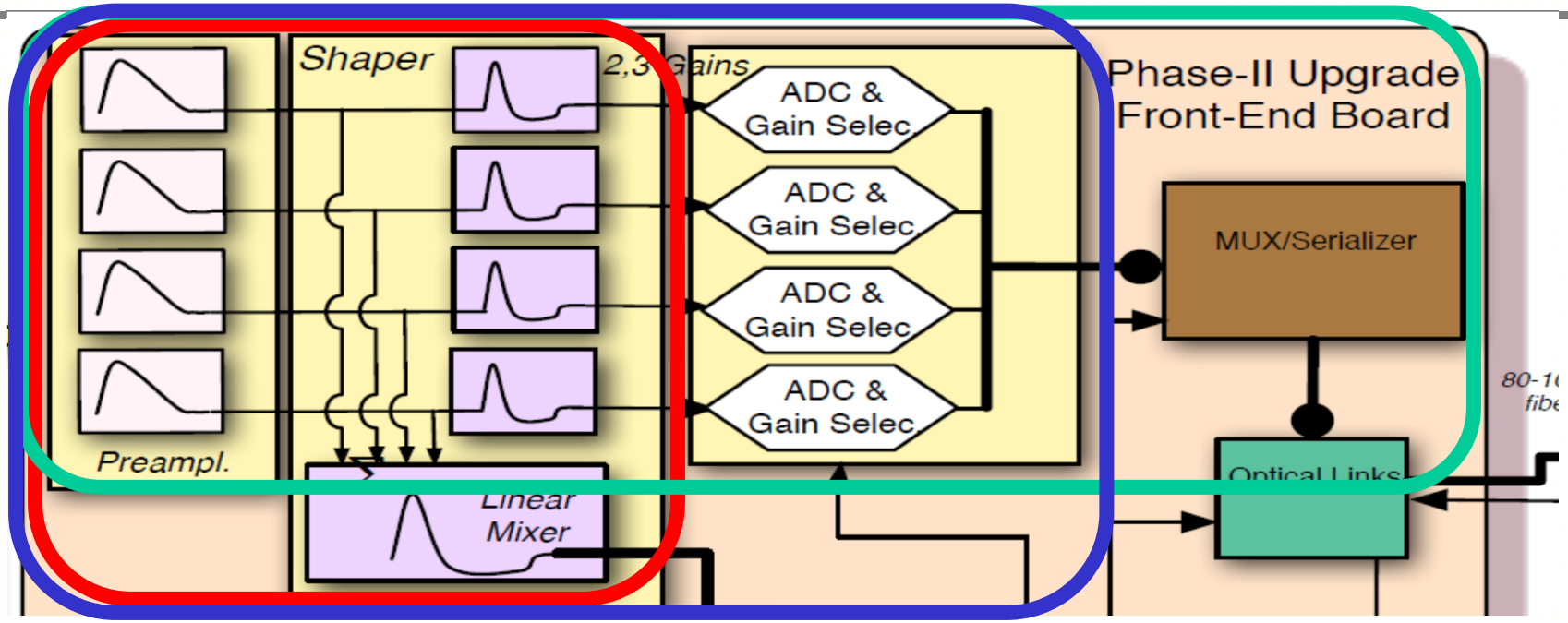
1- Investigate 2 gains system instead of 3 with all precision physics in high gain (per mille integral non linearity)
current high/medium gain selection on e/γ at pt between Z→e+e- and H→$\gamma\gamma$…
→ *Constraint on adc : need at least 12 bit ENOB or better*

2- "Unique" preamplifier type for EM : selectable dynamic range and cable matched input impedance (25/50 Ohm)

3- Tuneable shaper time constant (shape also?), and impedance (to minimize signal reflection)

4- Preshaper instead of preamplifier for HEC
("unique" LAr chip ?)

LARG Front End Evolution



Needed : preampli + shaper asic

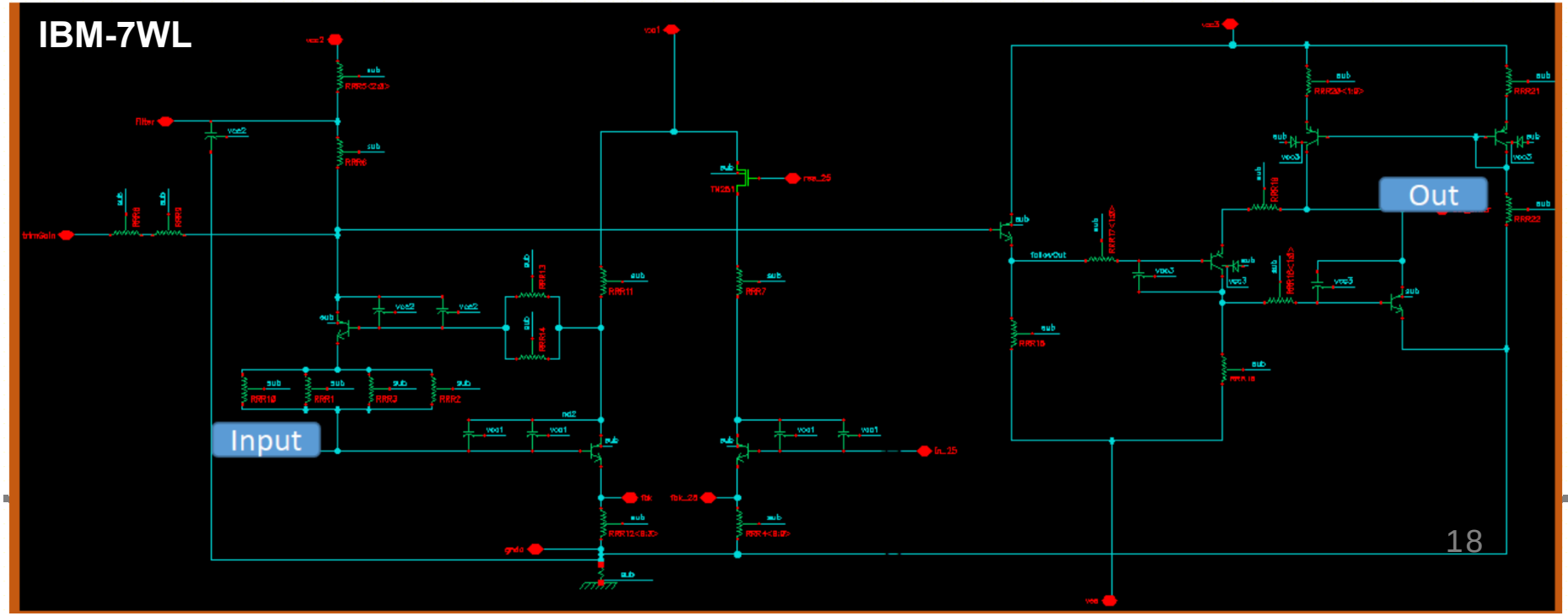
Desirable : integrate the ADC (no gain selection if possible and transfer two gains information 16/32 fibres/FEB)

Best : integrate also the serializer → FESOC

SiGe (180 nm) bipolar option (University of Pennsylvania)

Similar to current Phase 0 preamp design (done with discrete components)
Bonding option for 25/50 Ω. No impedance/dynamic range tuning
Might be marginal at High frequency (> 30 MHz) and large current (10 mA)
Good noise performance on simulation
25 Ω preamp : 97 nA for 1.0 nF with CR-RC2 shaping (power dissipation 47 mW preamp alone and ~90-100 mW with shaper)

Layout is existing but no submission date known… mainly funding issue



New preamp design in 130 nm CMOS (Omega+LAL)

Current 0T with discrete components (2.4 Ω, 1 μF) difficult to integrate in ASIC
→ New line terminating preamp with dual range output and electronically cooled resistor

Impedance :

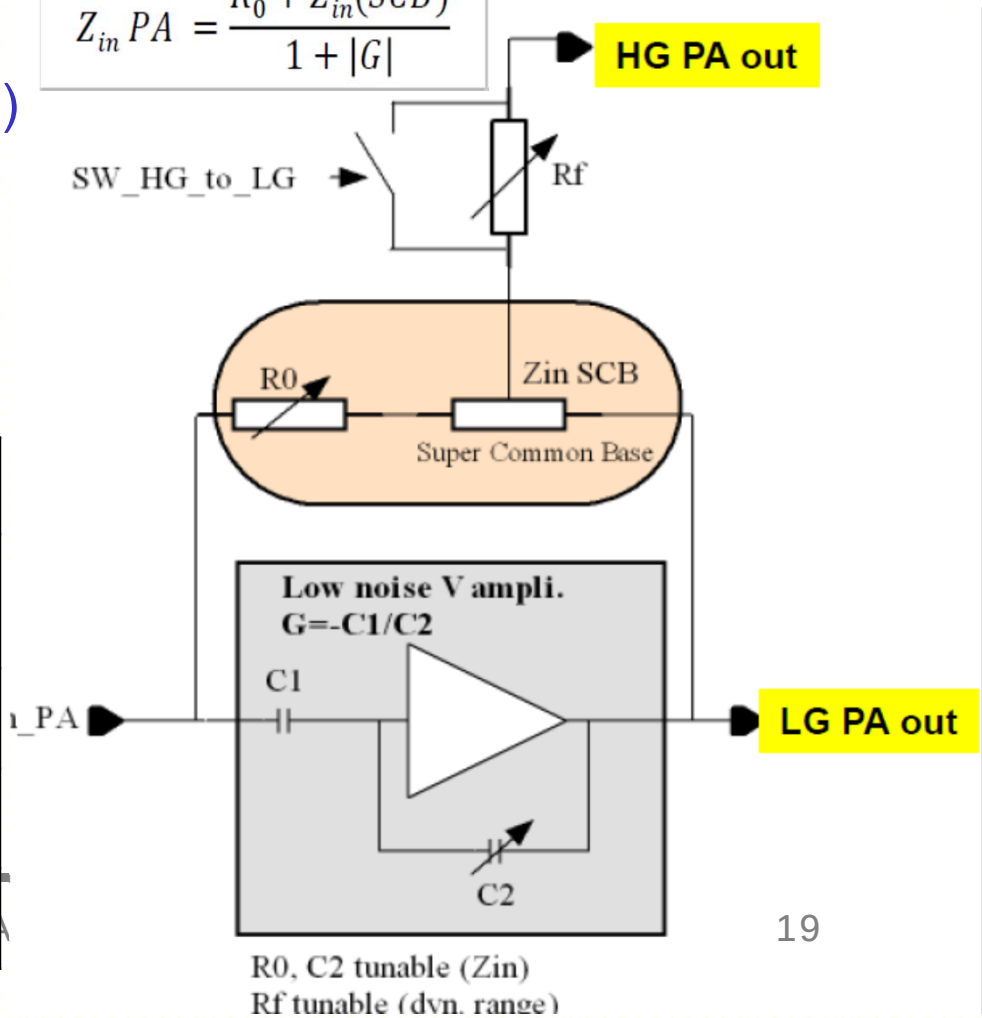
Super common base amplifier (low Zin)

Low noise voltage sensitive amplifier

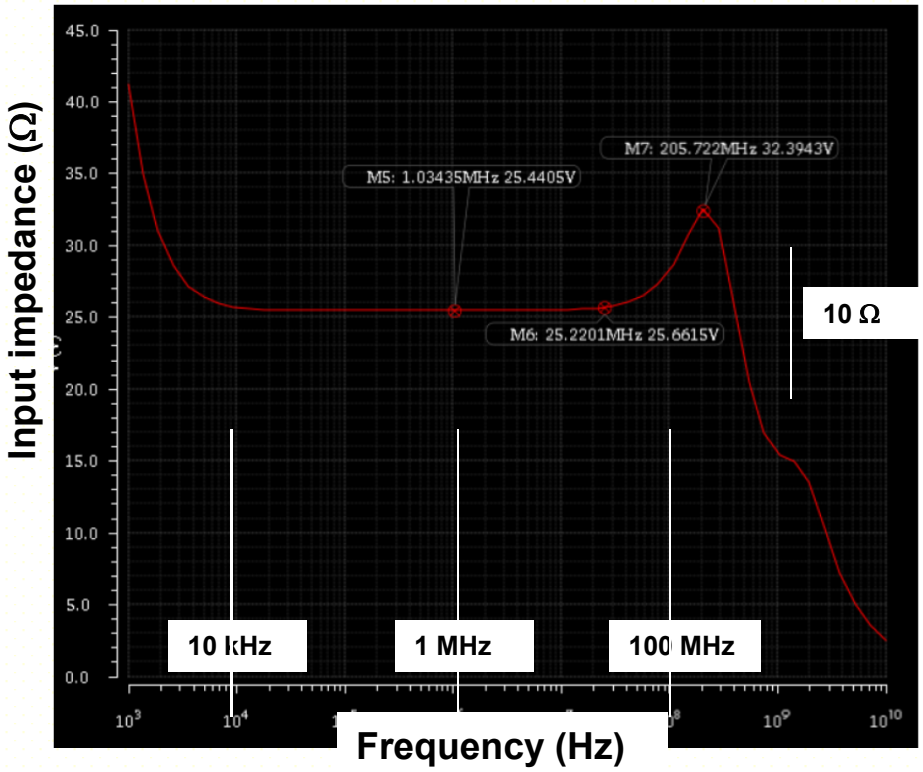
$$Z_{in}\,PA = \frac{R_0 + Z_{in}(SCB)}{1 + |G|}$$

Noise $\frac{4kTR_0}{(1+G)^2} \sim \frac{4kT\,Zin(PA)^2}{R0}$

	50 Ω	25 Ω
R_0	500 Ω → 2 mA	100 Ω →10 mA
G	C1/C2=9	C1/C2=3
R-Noise eq	5 Ω	6Ω
Dynamic	Rf=5kΩ	Rf=1kΩ

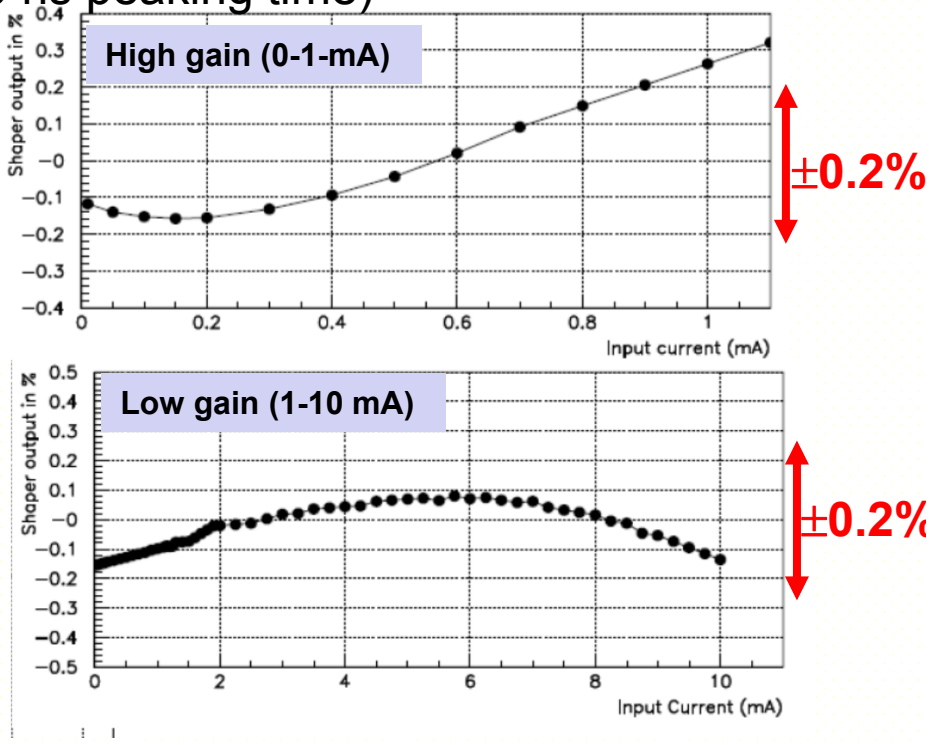


Simulation performance results (25 Ω /10 mA)



Impedance flat from 10 kHz to 100 MHz
< 1 Ω variation versus current due to Super Common base Zin variation

Integral non linearity (/linear fit) with CR-RC2 (40 ns peaking time)



Noise dominated by R0 and NMOS ampli : 150 nA with 1.5 nF
Preamp alone : 15 mW

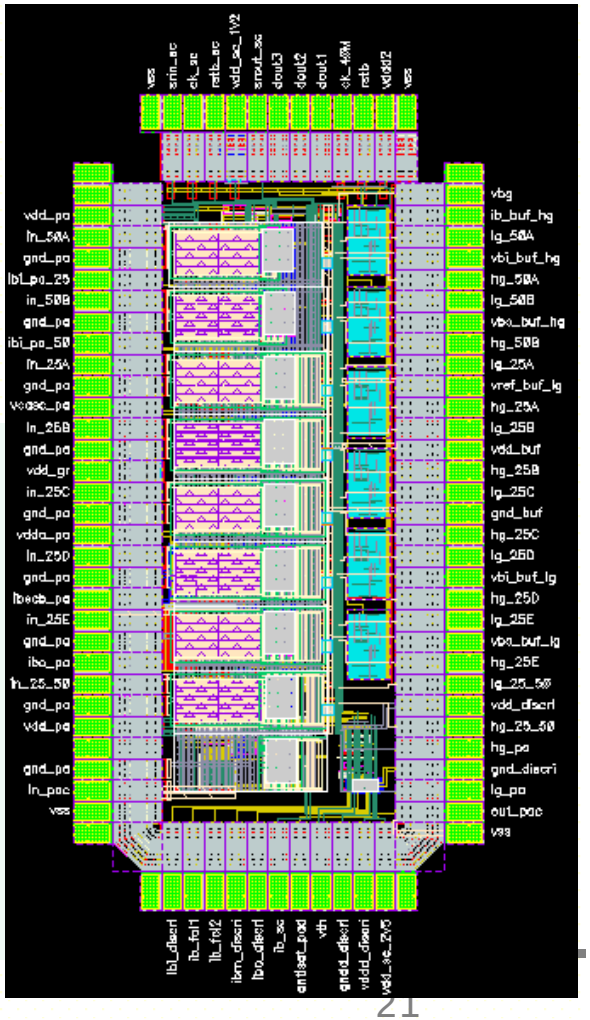
New preamp design in 130 nm CMOS

Layout chip finished. Expected submission on March 15th through CERN/TSMC MPW.. No enough users → End April

8 channels chips with or without tuning options (impedance/gain transition…)

Test various transistor size and capacitor types + protection diodes (against detector HV trip)

(2.5 V I/0 transistor)



BNL/Omega/LAL Collaborative effort :

- Same test boards/benches under development
- Cross measurements of 65/130 nm chips
- Tests under radiation….

→ Goal is to converge toward common CMOS preamp architecture technology by TDR

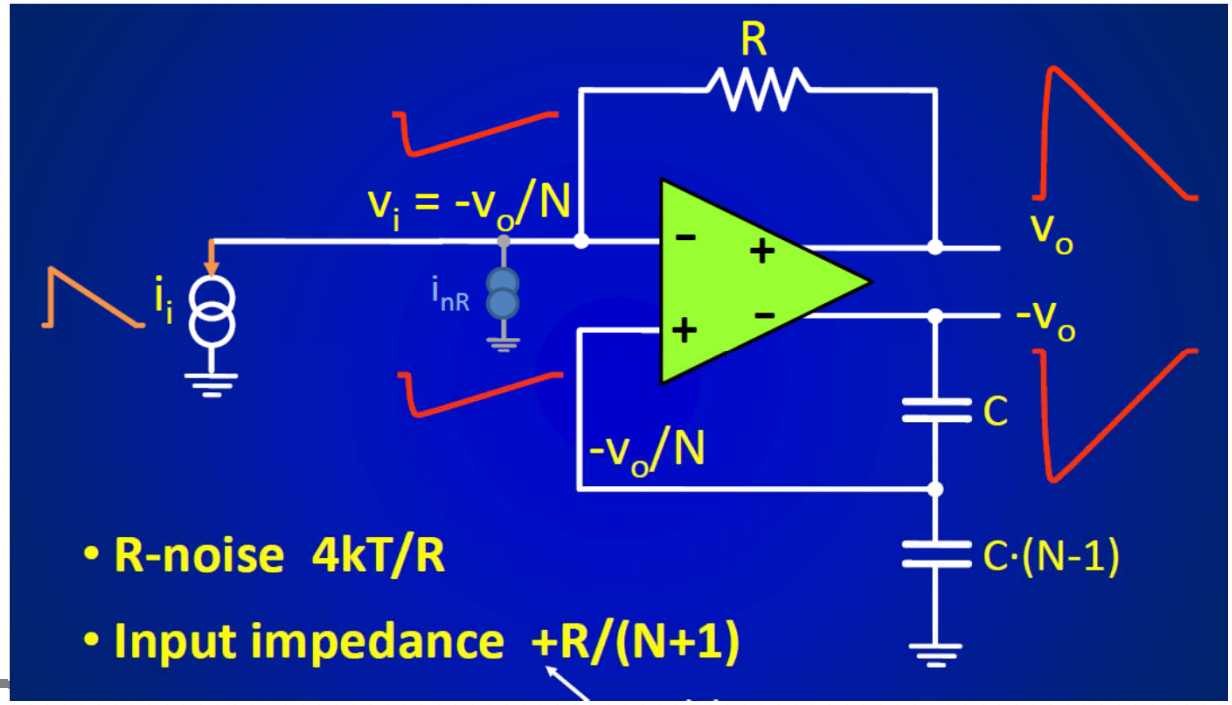
New preamp design in 65 nm CMOS
BNL

Fully differential approach with passive components
Quite similar architecture and functionality /option as 130 nm CMOS chip : dual range, programmable termination and gain, trimmable impedance +/- 3% steps (3 bits)
Simulated in 65 nm CMOS technology with single 1.2 V supply

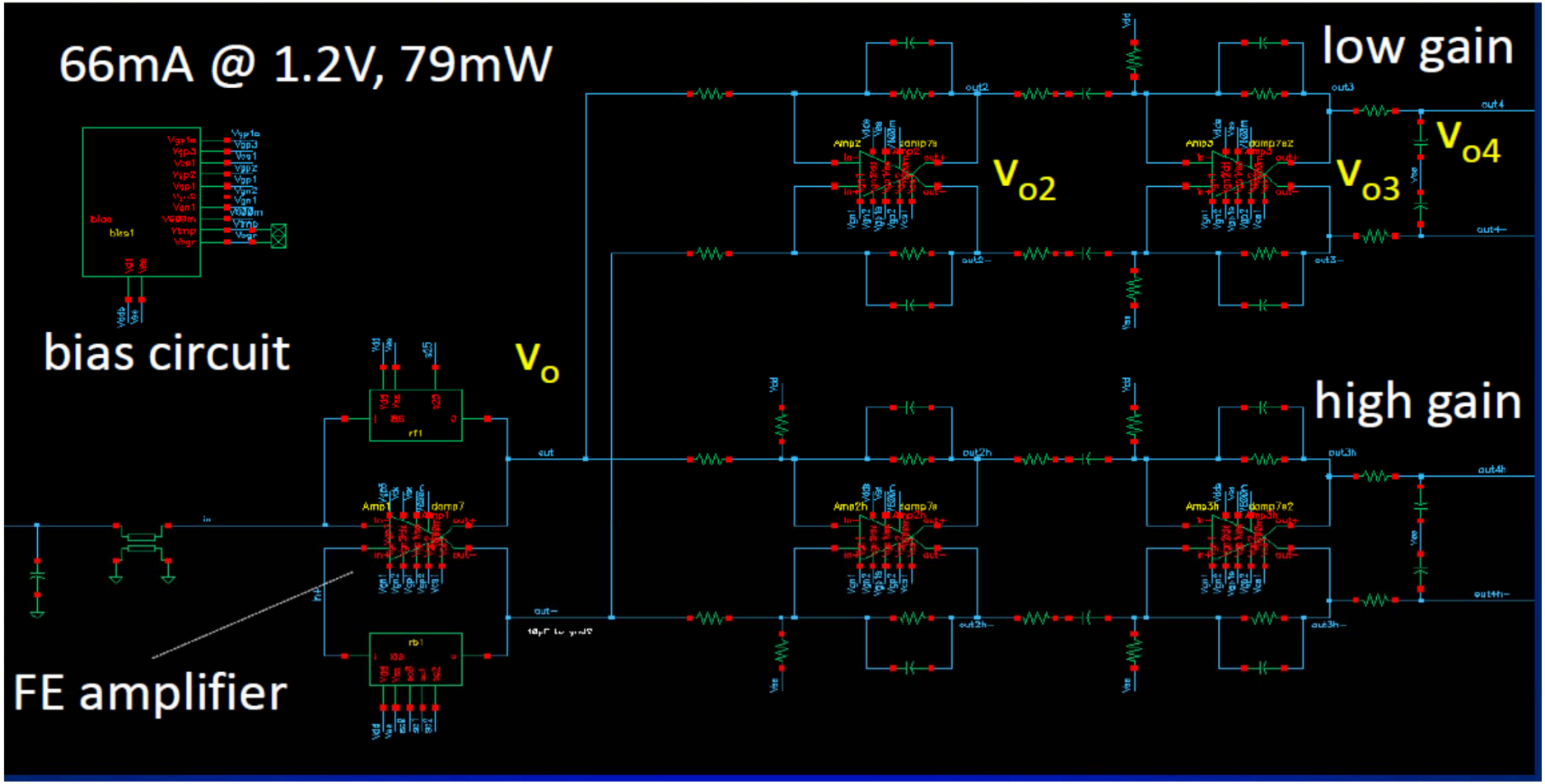
Limitation at high current could be overcome by using larger supply as in 130 nm

Layout to be finalized by June 2016

Expect prototype by Autumn 2016



Full differential read-out schematics



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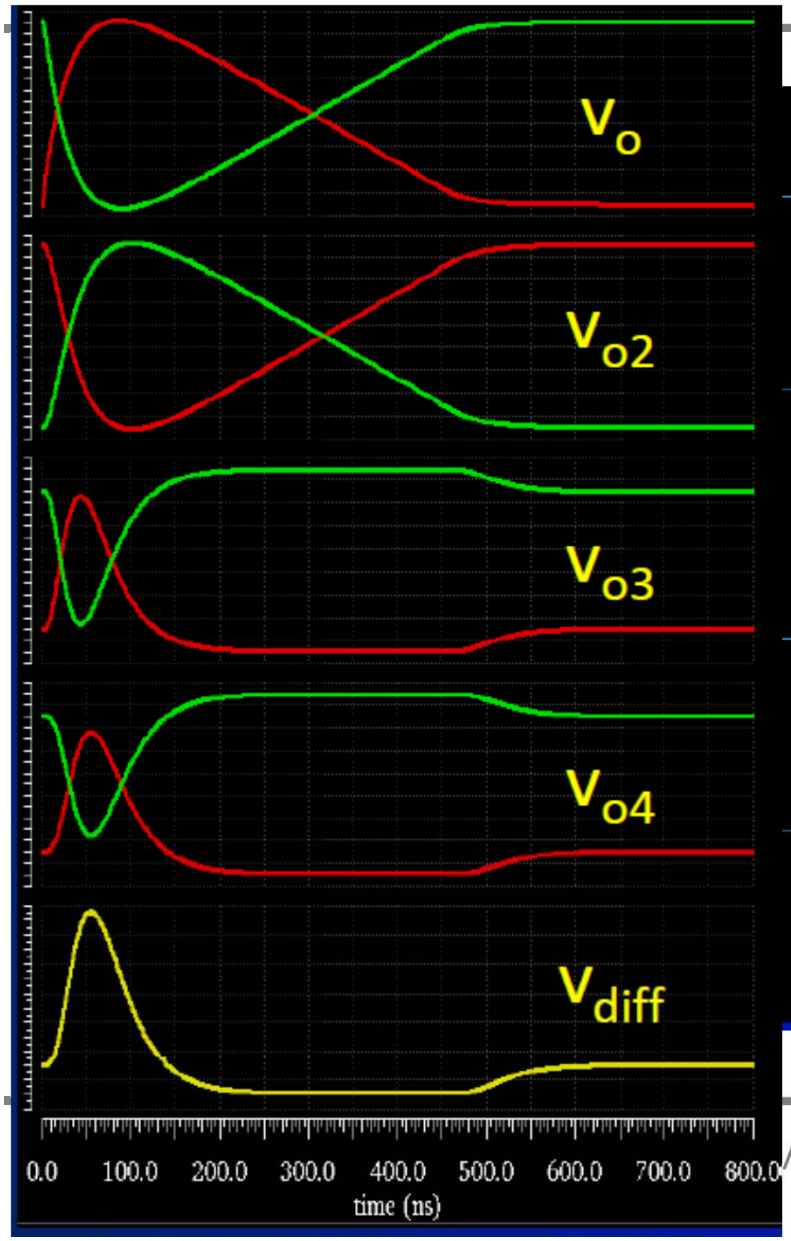
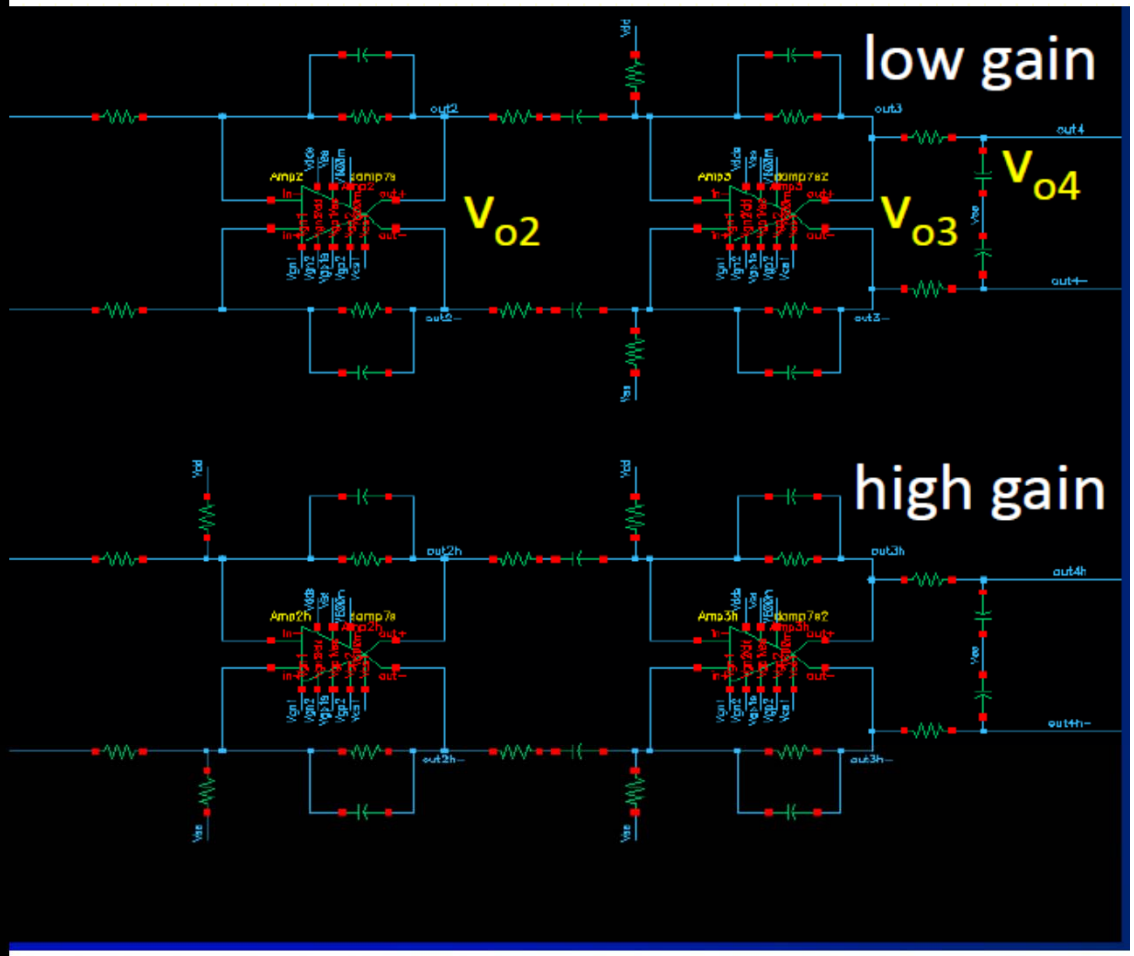
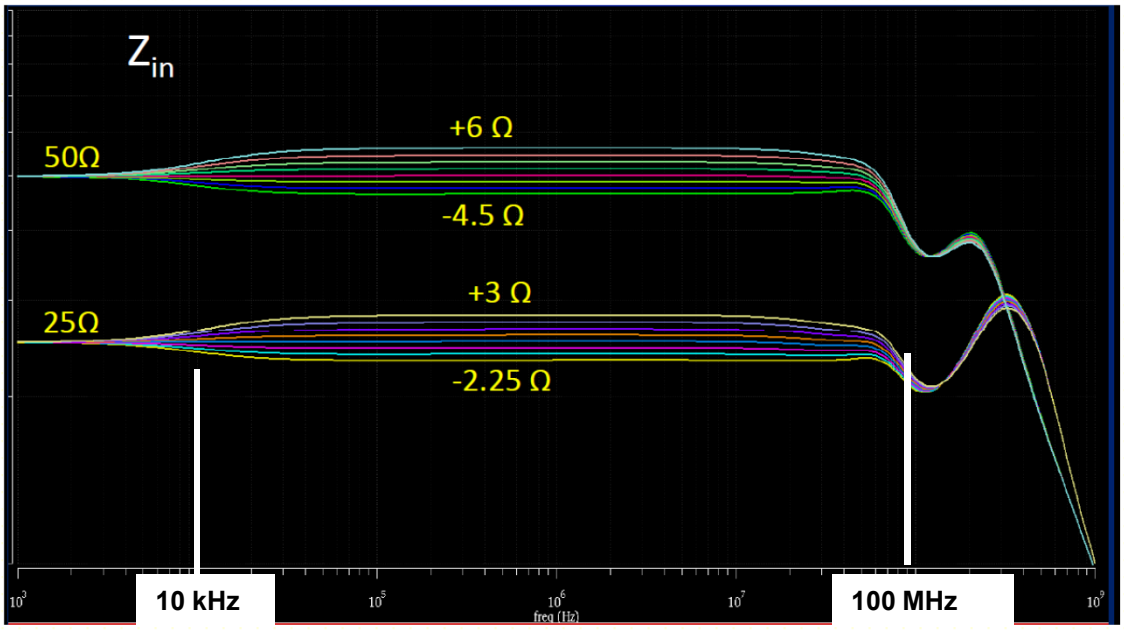
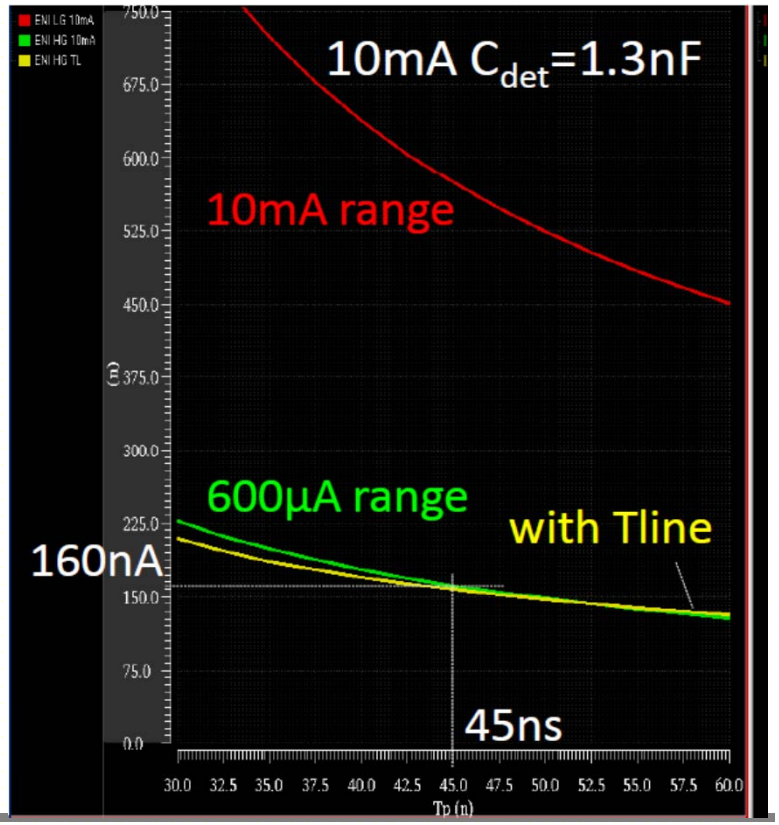


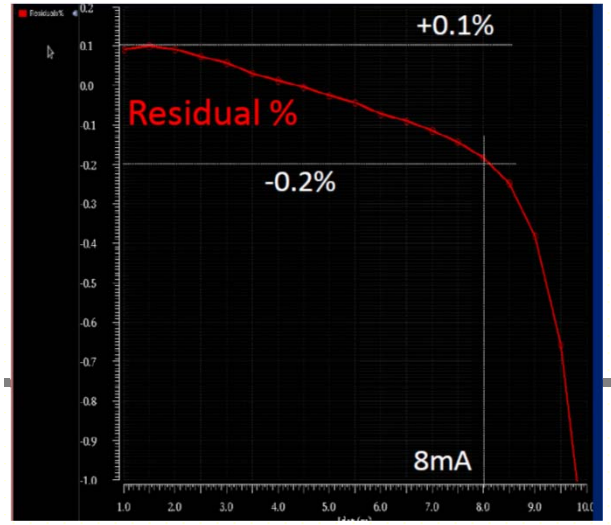


Performance results



160 nA noise for 1.3 nF detector capacitance





Integral non linearity :
+/- 0.2 % at 8 mA
+/- 0.4 % at 9 mA

ADC / serializers / Optical transmitter

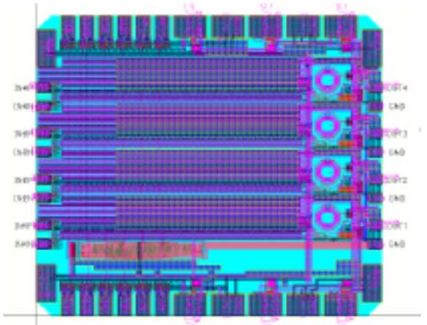
Developments mostly done in the framework of Phase I upgrade for LAr trigger

ADC :

- 40 MHz/12 bits ADC from NEVIS (130 nm CMOS) to be used by Phase I new trigger boards. Final chip expected in spring.
- ADC development by UT Dallas. Goal is 14 bits ADC at 40/80 MHz :
  - 65 nm Global Foundry SAR ADC received early 2016
  - Large DAC mismatch observed due to some area not filled with dummy around 14 bit SAR (misunderstanding with foundry)
  - Cured on one chip with Focused Ion Beam
  - VERY PRELIMINARY results are encouraging

Serializer and Optical transmitter (SMU)

- LOCx2 serializer (250 nm Silicon On Saphire CMOS) for Phase I but recently experience problem in the fabrication process
  Back up solution investigated, porting LOCx2 in 130 nm CMOS GF. Common work with CERN on using GBTx
- VCEL array driver (VLAD, lpVLAD) : submitted to IMEC in Feb 2016, 4 channels. Test before summer expected
  35 (20) mW/ch for VLAD (lpVLAD).



VLAD

Conclusion

Tiles Front End readout for HL-LHC less demanding than LAr and well advanced :

- Discrete COTS approach similar to current one : expect to work as today
- Two ASICS approaches (QIE & FATALIC) : chips are existing

→ 2016 : Test beam campaign to compare performances with demonstrator and make baseline choice

Lar Front End R&D recently started. Still investigate different architectures and technologies

→ 2016 :

First prototype of CMOS analog part (mainly preamp) expected

Still need simulation study of best shaping/digital filtering approach for HL-LHC before TDR

On going work on ADC developments/serializers/optical transmitters based on Phase I development

Phase II radiation levels

Table 14. Radiation tolerance criteria of the LAr electronics for operation at HL-LHC for a total luminosity of 3000 fb^{-1}, including safety factors for background estimation, given in brackets. For COTS, an additional safety factor of 4 is included in case of production in unknown multiple lots. Furthermore, the ATLAS policy specifies annealing tests that allow reducing the enhanced low dose rate safety-factor to 1, which currently is set to 1.5 for ASICs and 5 for COTS.

	TID [kGy]		NIEL [n_{eq}/cm^2]		SEE [h/cm^2]	
ASIC	0.75	(2.25)	2.0×10^{13}	(2)	3.8×10^{12}	(2)
COTS (multiple lots)	9.9	(30)	8.2×10^{13}	(8)	1.5×10^{13}	(8)
COTS (single-lot)	2.5	(7.5)	2.0×10^{13}	(2)	3.8×10^{12}	(2)
LVPS (EMB and EMEC)	0.58	(30)	9.2×10^{12}	(8)	2.4×10^{12}	(8)
LVPS (HEC)	0.17	(2.25)	4.7×10^{12}	(2)	2.7×10^{11}	(2)

Phase 2 Radiation Tolerance Requirements (Estimate), TileCal HV_Opto					
Type	**Simulated Dose/Yr**	**Simulation Safety Factor**	**Low Dose Rate Safety Factor**	**Lot Variation Safety Factor**	**Total 10 Year Operation**
TID	8.13E-01 Gy/yr	1.5	5	4	2.44E+02 Gy
NIEL	7.62E+10 n/cm²/yr	2	1	4	6.10E+12 n/cm²
SEE	1.85E+10 p/cm²/yr	2	1	4	1.47E+12 p/cm²

QIE pipelined operation sequence