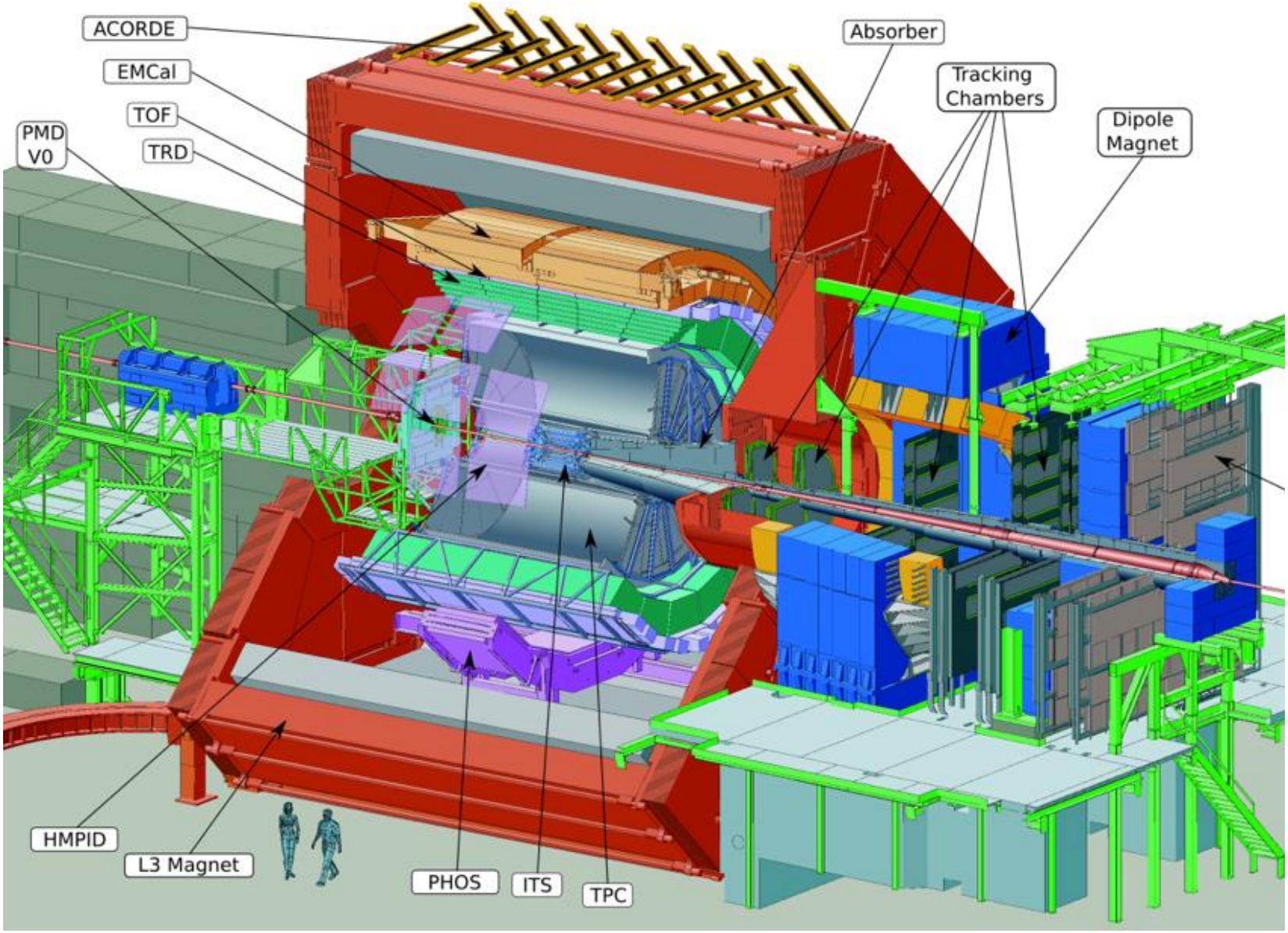
ALICE upgrade in LS2

A. Kluge, March 6, 2016

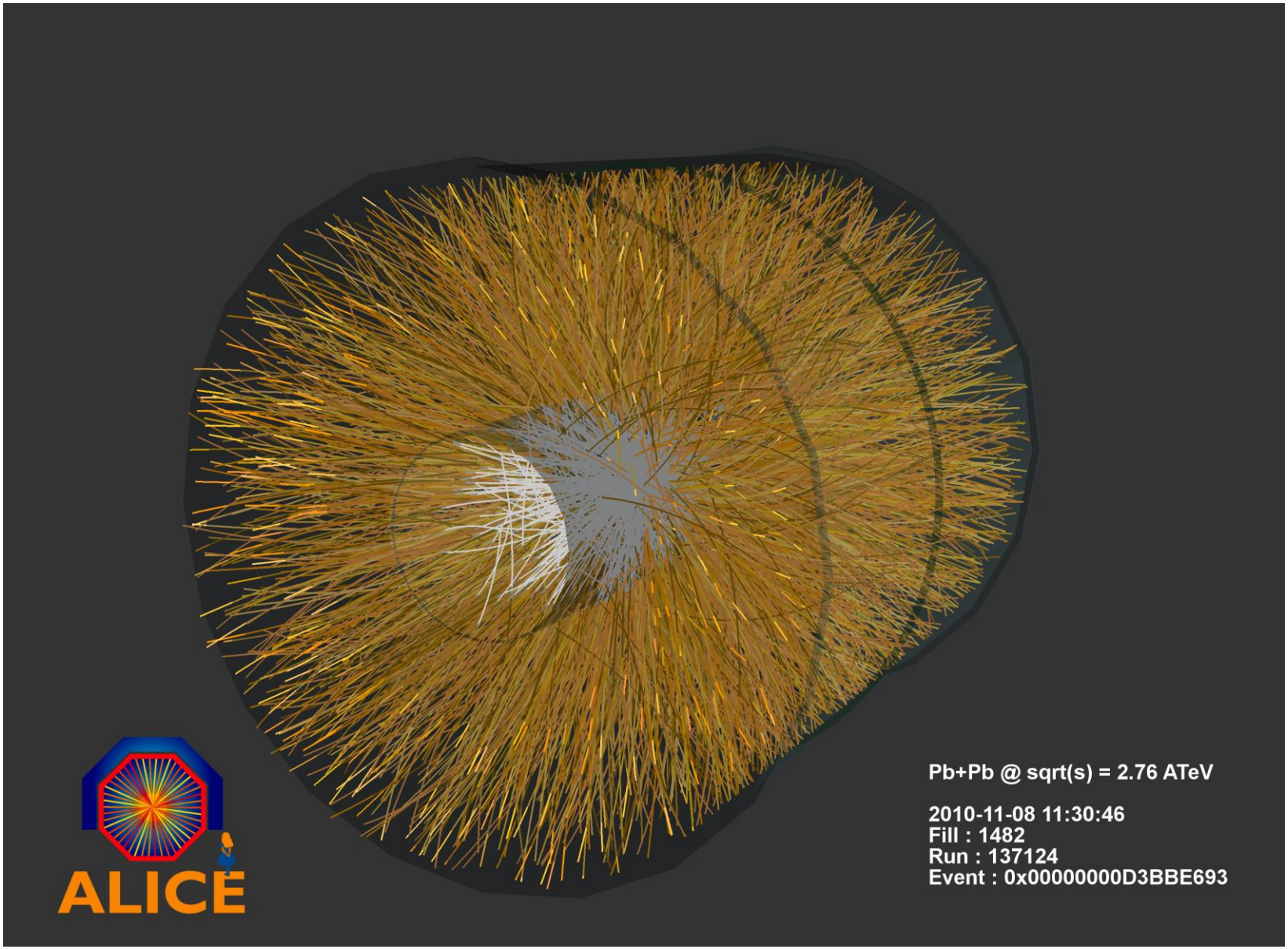
Outline

- What is different in ALICE?
- What do we upgrade?

ALICE

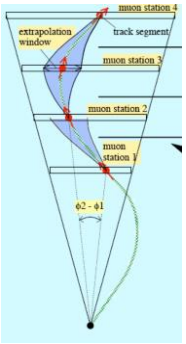

ACORDE
EMCal
TOF
TRD
PMD
V0
Absorber
Tracking
Chambers
Dipole
Magnet
HMPID
L3 Magnet
PHOS
ITS
TPC

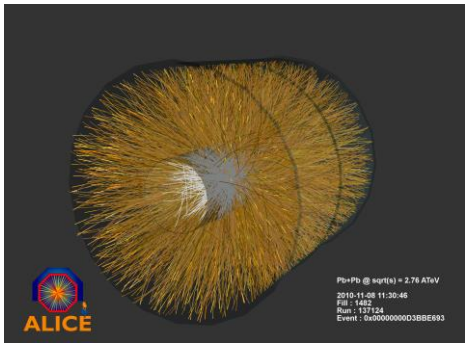
ALICE: heavy ion collision



ALICE Run1&2

- **At present:**
  - Interaction rate 8 kHz → max. trigger rate < 3.5 kHz
- **Why?**
  - Event topology too complex for simple electronics triggers

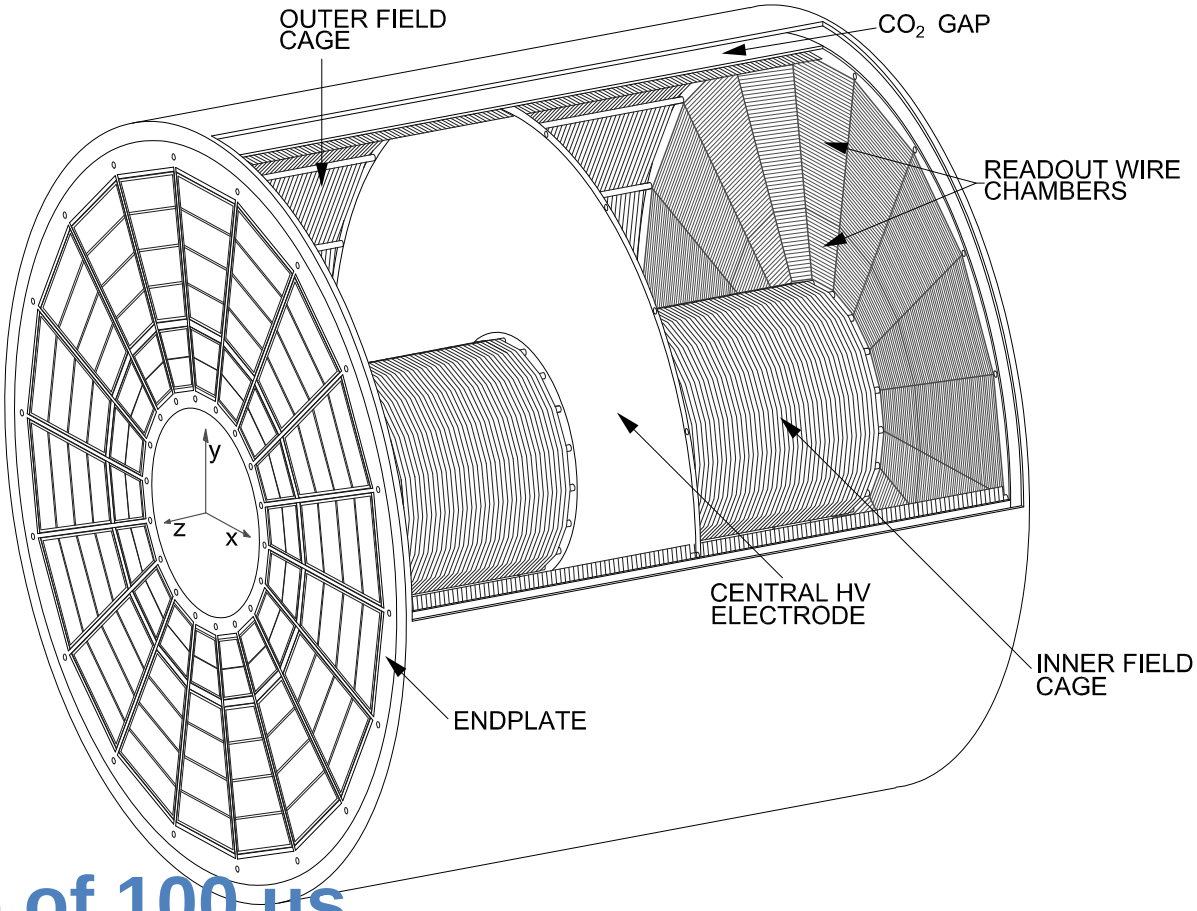




1 TB/s data in Run 3

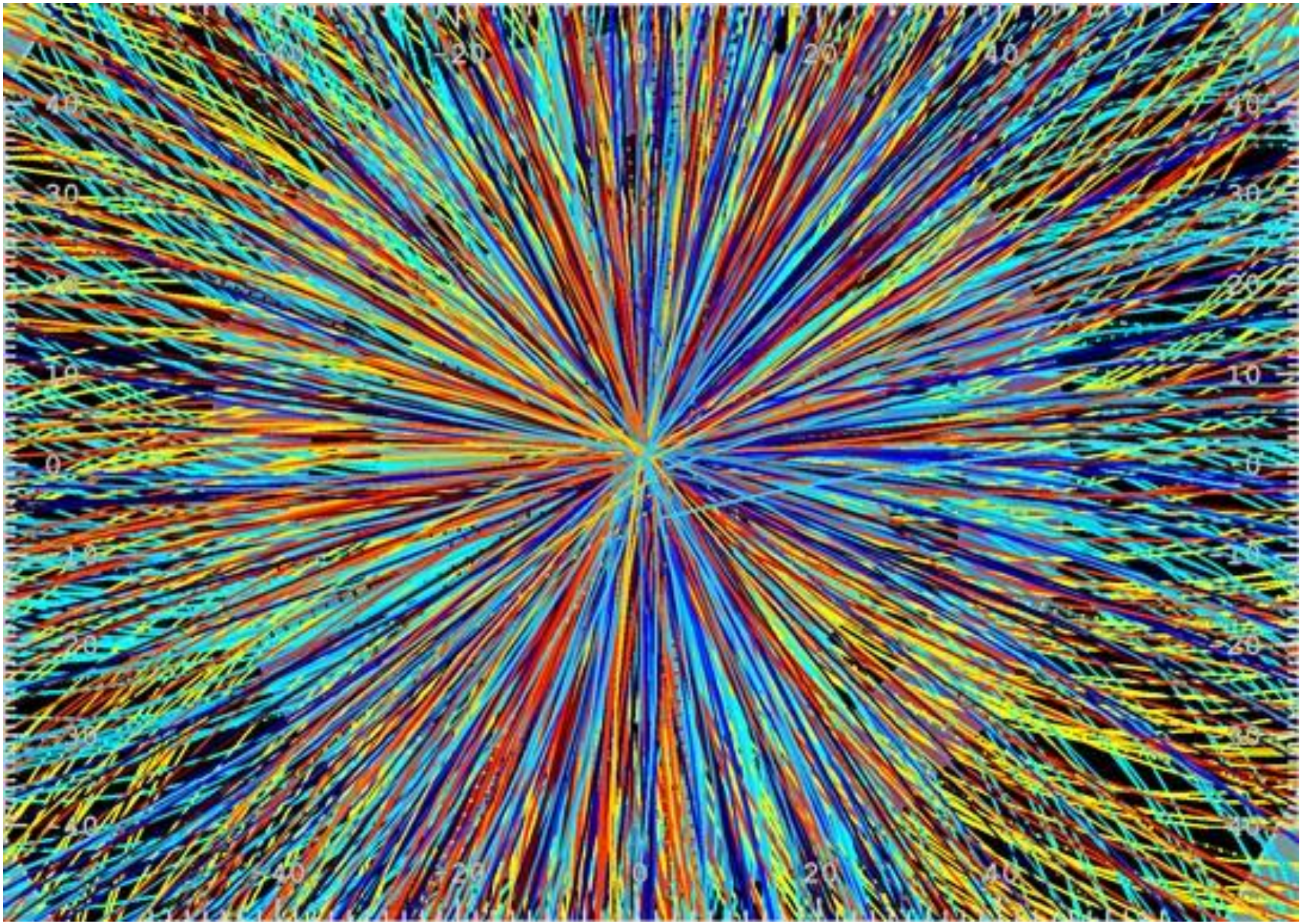
  - Reconstructed needed → All event needs to be read out
- **Reduction of interaction rate to 8 kHz**
  - Not all bunches have collisions

ALICE TPC



- **Drift time of 100 us**
- **Ions drift back →**
  - gating grid closed for 280 us → max. 3.5 kHz trigger rate

ALICE: upgrade goals



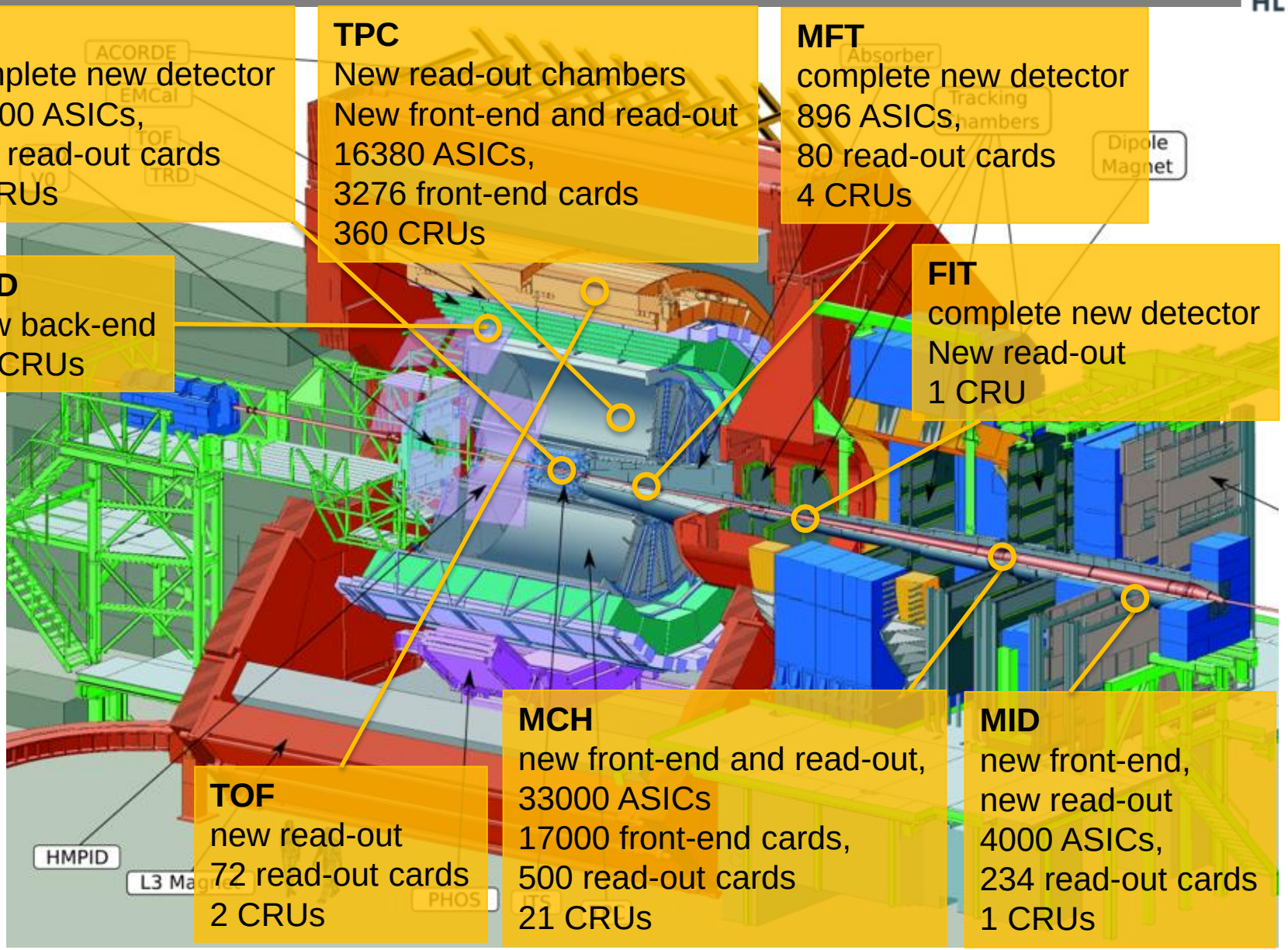
ALICE: upgrade goals

- **High precision measurements**
  - of rare probes at low pt
- **Cannot be selected with a trigger**
- **Require a large sample of events recorded**
- **Target**
  - Pb-Pb ≥ 10 nb-1 → 8 x 10^{10} events
  - pp (@5.5 TeV) ≥ 6 pb-1 → 1.4 x 10^{11} events
  - Gain factor 100 in statistics

Upgrade strategy

- **Upgrade ALICE read-out and online systems**
  - **Read-out all Pb-Pb interactions at**
    - 50 kHz ($L = 6 \times 10^{27}$ $cm^{-1}s^{-1}$) with min bias trigger
  - **Online data reduction ← no filtering**
    - Reconstruction of clusters and tracks
- **Improve vertexing and tracking at low p_t**
  - **New inner tracking system**

ALICE



ITS
complete new detector
24000 ASICs,
192 read-out cards
8 CRUs

TPC
New read-out chambers
New front-end and read-out
16380 ASICs,
3276 front-end cards
360 CRUs

MFT
complete new detector
896 ASICs,
80 read-out cards
4 CRUs

TRD
new back-end
30 CRUs

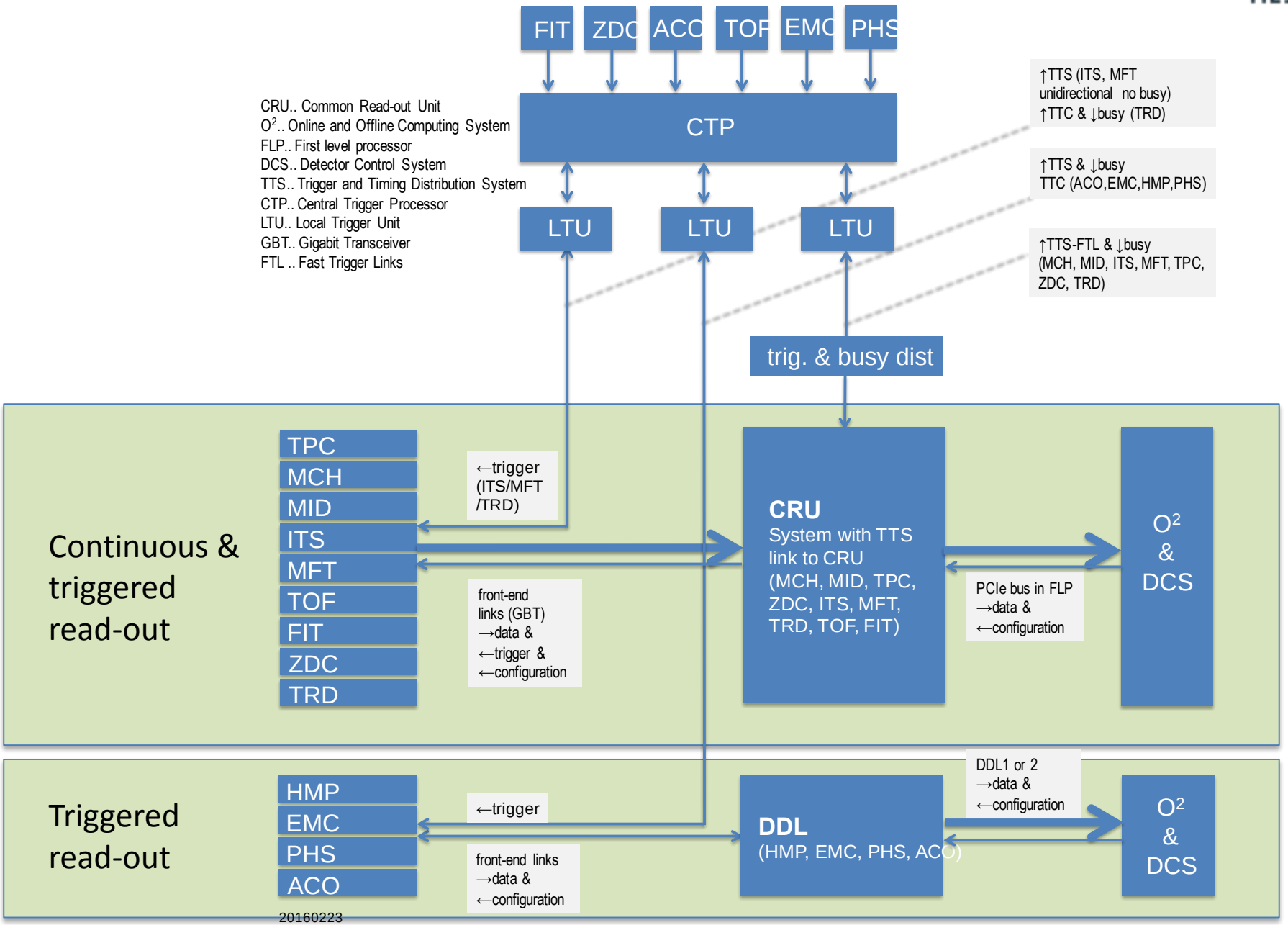
FIT
complete new detector
New read-out
1 CRU

TOF
new read-out
72 read-out cards
2 CRUs

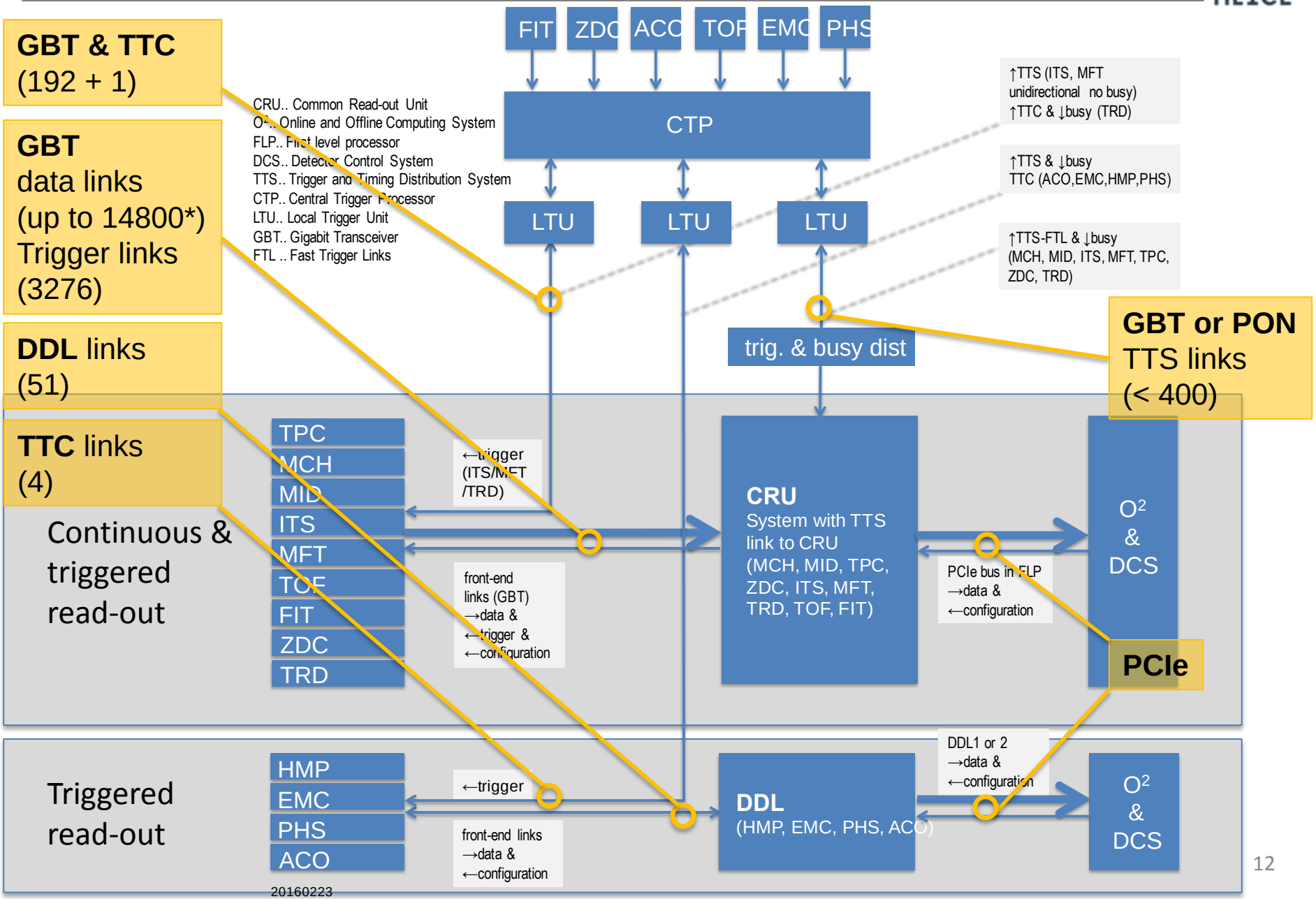
MCH
new front-end and read-out,
33000 ASICs
17000 front-end cards,
500 read-out cards
21 CRUs

MID
new front-end,
new read-out
4000 ASICs,
234 read-out cards
1 CRUs

Upgrade architecture overview

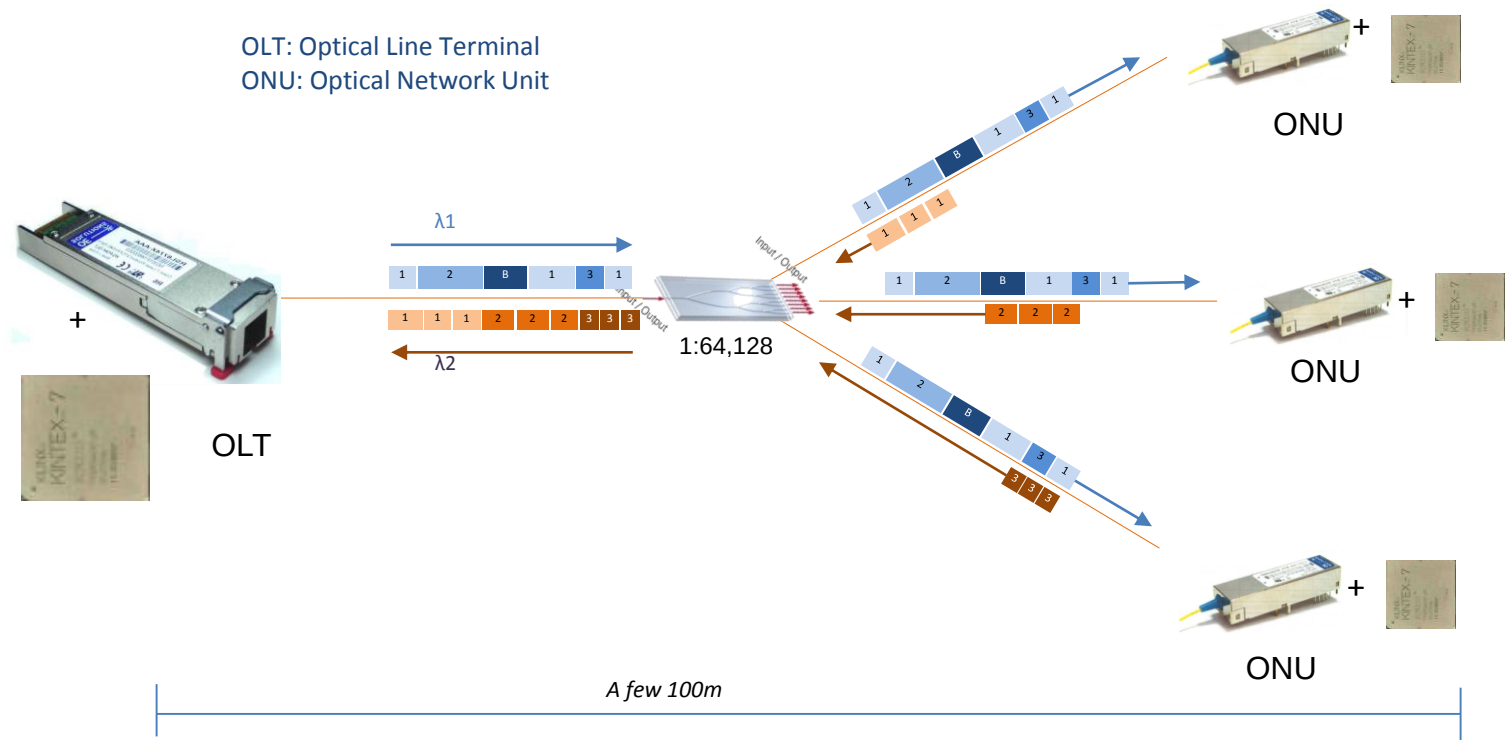


Upgrade architecture overview



TTS between CTP & CRU

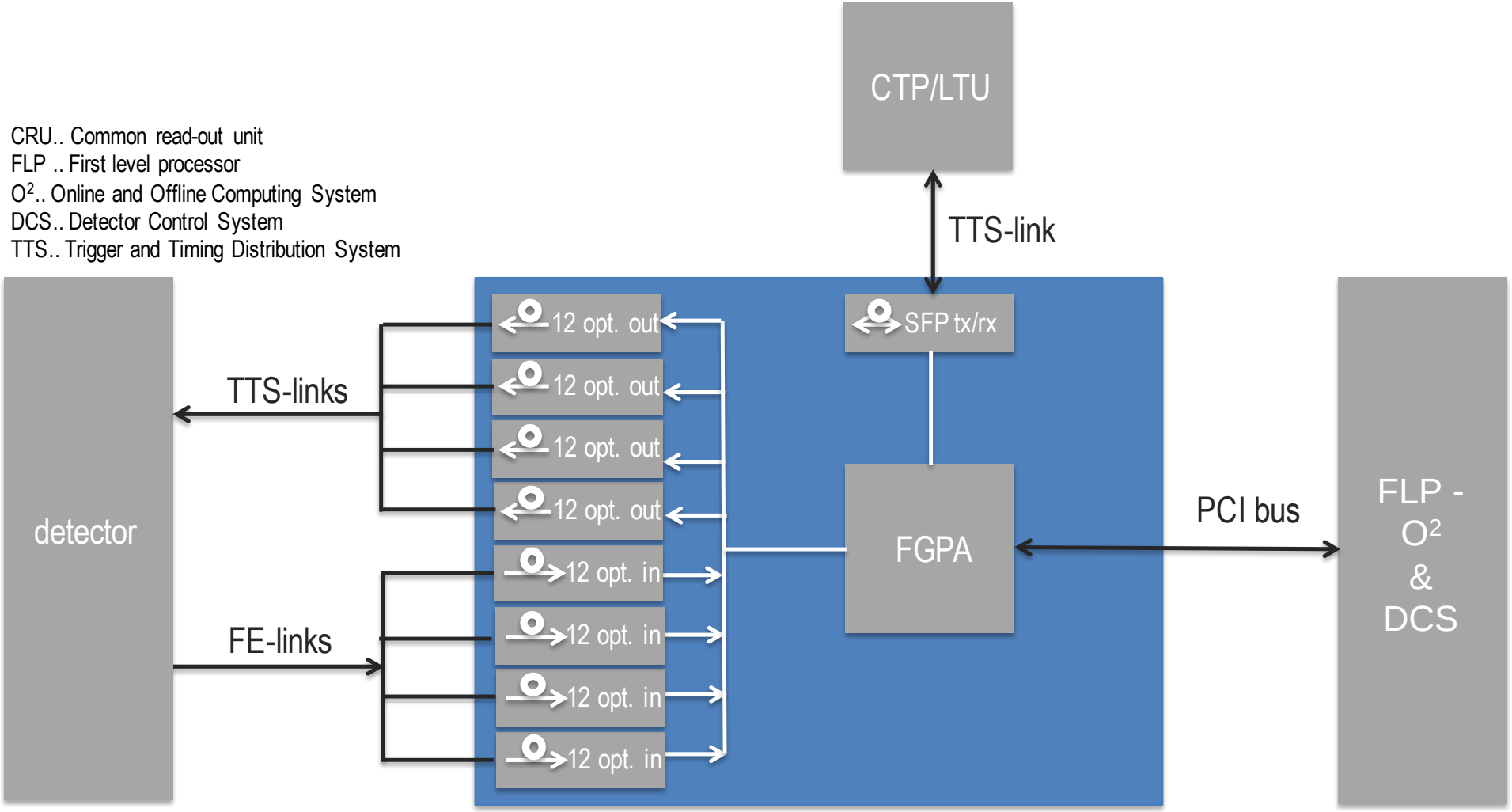
- **Option to use GBT links with active splitting or**
- **PON devices + FPGAs**
  - Fully synchronous with Bunch Clock
  - Custom protocol (removed typical PON protocol layers)
  - Detector busy transmitted back to CTP (delay of up to 8 us)



CRU – common read-out unit

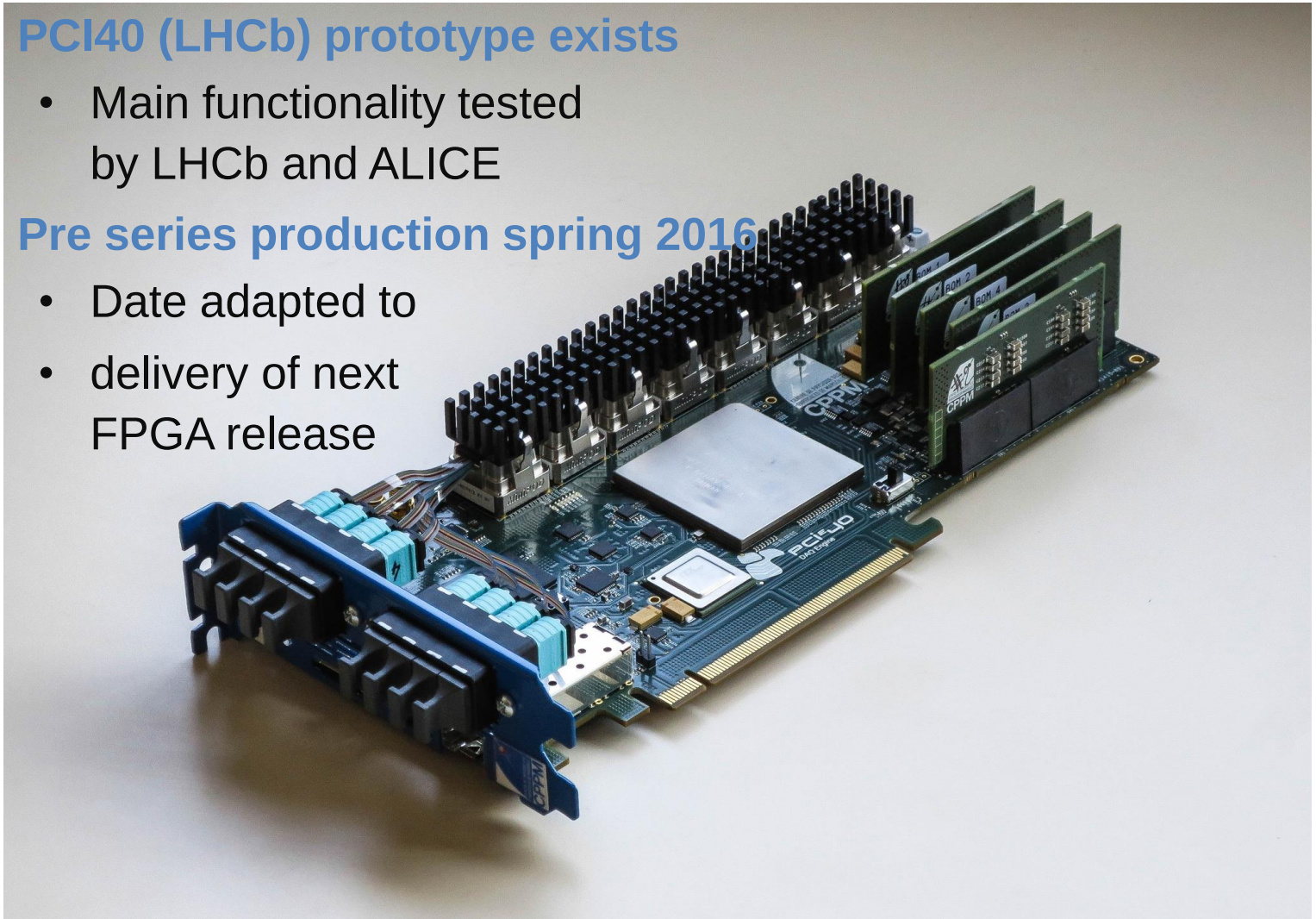
Common readout unit (CRU)

CRU.. Common read-out unit
FLP .. First level processor
O^2.. Online and Offline Computing System
DCS.. Detector Control System
TTS.. Trigger and Timing Distribution System



Common read-out unit – PCI40

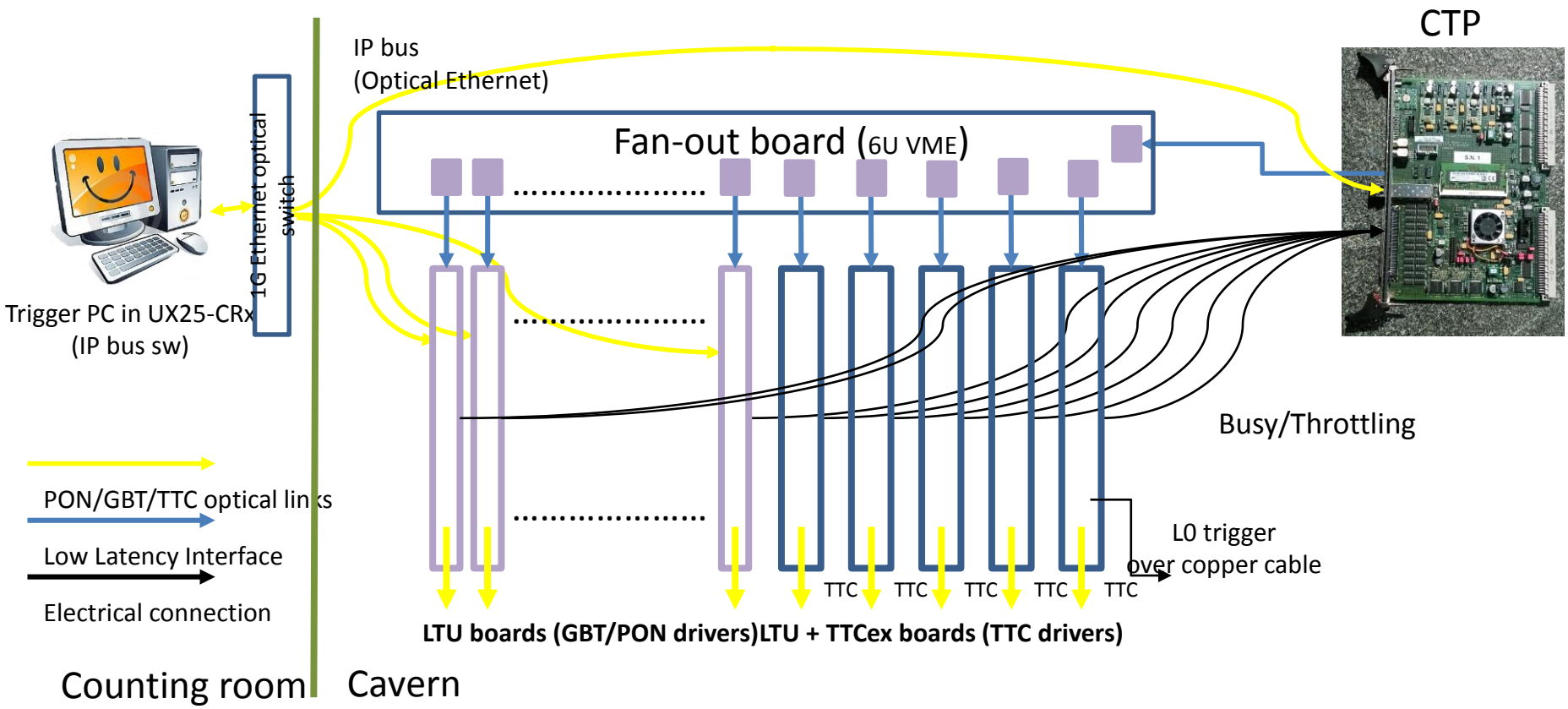
- **PCI40 (LHCb) prototype exists**
  - Main functionality tested by LHCb and ALICE
- **Pre series production spring 2016**
  - Date adapted to
  - delivery of next FPGA release



PCI40 prototype CPPM

CTP – Central Trigger processor

CTP

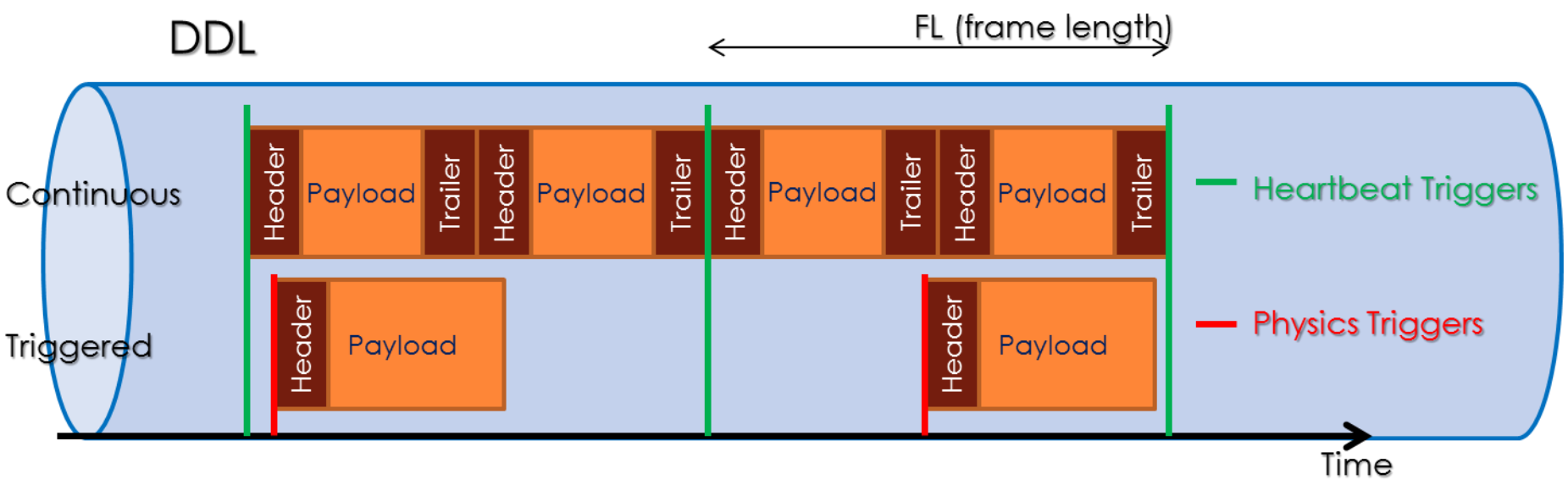

CTP
IP bus
(Optical Ethernet)
Fan-out board (6U VME)
1G Ethernet optical switch
Trigger PC in UX25-CRx
(IP bus sw)
Busy/Throttling
PON/GBT/TTC optical links
Low Latency Interface
Electrical connection
L0 trigger
over copper cable
TTC
TTC
TTC
TTC
TTC
LTU boards (GBT/PON drivers)LTU + TTCex boards (TTC drivers)
Counting room
Cavern

Trigger signals

Level	Trigger Input to CTP [ns]	contributing detectors
LM	425	FIT
L0	1200	ACO, EMC, PHO, TOF, ZDC
L1	#6100	EMC, ZDC

- **LM .. TRD & ITS: by FIT only**
- **L0 .. main trigger signal: by FIT & additional trigger inputs**
- **L1 .. optional EMC-jet and ZDC contribution: long latency**

Heartbeat trigger

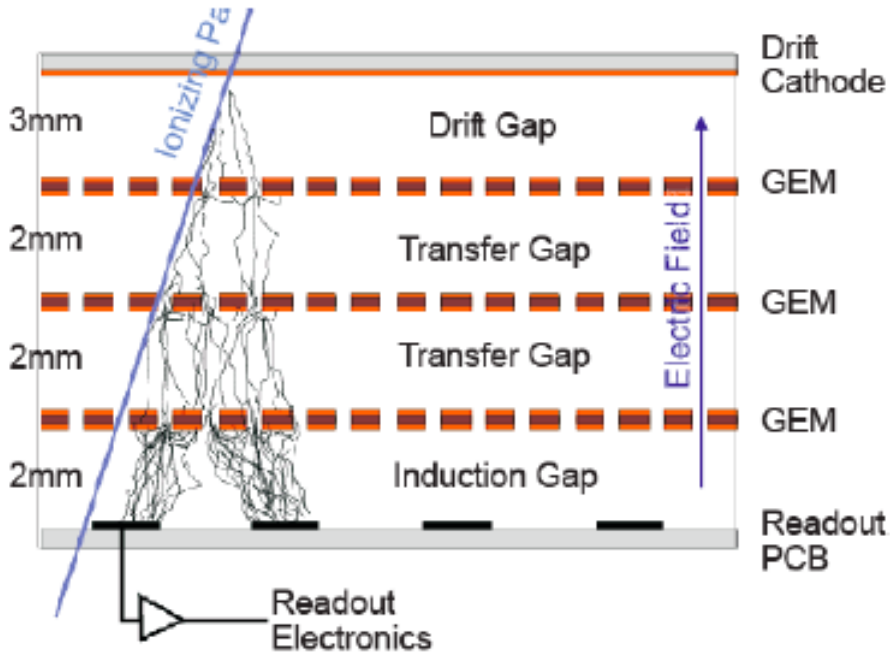


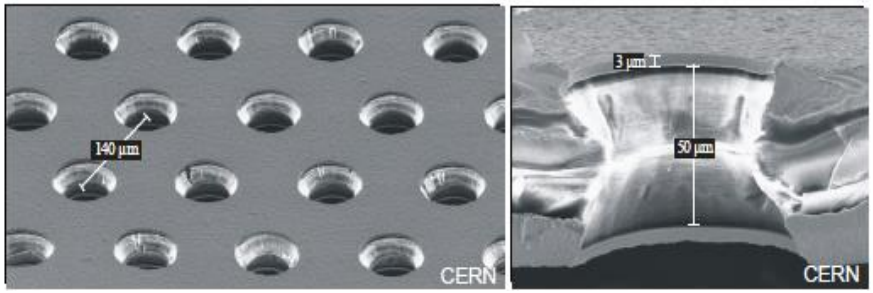
- **Periodic non-physics trigger to**
  - synchronize data from non-/continuous readout detectors
  - synchronize local copies of bx-id, orbit counters

TPC

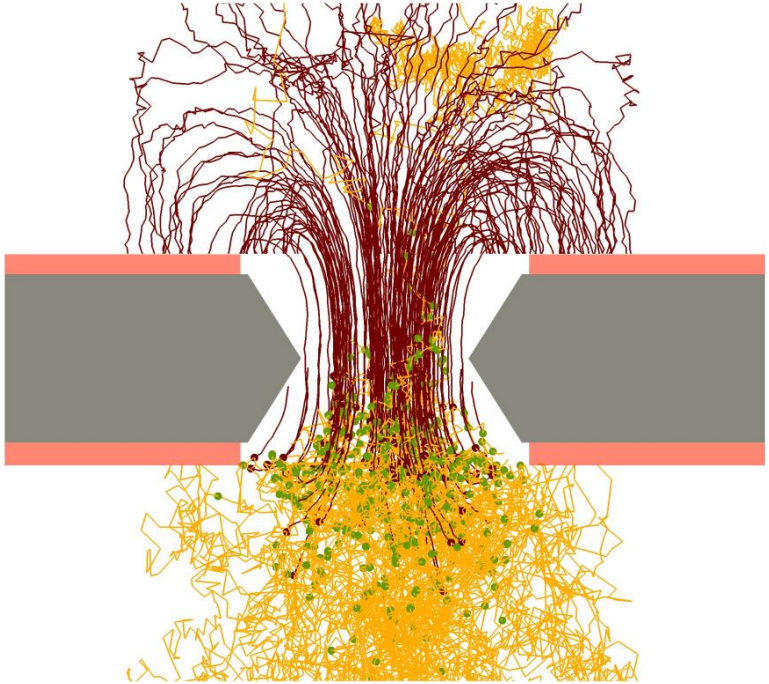
I just said it works only up to 3500 Hz

multiple GEM principle



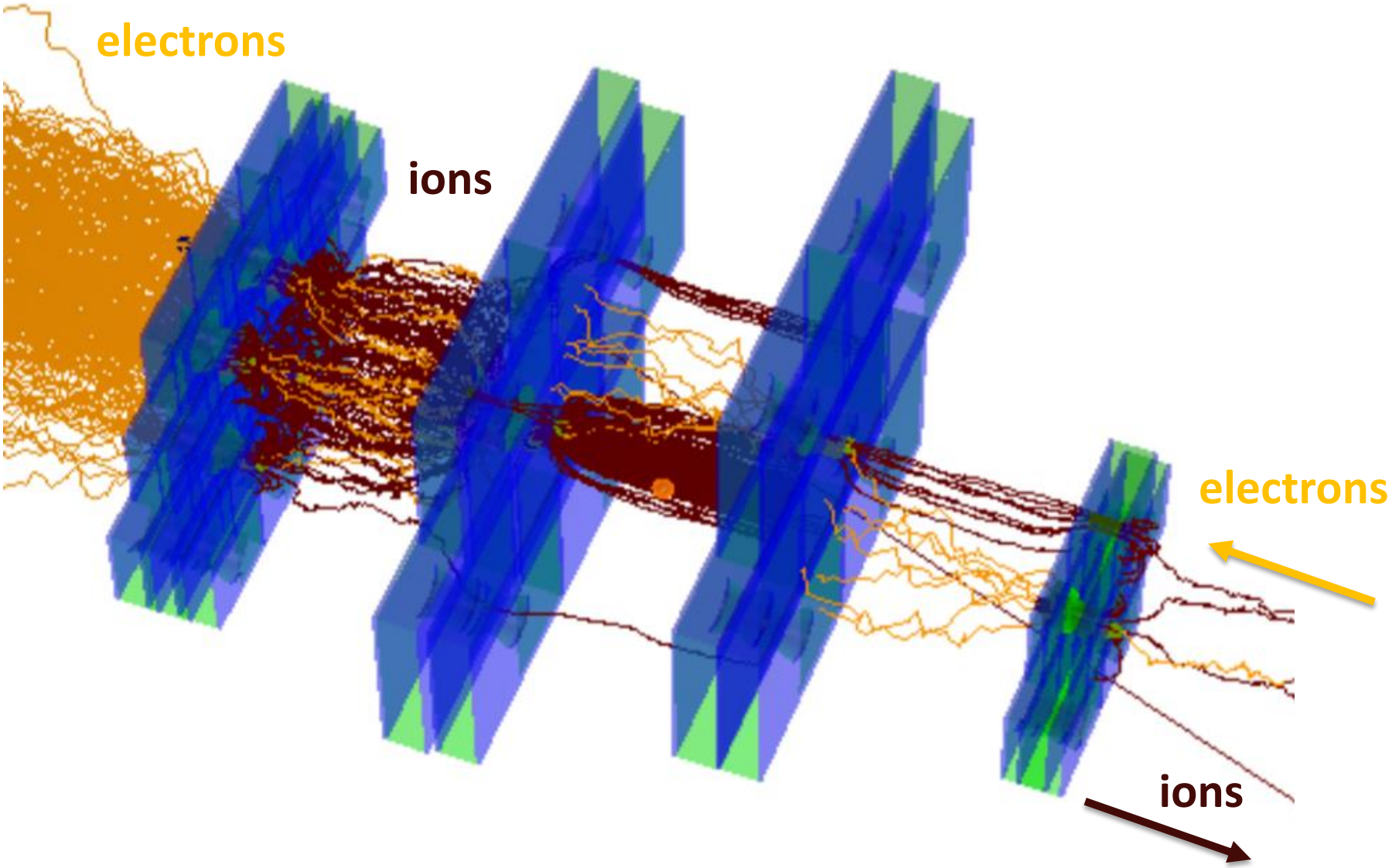


Electron microscope photograph of a GEM foil



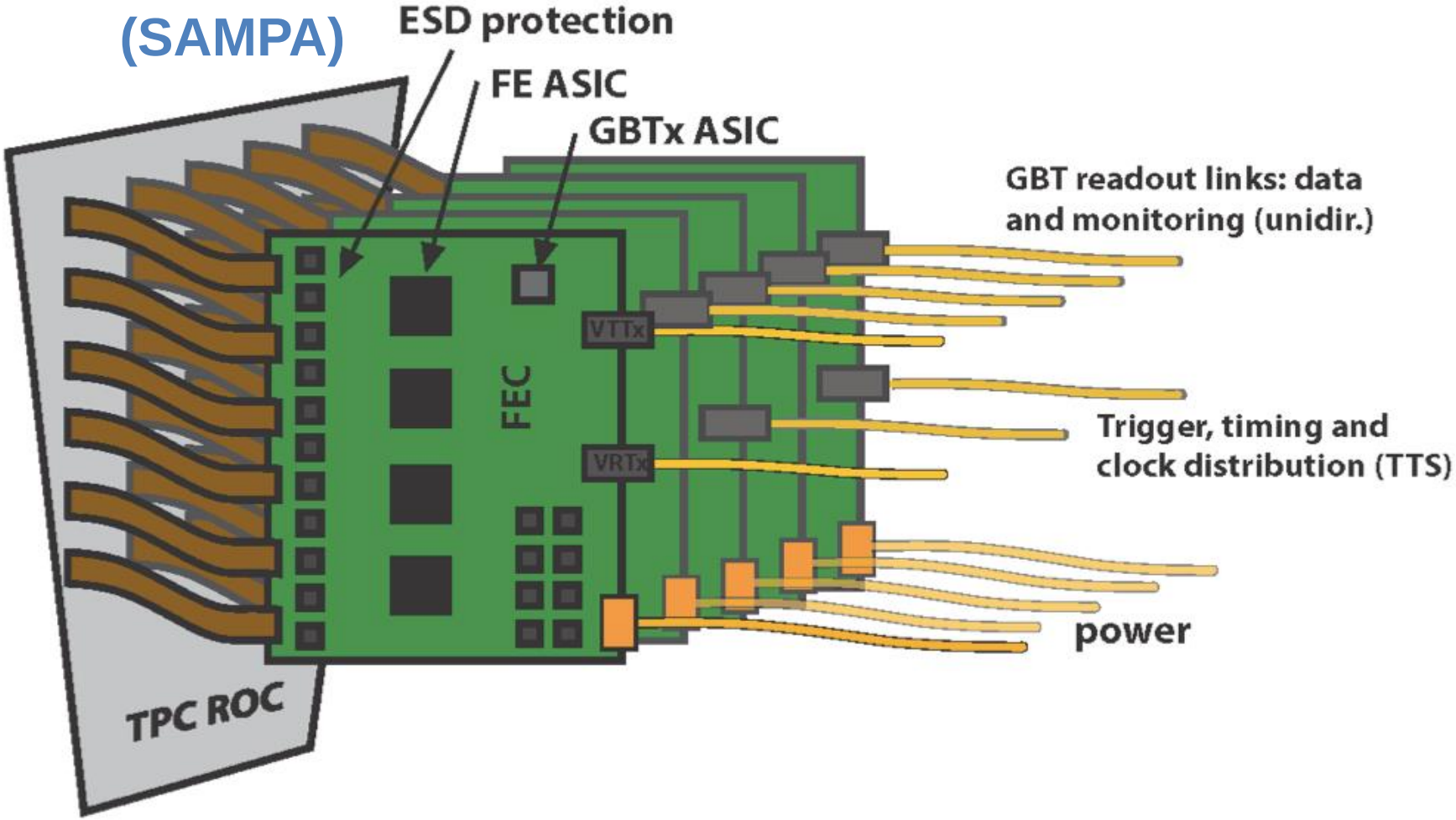
GEMs are made of a copper-kapton-copper sandwich, with holes etched into it

4 GEM simulation



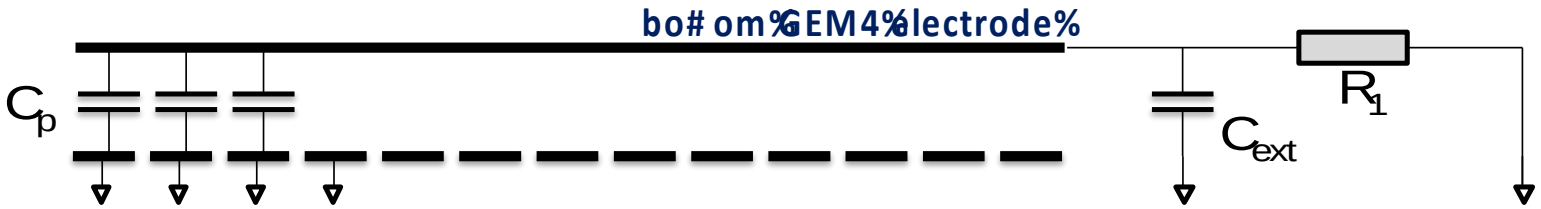
TPC front-end card

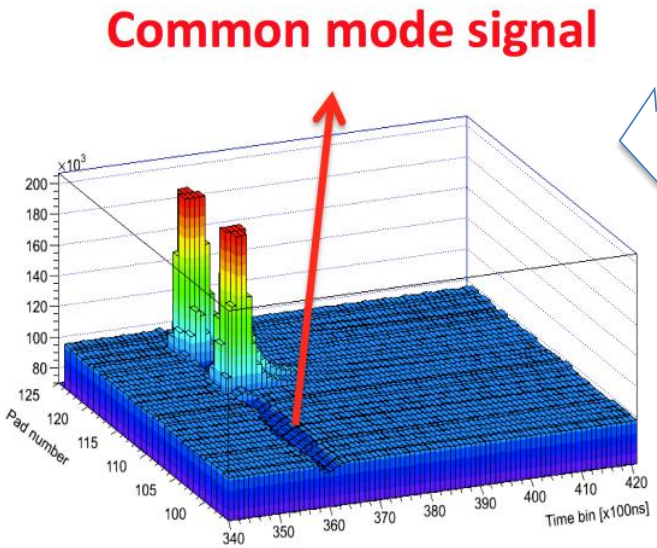
- 524.160 channels @ 50 kHz read-out rate
- 3276 front-end cards & ~ 16380 front-end ASICs (SAMPA)



TPC: common mode effect

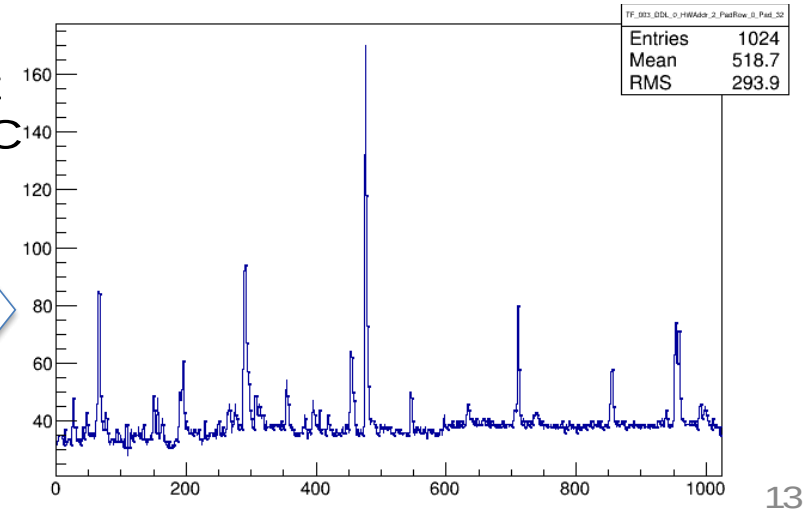
- Common mode effect: Baseline shift and "noise" due to capacitive coupling of electrodes in readout structure





Measurement in current TPC

Simulation of the effect at large occupancies



C. Lippmann

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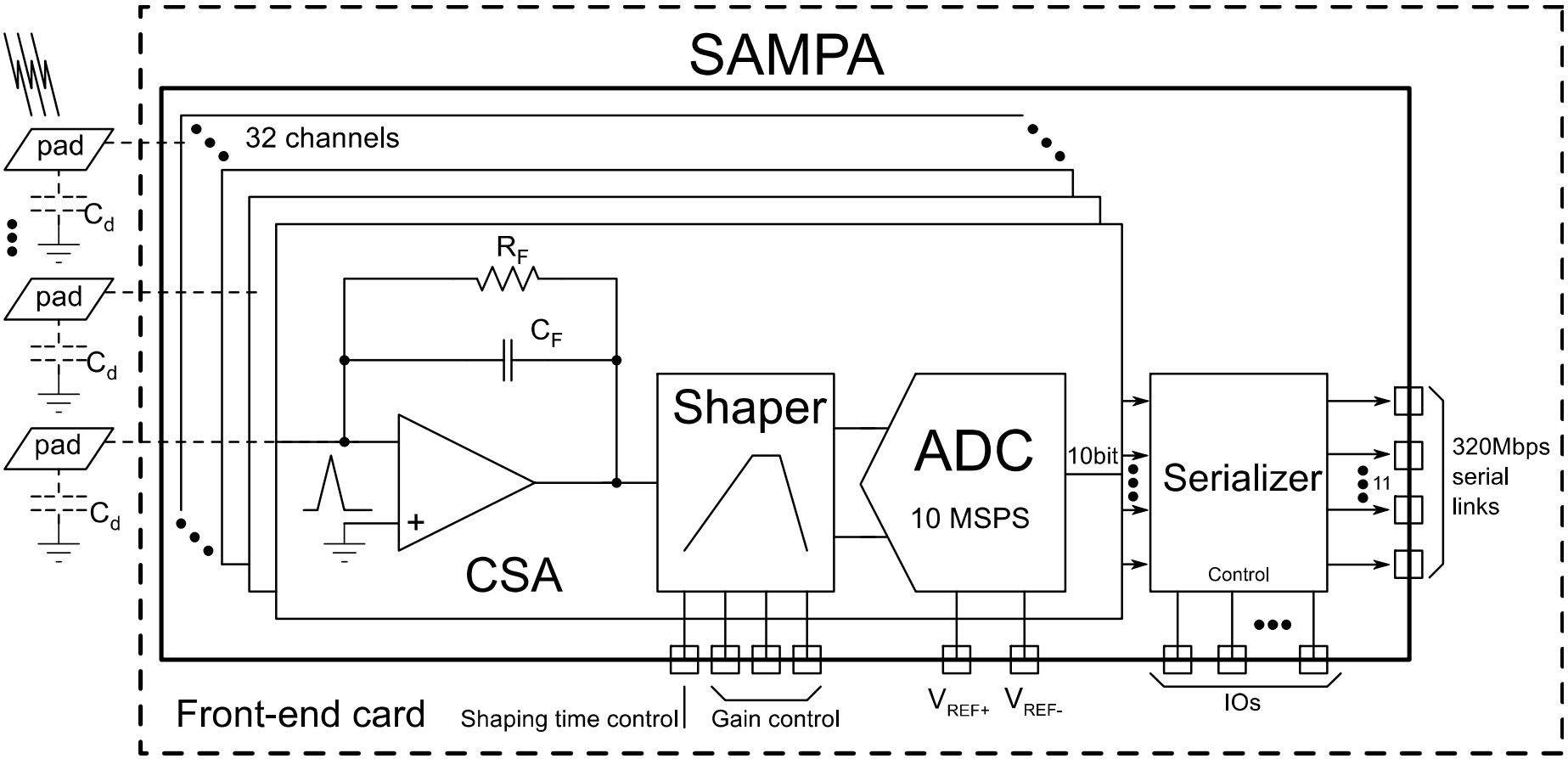
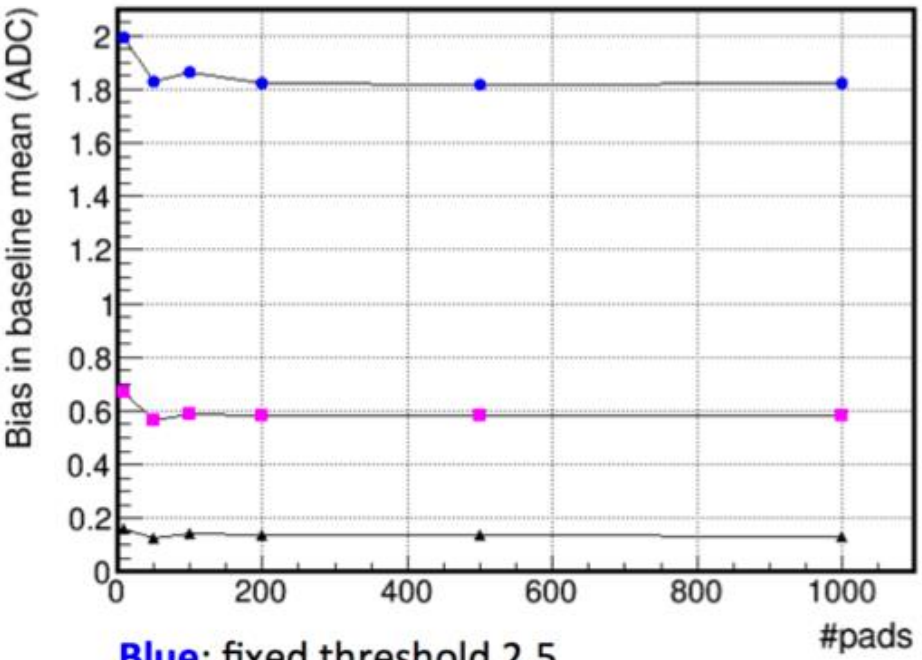
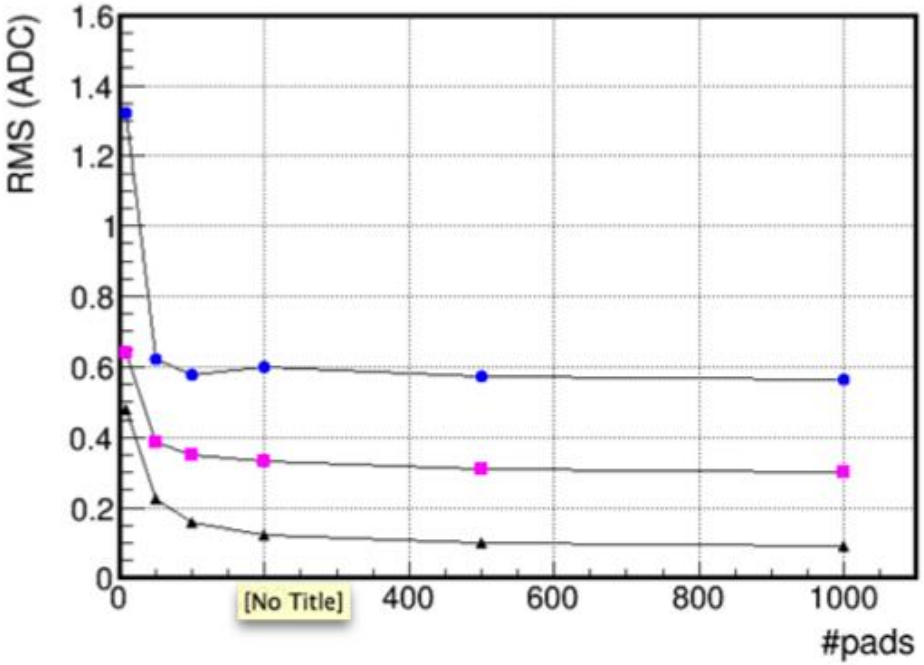
SAMPA front-end ASIC



Base line correction in CRU



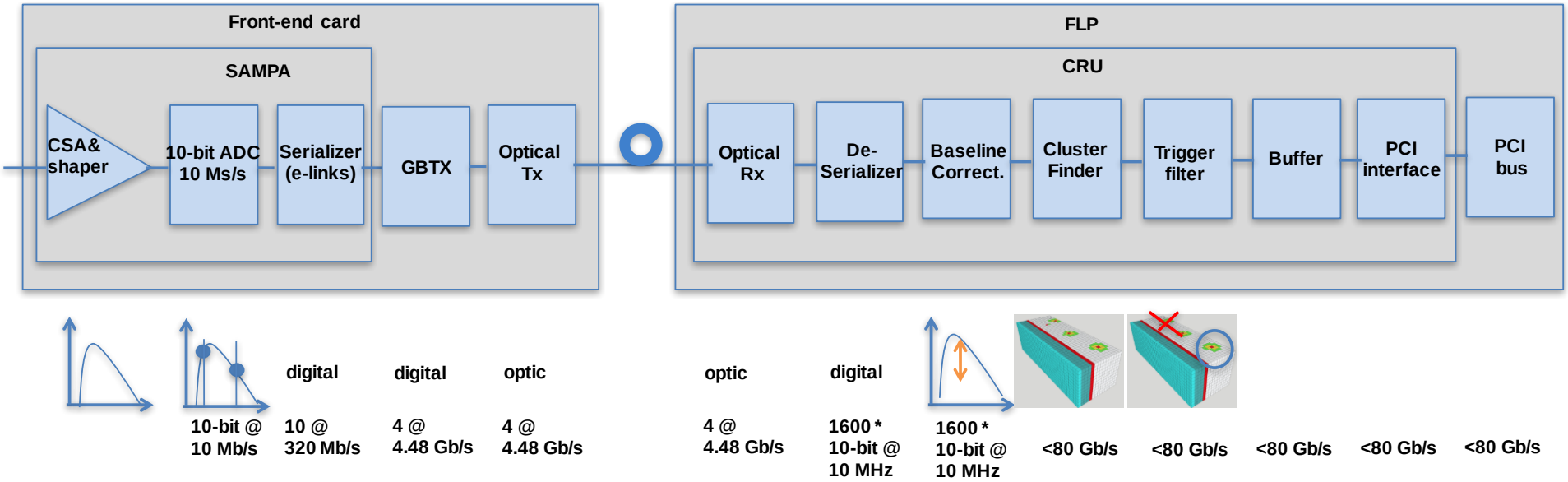


Blue: fixed threshold 2.5

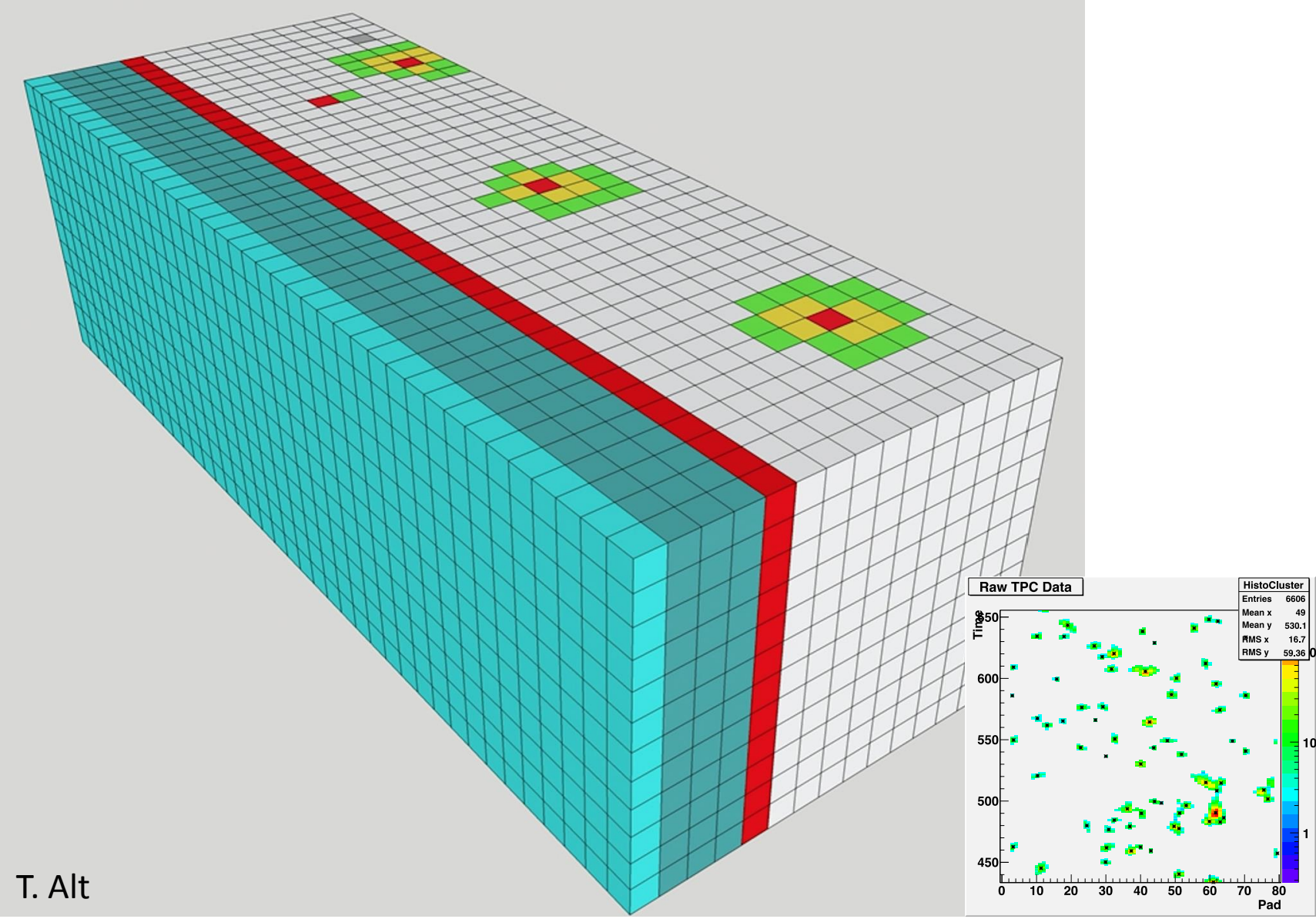
Magenta: last value kept inside detected signal

Black: detected signal region excluded from mean calculation

TPC processing chain



CRU processing



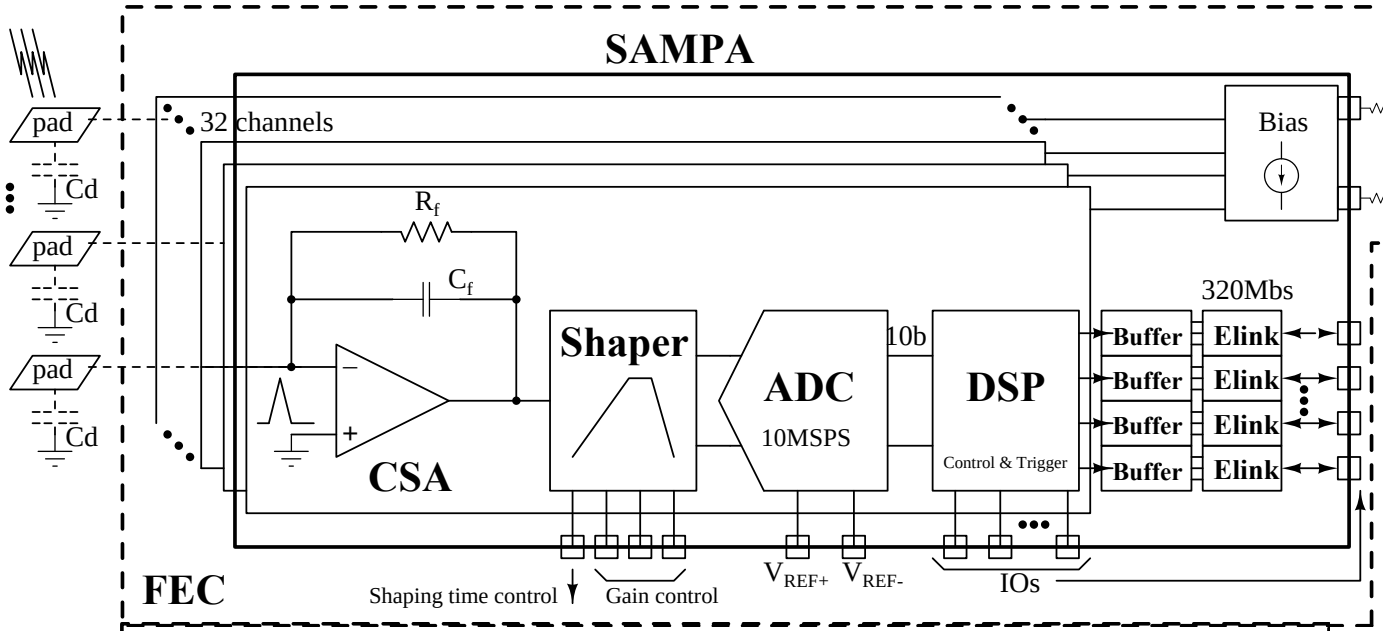
T. Alt

SAMPA

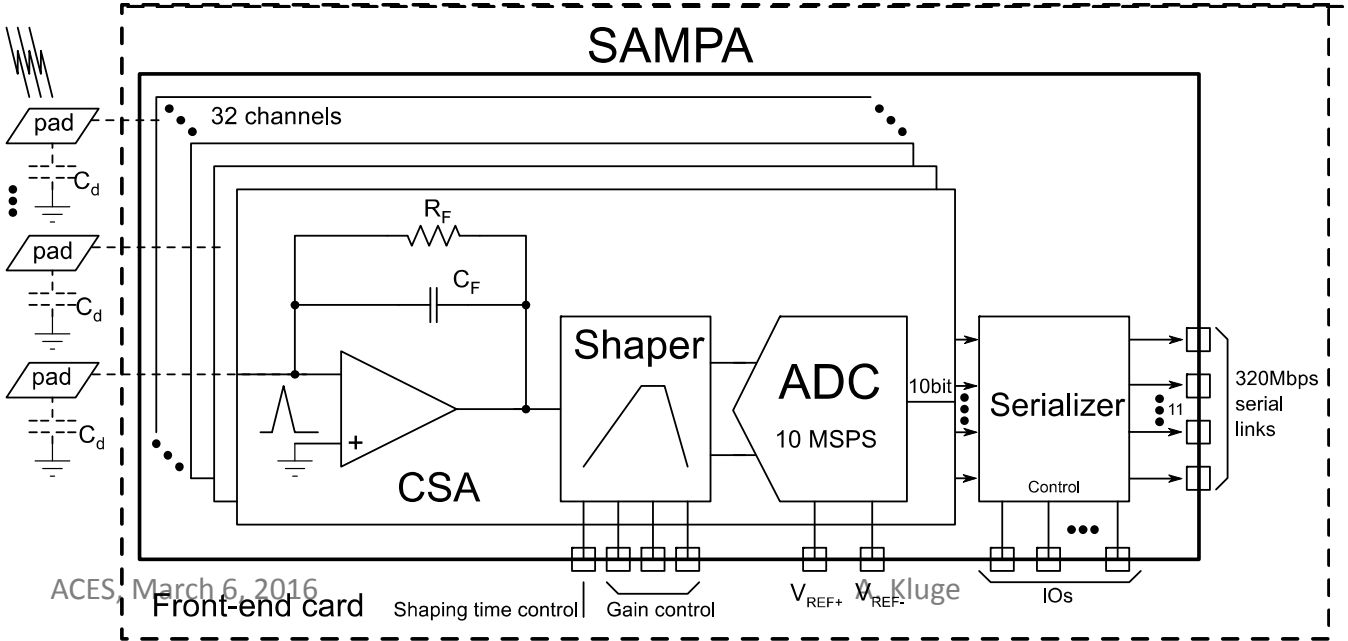
SAMPA

- **TPC & muon chambers (MCH)**
  - 32 channel amplifier-shaper-ADC-DSP
  - triggerless/continuous & triggered readout
  - < 600 e @ 25 pF (TPC), < 950 e @ 40 p (MCH)
  - bi-polarity input
  - 10 bit ADC – 5/10/20 Msamples/s
  - on ASIC base-line correction and zero suppression
  - 1-11 (programmable) x 320 Mbit/s serial outputs
  - 130 nm TSMC CMOS process

SAMPA: 2 read-out modes



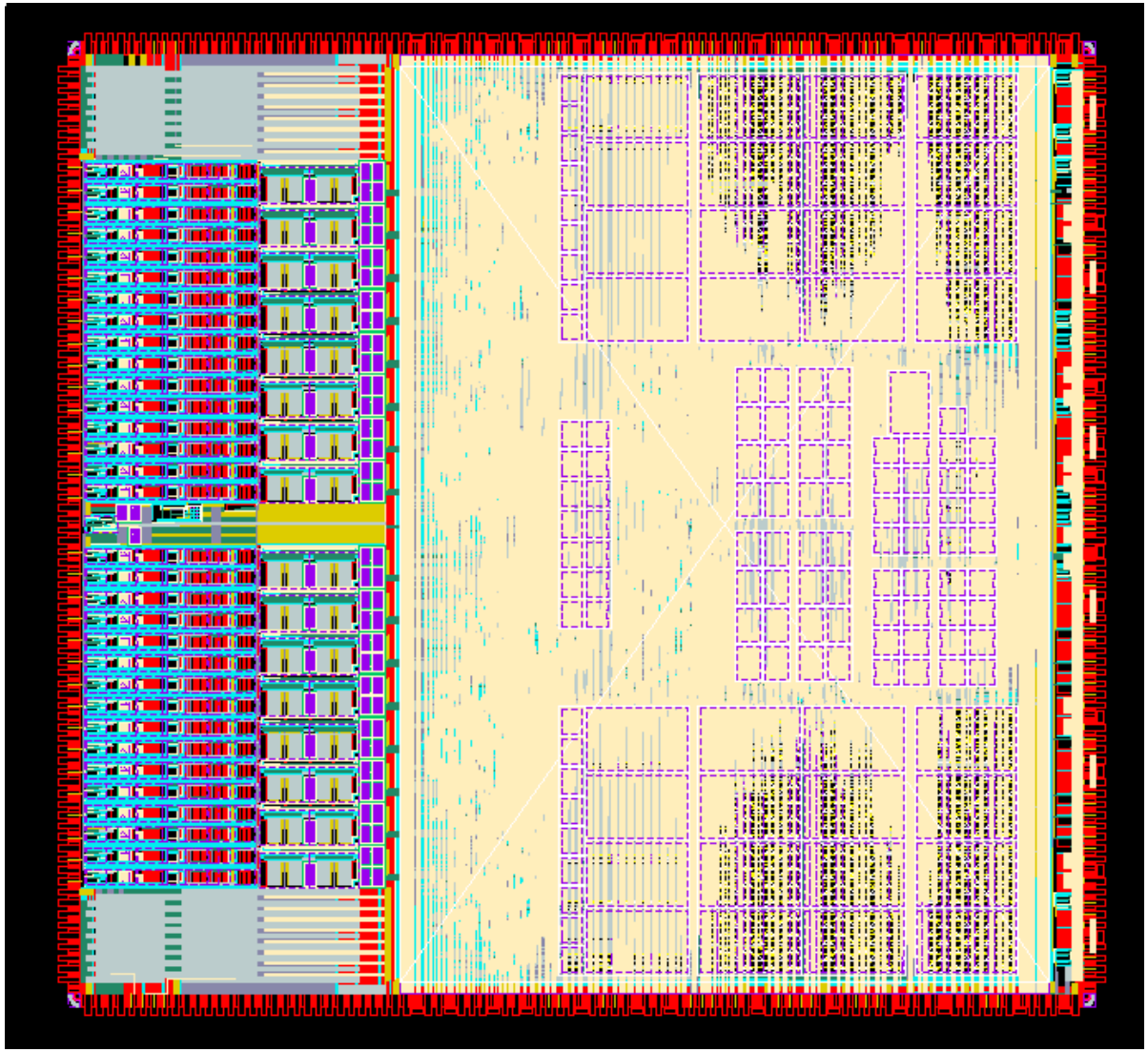
Data processed by DSP
-Baseline correction and ZeroSuppression and/or
-Compression



Direct serialization:
all data via 10 e-links
(DSP bypassed)

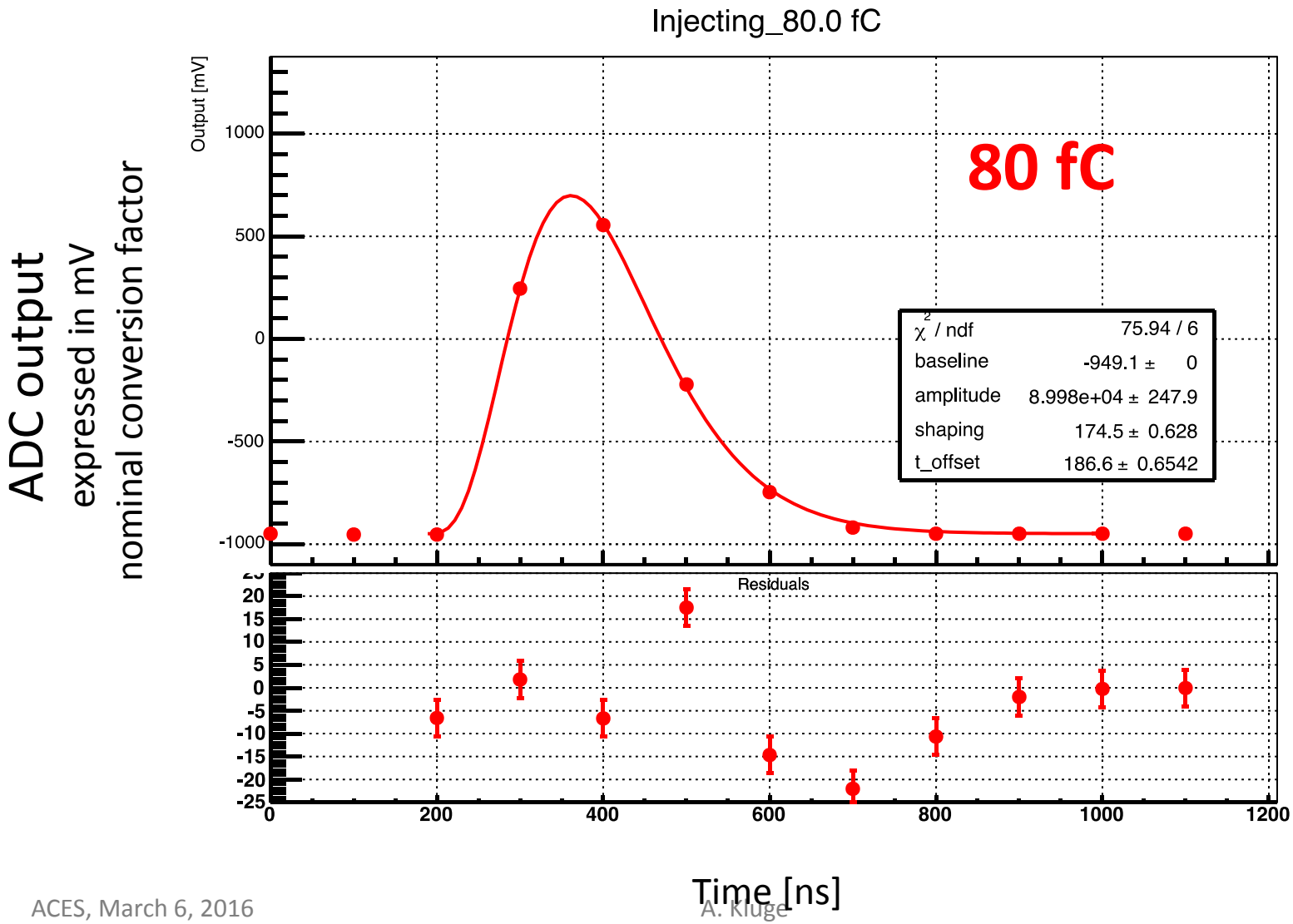
SAMPA

Die size: 9.575 x 8.985 mm^2



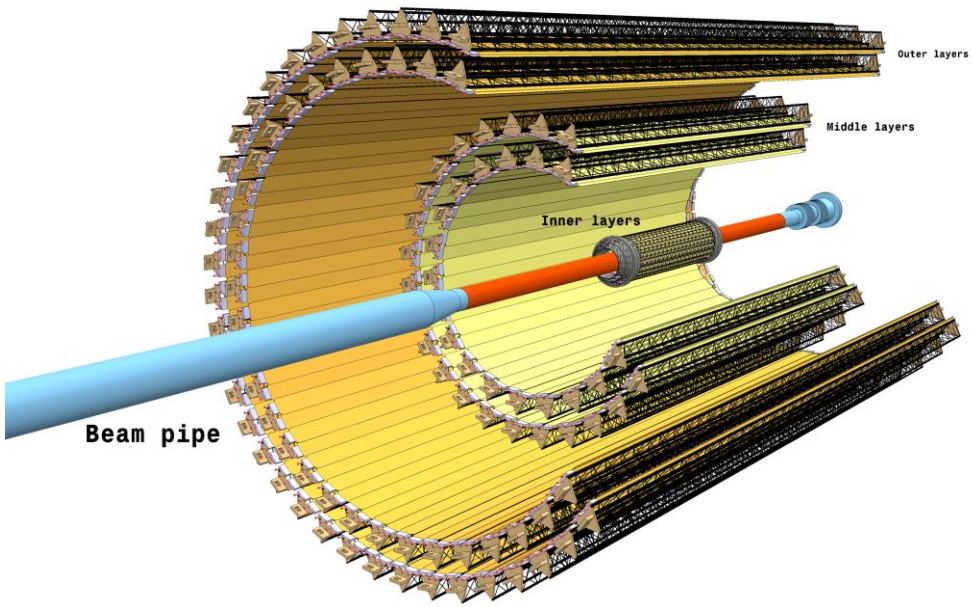
Simulation 8 ch. FE + ADC: response 20mV/fC neg

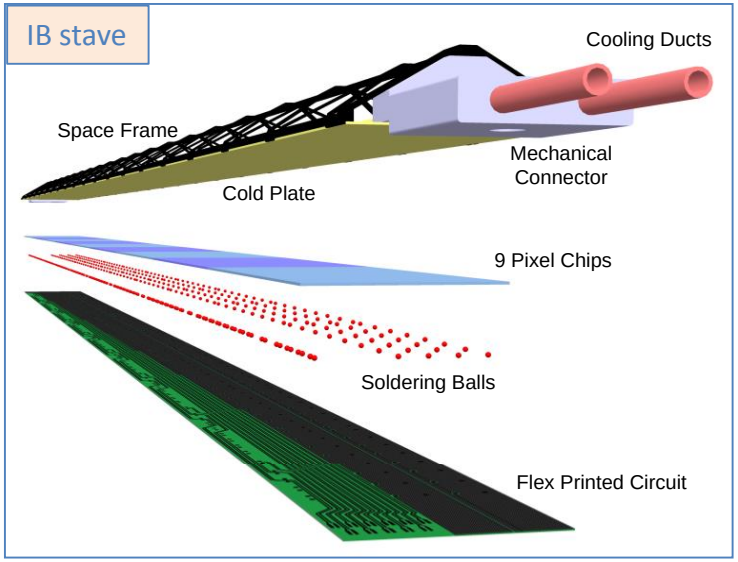
ADC ENOB simulation: 9.6 bit

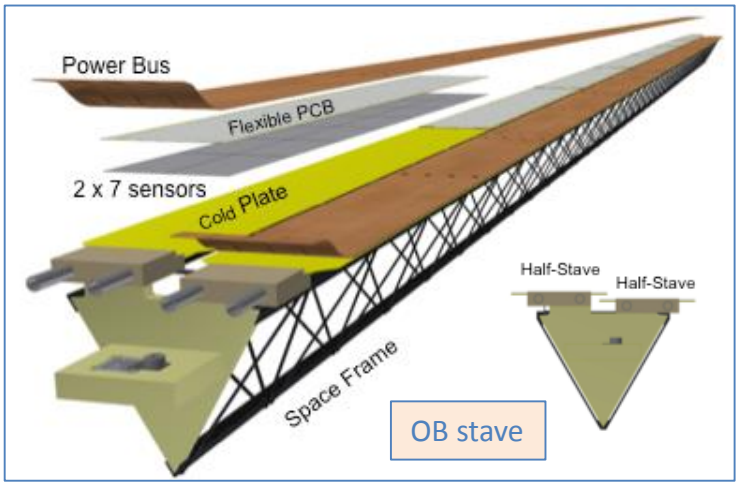


ITS – Inner Tracker System

New ITS Layout





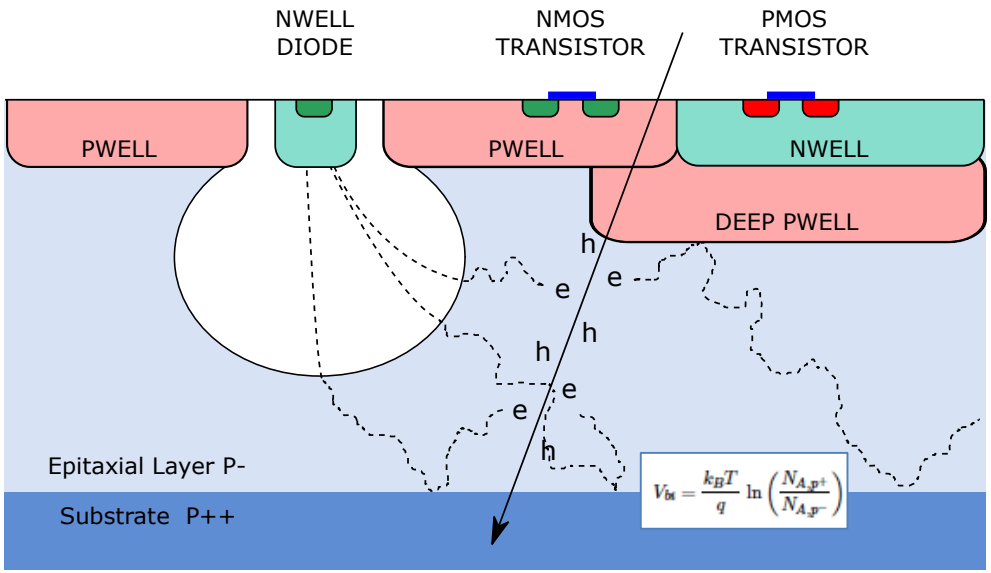


L. Musa

- 7-layer barrel based on CMOS sensors
- Radial coverage 22 – 400 mm
- Total active area ~10m^2
- ~ 24,000 pixel chips (12.5 G pixels)
- Radiation: ~2.7 Mrad (~1.7x10^{13} 1MeV n_{eq}/cm^2) including safety factor 10

ITS Pixel Chip – technology choice

CMOS Pixel Sensor using TowerJazz 0.18μm CMOS Imaging Process



Tower Jazz 0.18 μm CMOS

- feature size 180 nm
- metal layers 6
- gate oxide 3nm

substrate: $N_A \sim 10^{18}$
epitaxial layer: $N_A \sim 10^{13}$
deep p-well: $N_A \sim 10^{16}$

- High-resistivity (> 1kΩ cm) p-type epitaxial layer (18μm to 30μm) on p-type substrate
- Small n-well diode (2 μm diameter), ~100 times smaller than pixel => low capacitance
- Application of (moderate) reverse bias voltage to substrate (contact from the top) can be used to increase depletion zone around NWELL collection diode
- Deep PWELL shields NWELL of PMOS transistors to allow for full CMOS circuitry within active area

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pALPIDE-1&2 – Main Design Features

ALPIDE full-scale prototypes

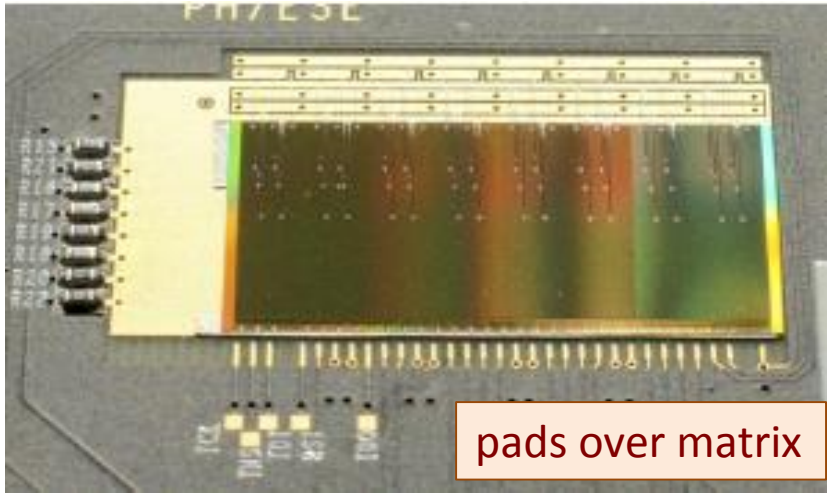


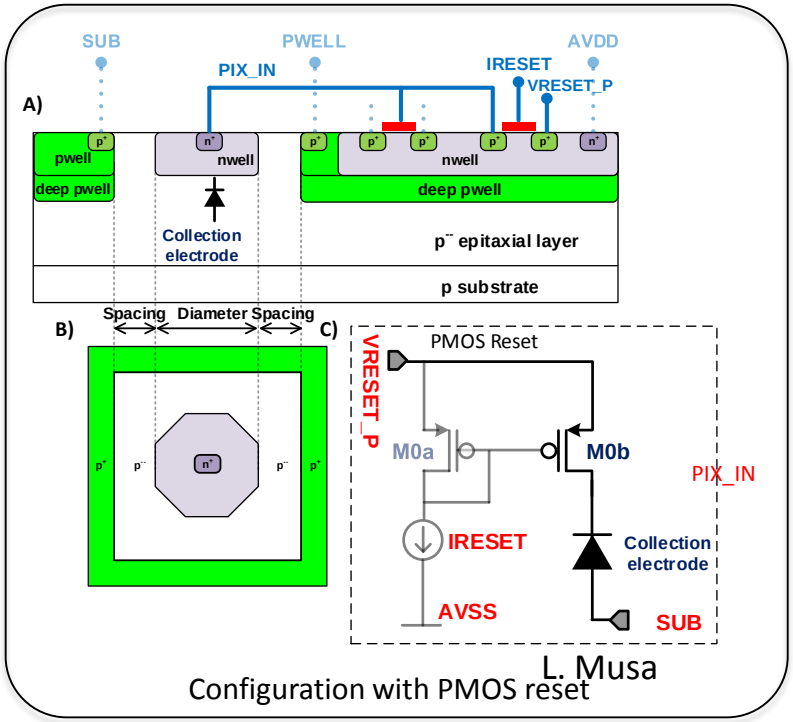
Figure: picture of pALPIDE-2

Main parameters

- Dimensions: 30mm x 15 mm
- Pixel Matrix: 1024 cols x 512 rows
- Pixel pitch: 28μm x 28μm
- Integration time: <10μs
- Power consumption: < 40mW/cm^2
- (vers. 3) 8 sectors with different pixels

Matrix divided in 8 sectors, each with 128 cols x 512 rows

- Collection node: octagonal 2μm diameter
- Spacing NWELL and PWELL: 2μm to 3μm
- 2 reset mechanism: diode, PMOS



Configuration with PMOS reset

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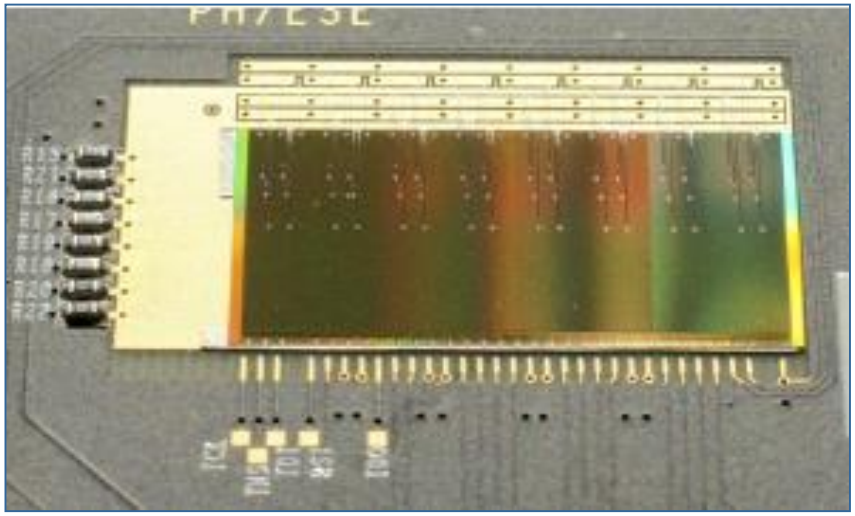
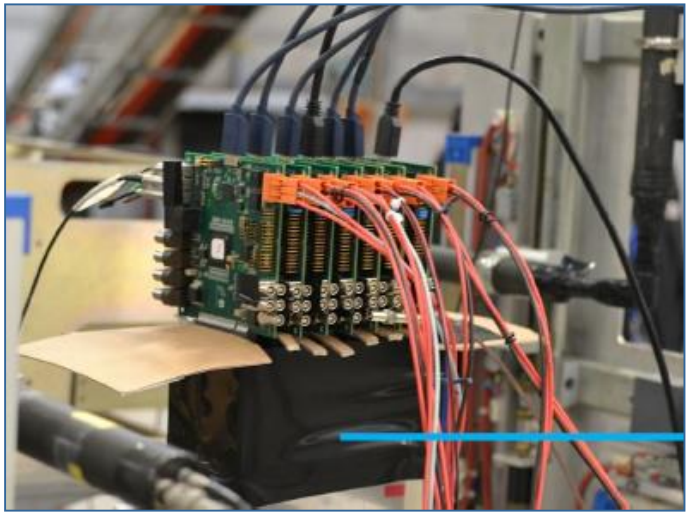
ITS Pixel Chip

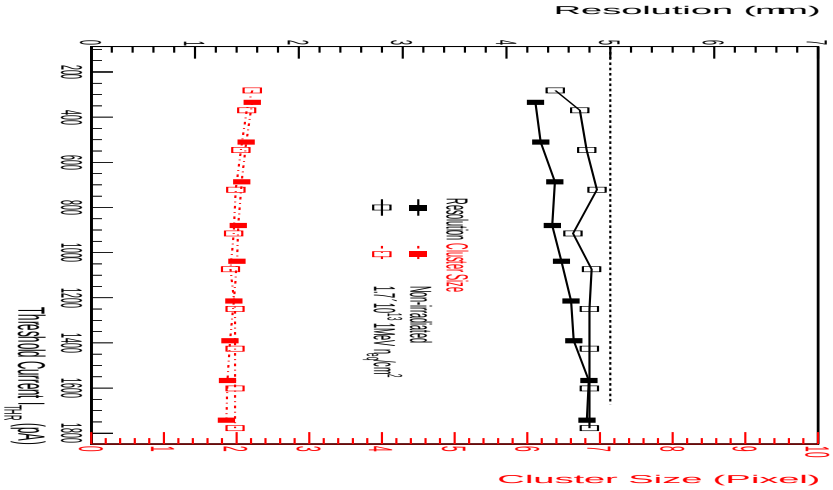
pALPIDE-2 - 2nd full-scale prototype (2015)



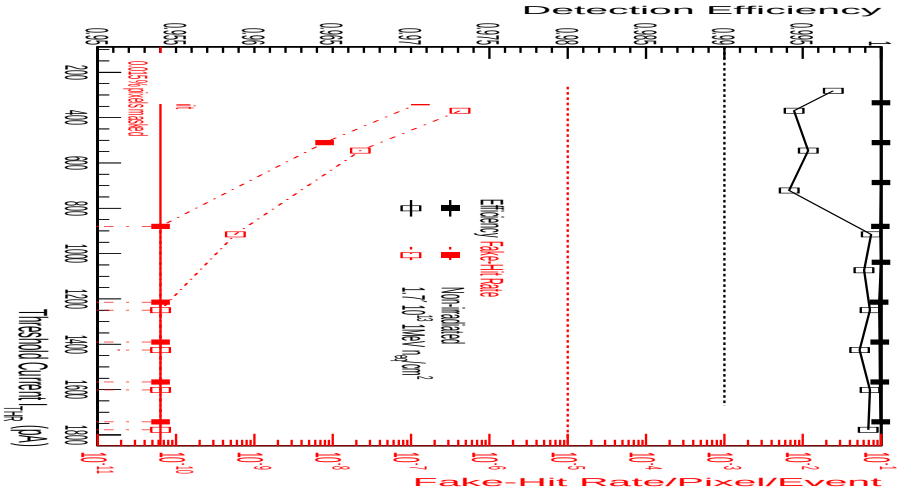
Test beam (7-plane telescope)



$\sigma_{det} \approx 5\ \mu m$



$\lambda_{fake} << 10^{-5}$/event/pixel @ $\varepsilon_{det} > 99\%$



Mass Production planned to start mid 2016

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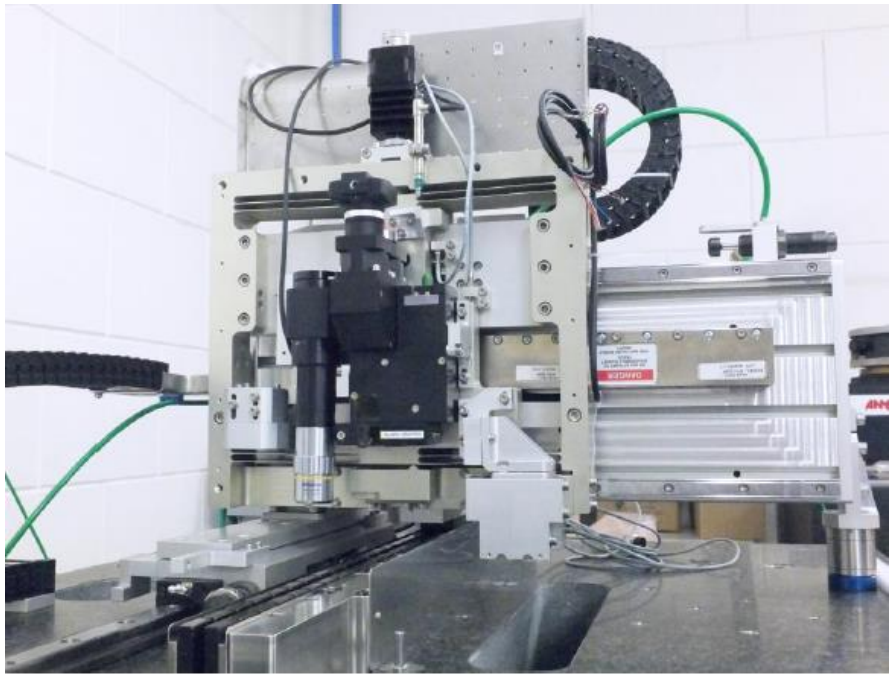
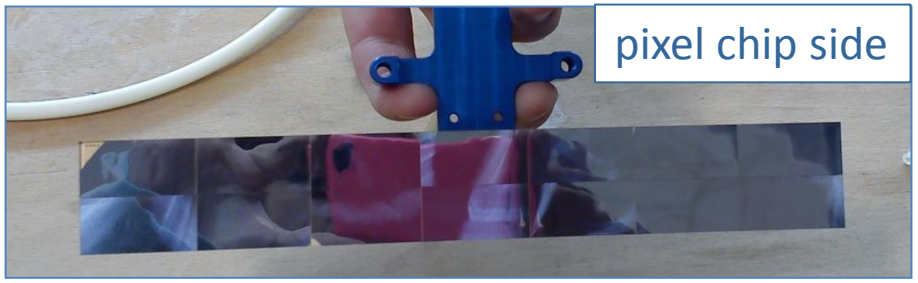
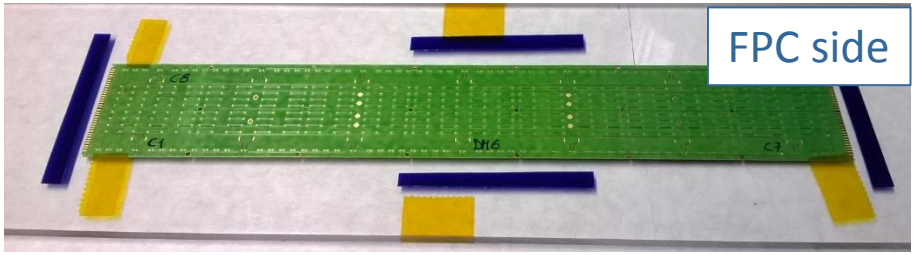
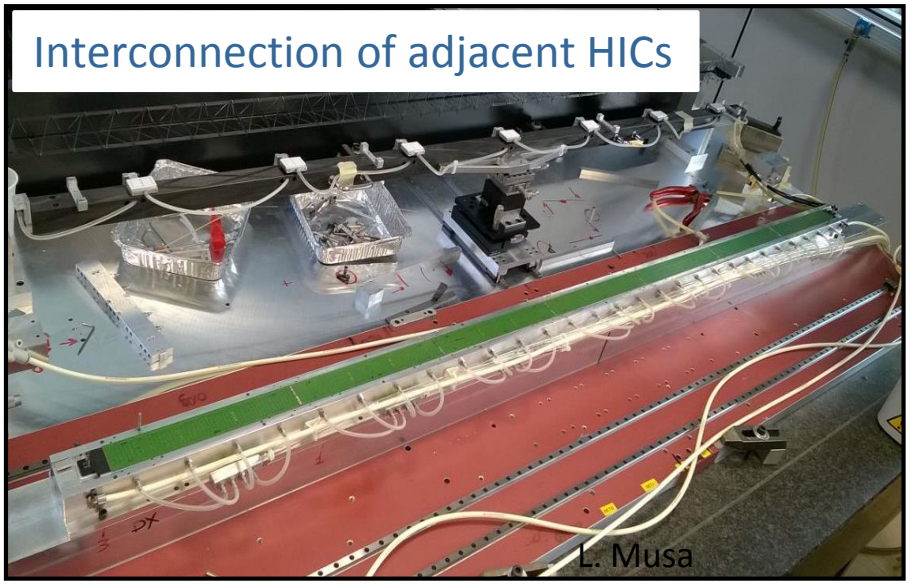
ITS Pixel Chip

Semi-automatic Module Assembly Machine



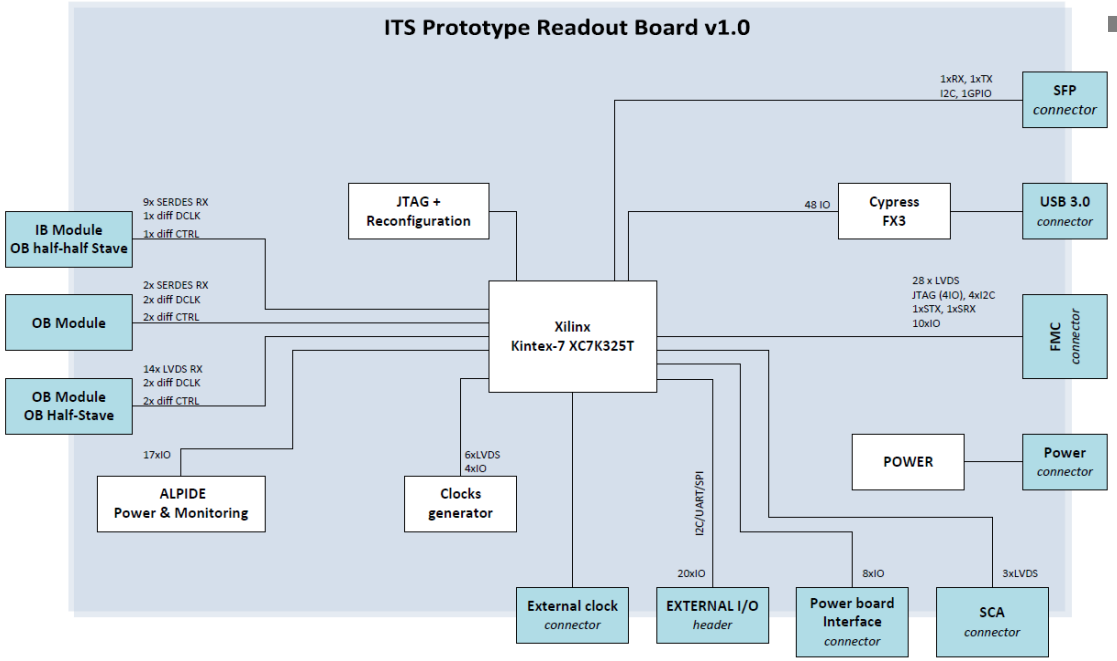


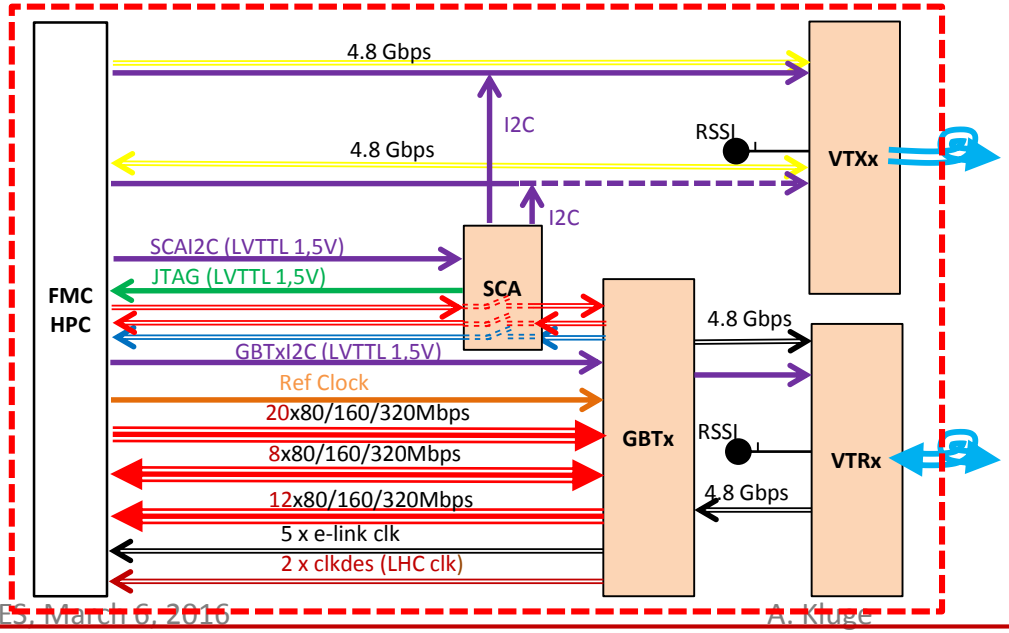


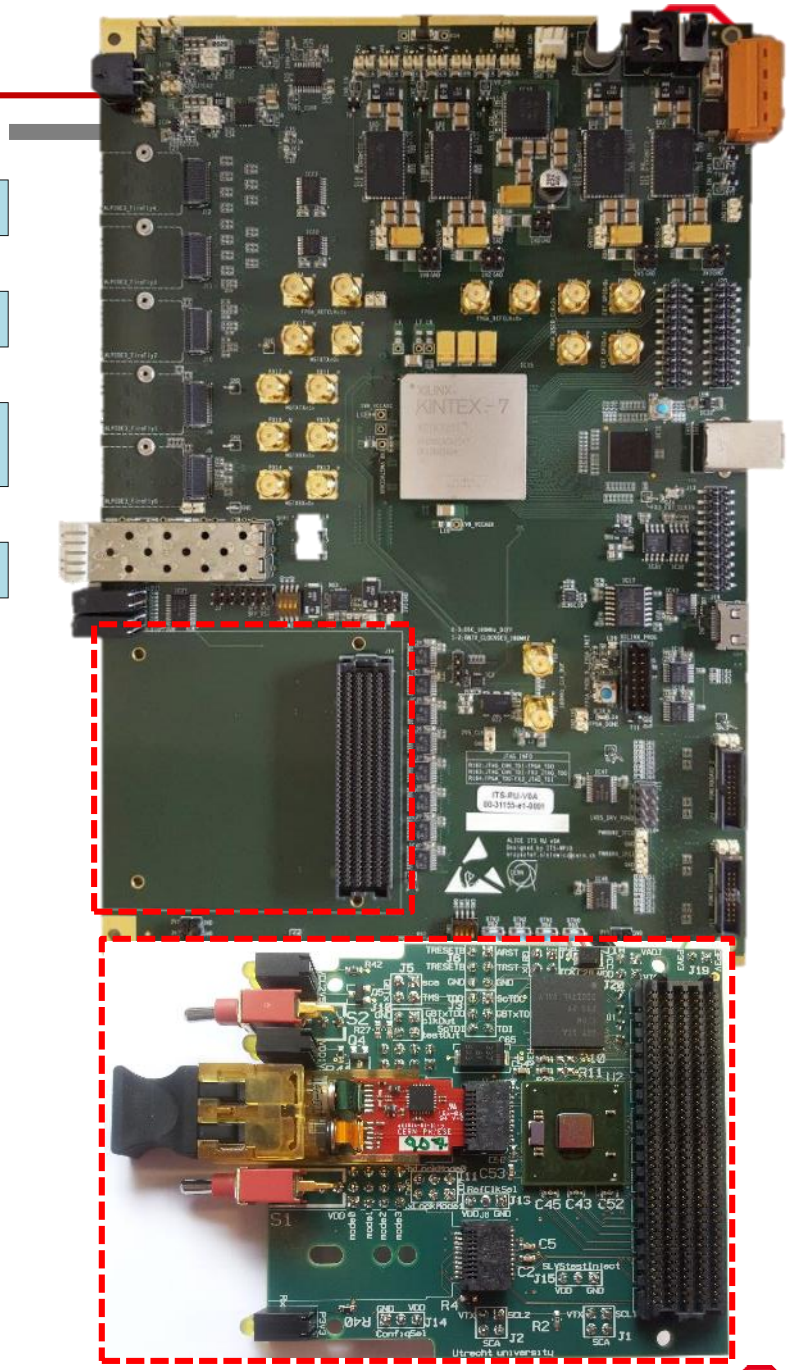


- Prototype is being tested at factory (IBS Precision Mechanics – Netherlands)
- Delivery at CERN: January 2016
- 5 more machines will be delivered in May – Aug 2016

ITS Readout Unit v0





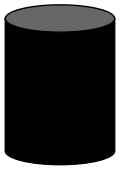


Interconnection of Pixel Chip to Flex PCB

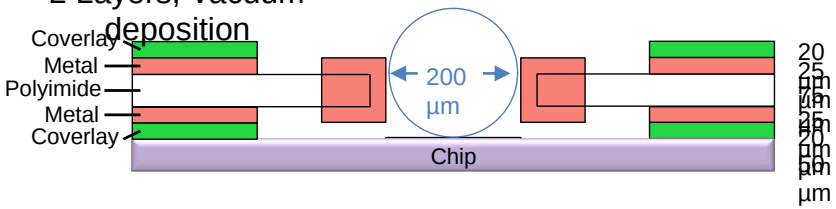
A Large Ion Collider Experiment

Selective Laser Soldering

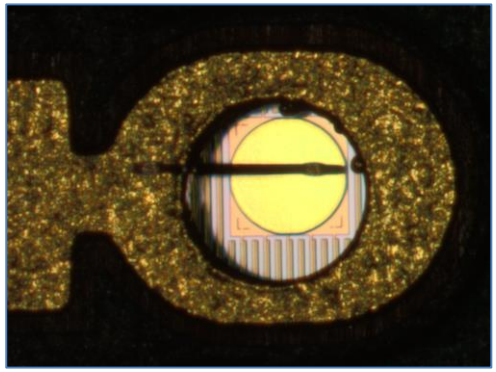
Laser soldering machine
(Dr. Mergenthaler GMBH

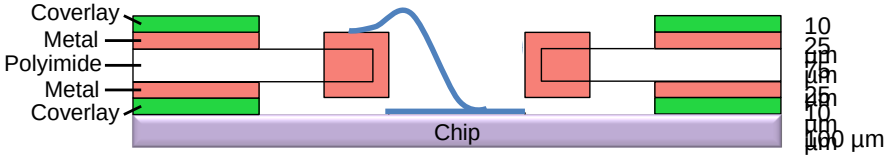


2 Layers, Vacuum deposition

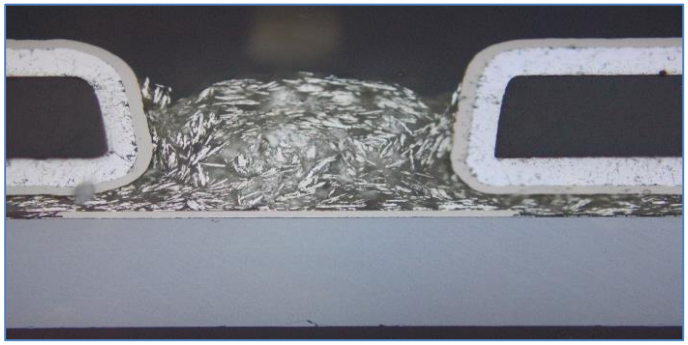


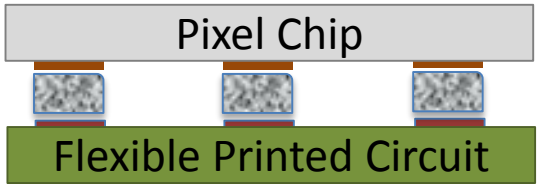
Wire bonding





Isotropic Conductive Adhesive





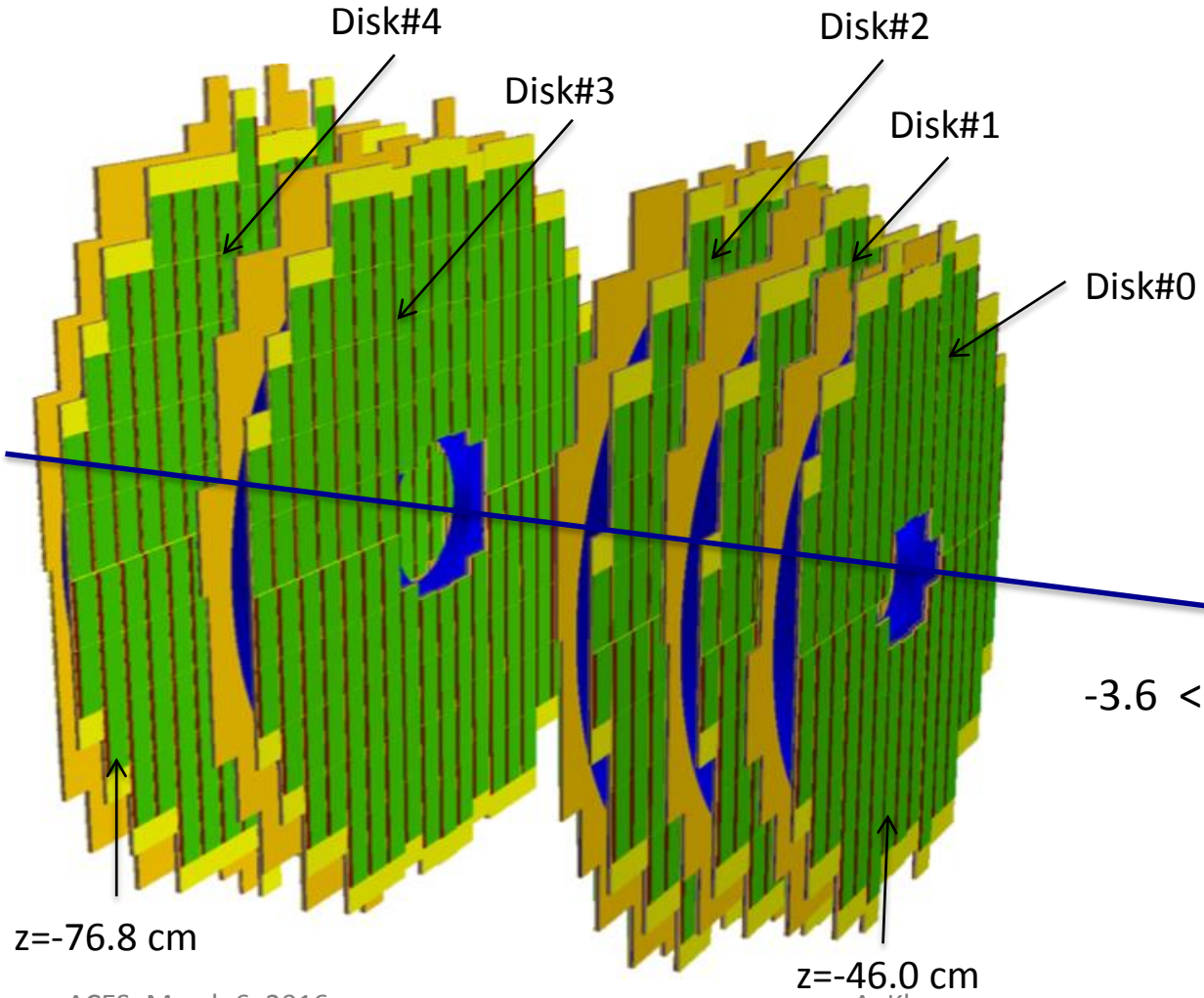
L. Musa

MFT – Muon Forward Tracker

Muon Forward Tracker

MFT Layout

896 silicon pixel sensors (0.4 m²) in 280 ladders of 1 to 5 sensors each.



10 Half-disks
2 detection planes each

MFT doses
< 400 krad
< 6×10^{12} 1 MeV n_{eq}/cm^2
10-fold security factor

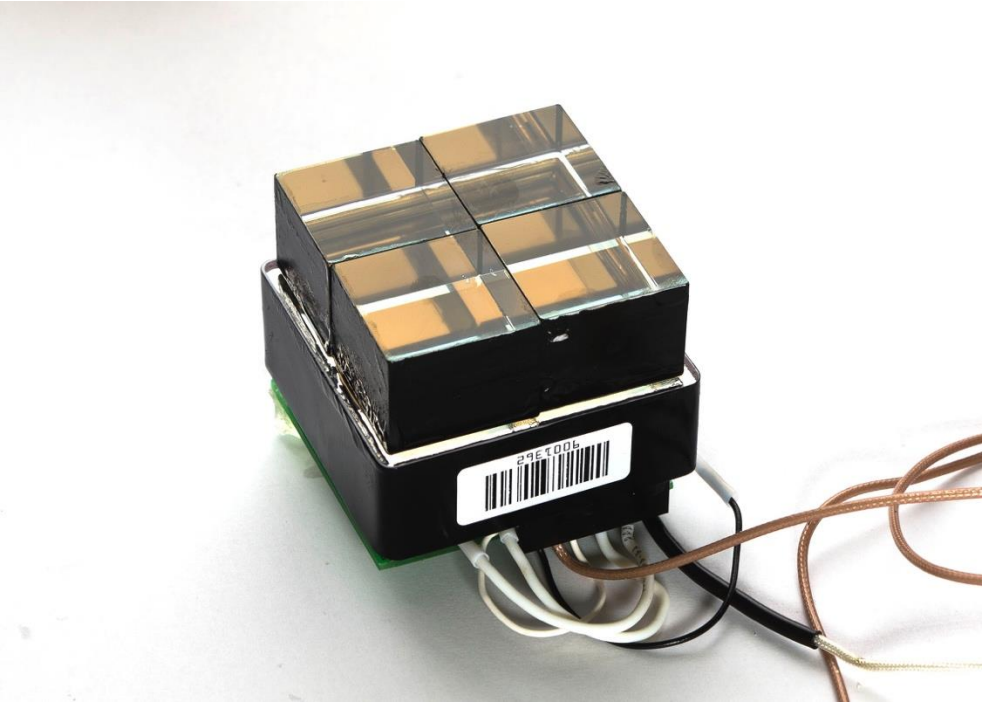
$-3.6 < \eta < -2.45$

IP region

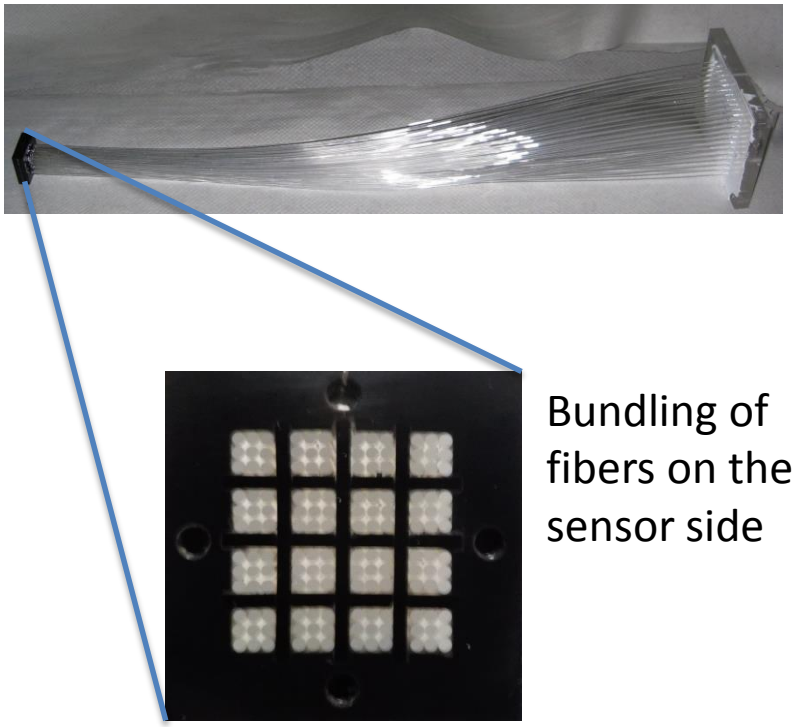
FIT – Fast interaction trigger

FIT-T0/V0

- **T0**



V0

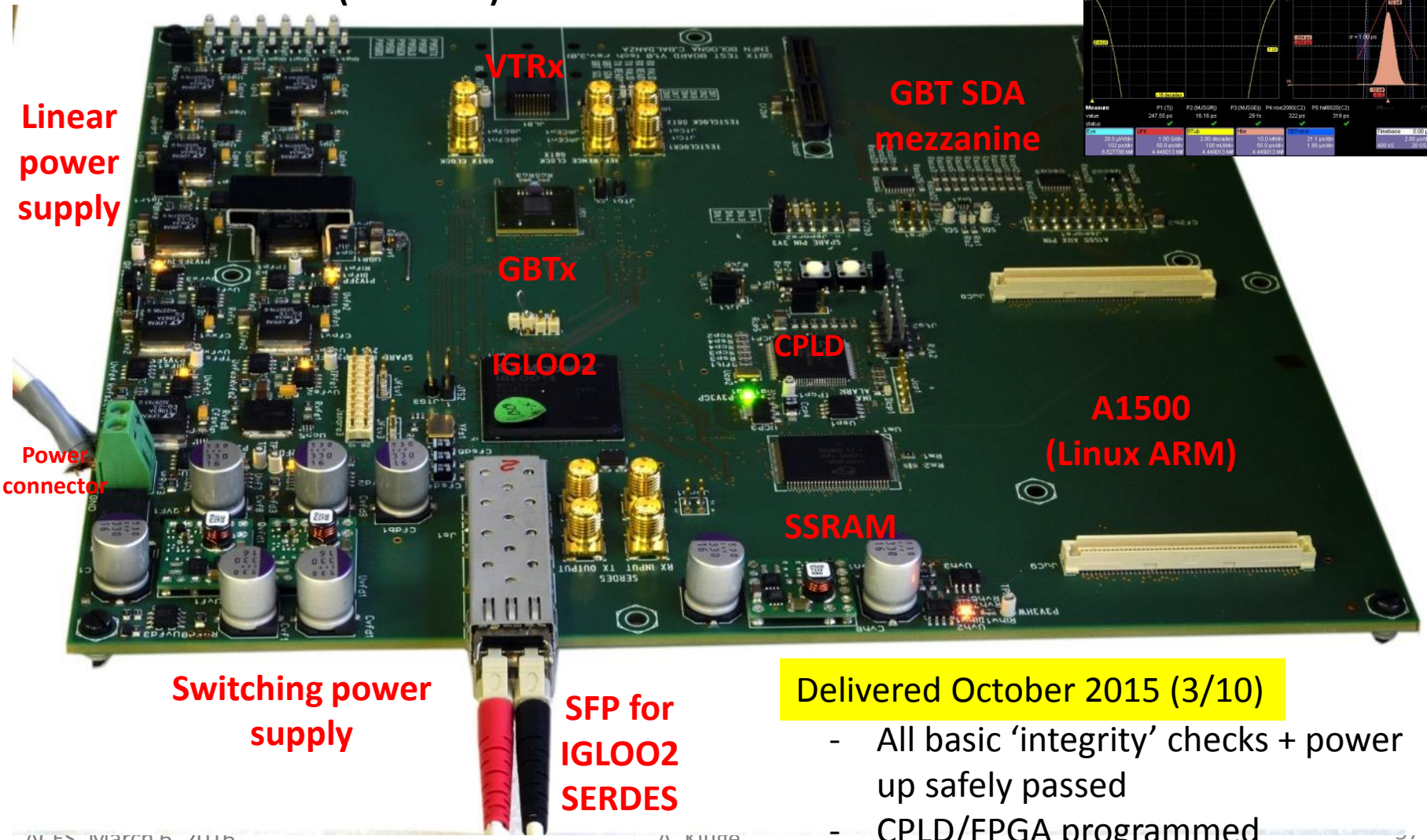


Bundling of fibers on the sensor side

TOF

TOF GBTX Test Board

Move to continuous readout (1 MHz pp)
Replacement of the readout card (DRM) in TOF VME crates (72 crates)



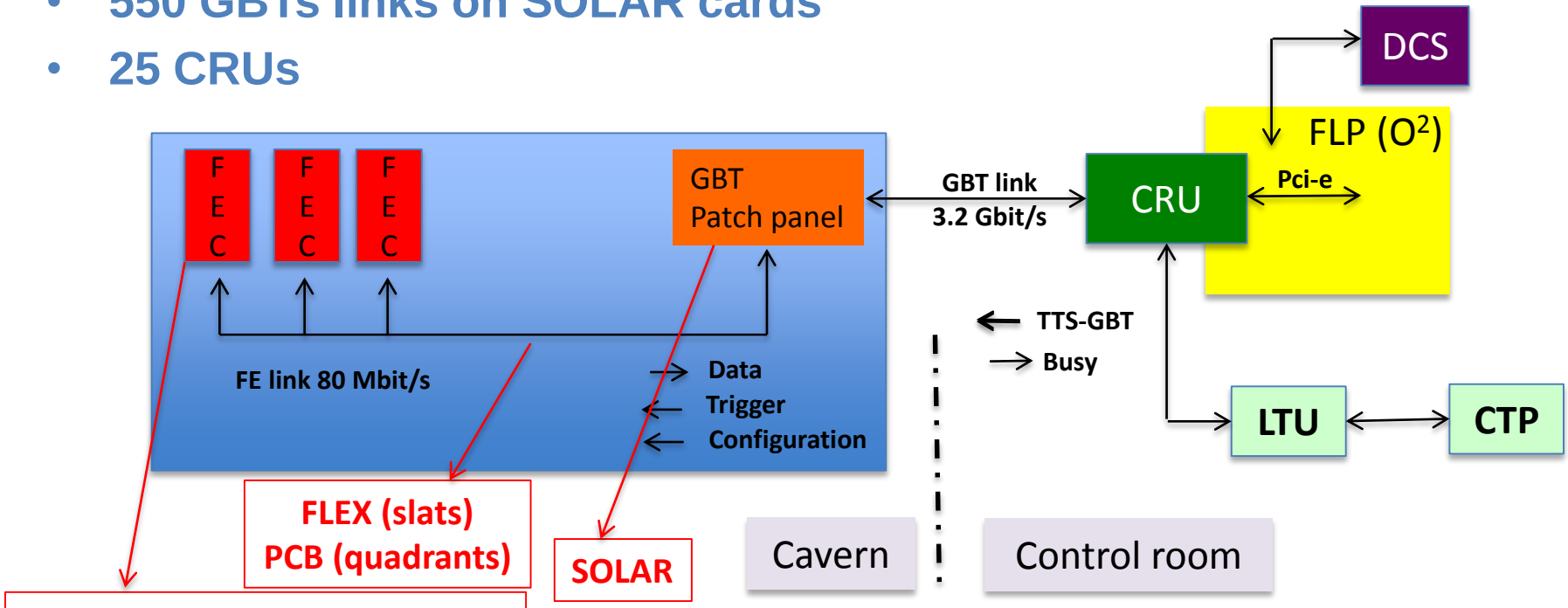
Delivered October 2015 (3/10)

- All basic 'integrity' checks + power up safely passed
- CPLD/FPGA programmed

MCH

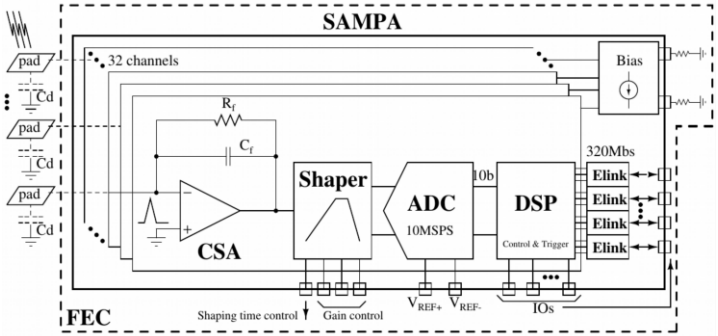
MCH

- 17.000 FE cards (64 ch.) with 2 SAMPA ASIC each=> 1M channels
- 34.000 SAMPA ASIC (32 ch.)
- 550 GBTs links on SOLAR cards
- 25 CRUs



1 FEC = 2 SAMPA = DualSAMPA

SAMPA = analog + digital



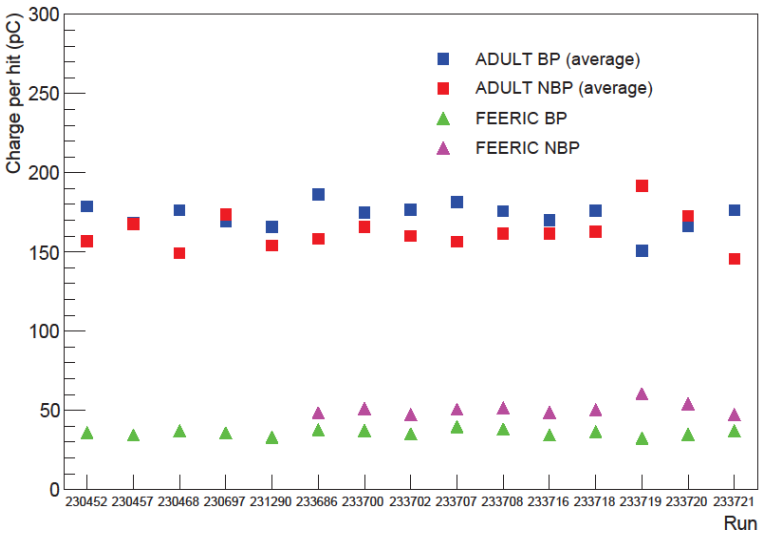
- FEC: Orsay
- FLEX: Cagliari
- GBT board: Saclay
- CRU: India

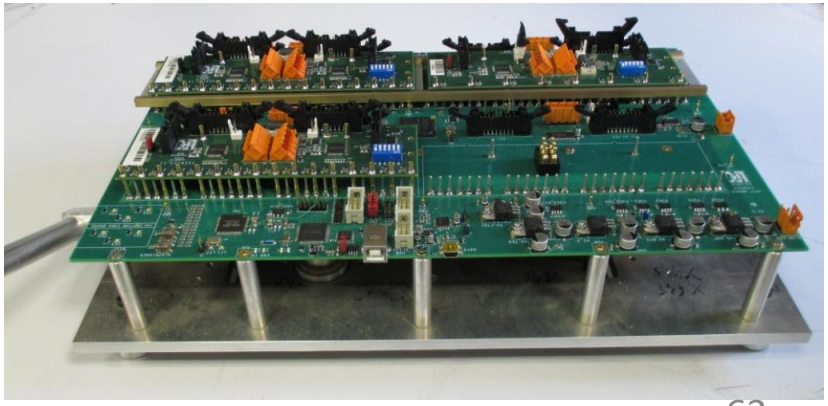
MID

P. Dupieux

MID: front-end

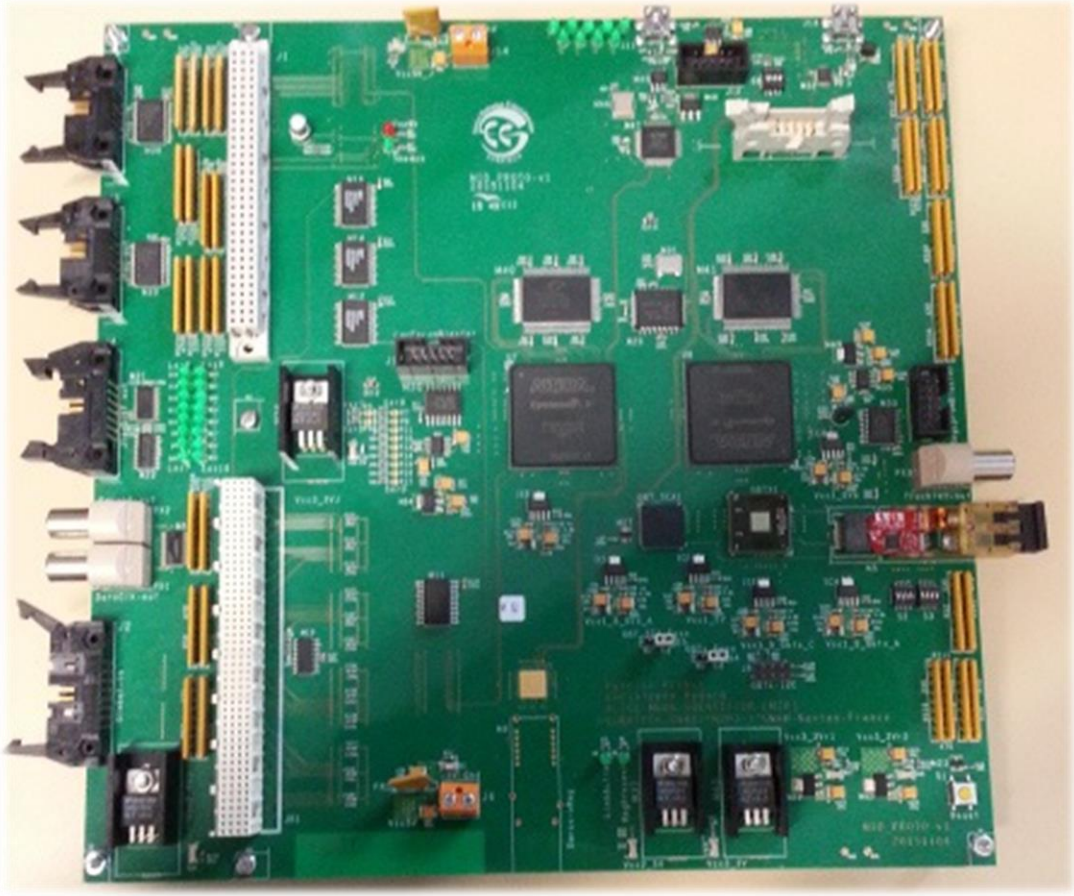
- Goal: slow down RPC aging after LS2
- 2384 FE cards (+spares)
  - Present ASIC ADULT: no amplification
  - Future ASIC FEERIC (0.35 µm CMOS) with amplification
- FEERIC card pre-series on 1 (/72) RPC in cavern since Feb. 2015
  - Very satisfactory performance and stability
  - Factor 4 less charge released in the RPC gas with FEERIC (right plot)=> reduced aging
- Production test bench ready
  - Up to 4 FEERIC cards tested in parallel
  - Test of ASIC-alone prod. (x4000) early 2016





MID: Read-out Electronics

- Continuous read-out
- Replacement of 234 LOCAL and 16 REGIONAL cards presently in operation
- Readout card prototype ready



Summary

- Large number of detector or read-out is replaced
  - ITS & TPC & MFT: new concepts
- Continuous read-out
- Common solutions adopted