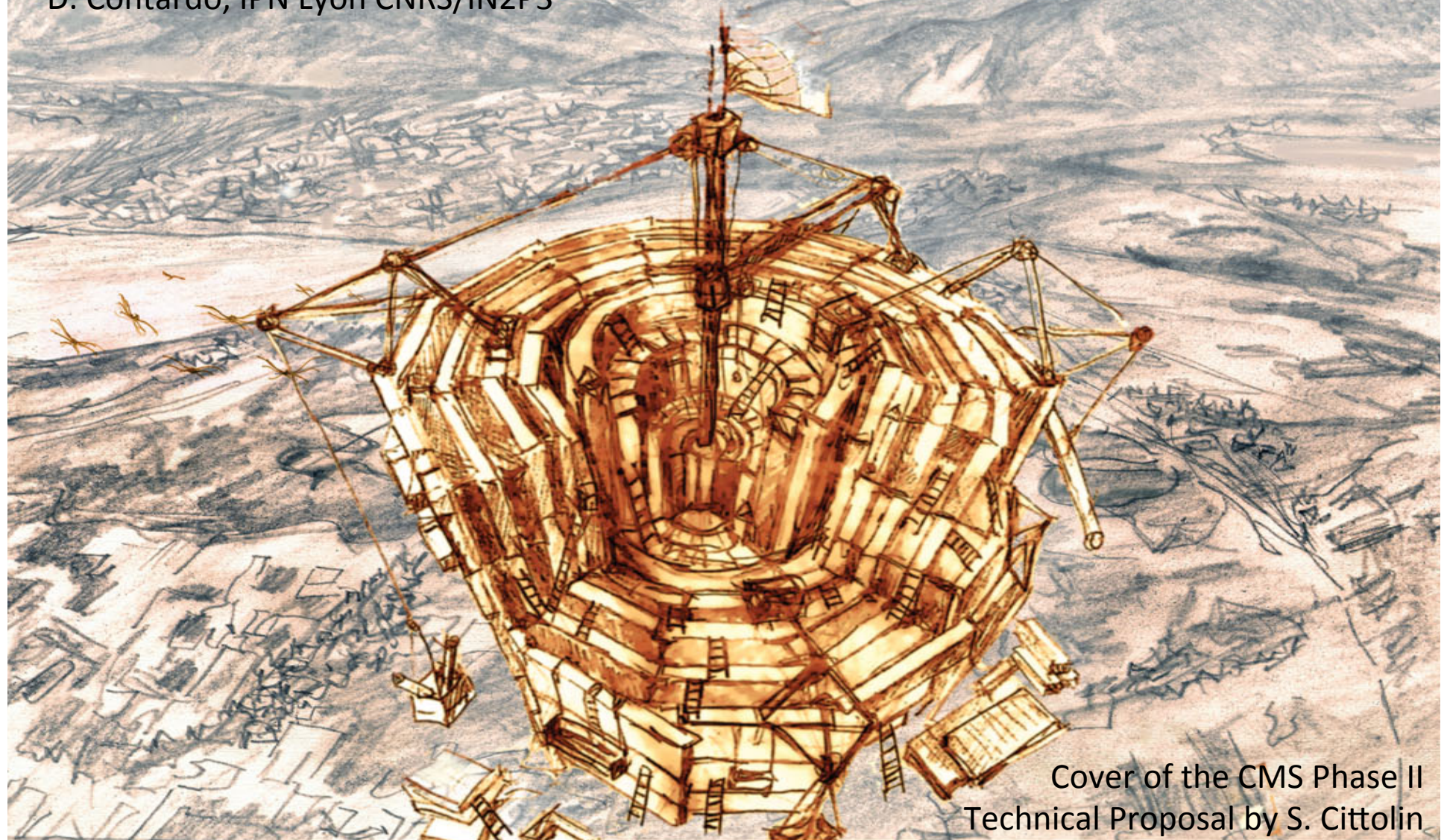


The CMS Phase-II Upgrade for the HL-LHC

ACES Workshop, Mar. 7, 2016

D. Contardo, IPN Lyon CNRS/IN2P3



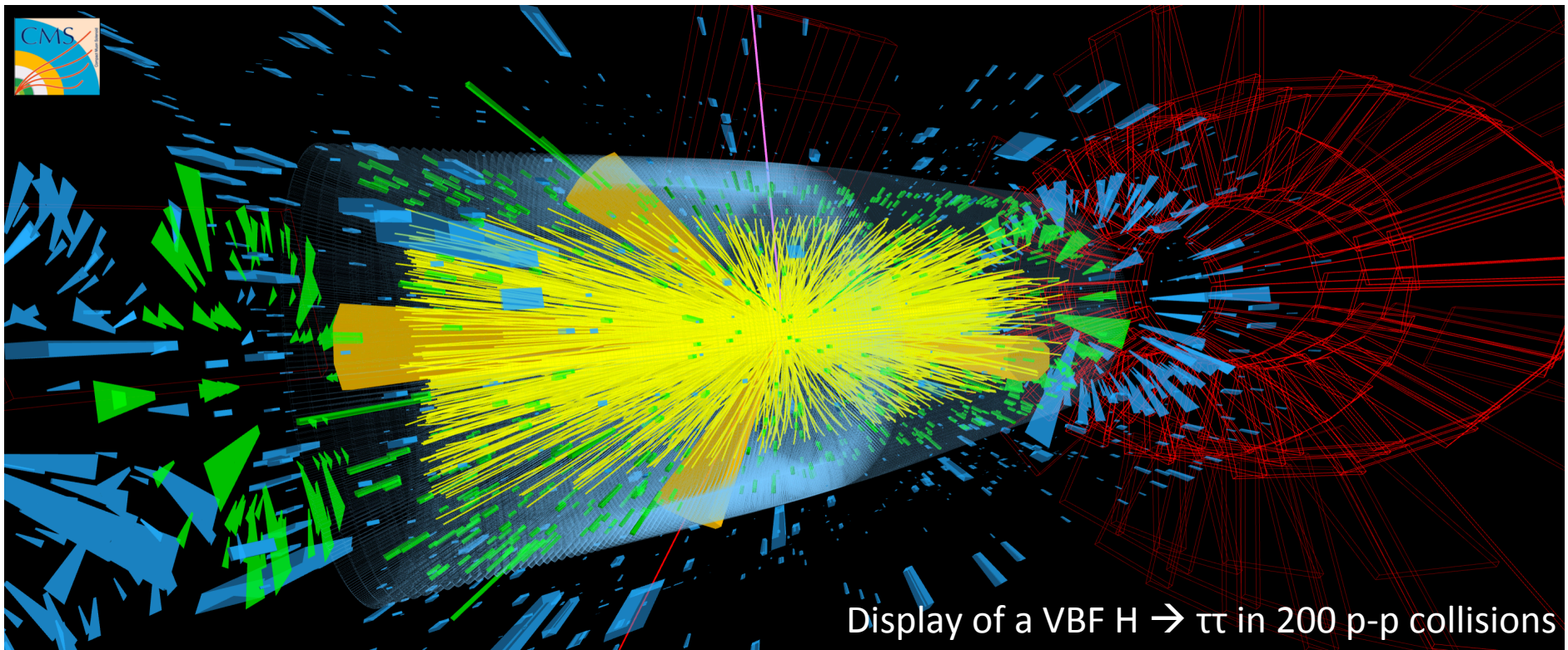
Cover of the CMS Phase II
Technical Proposal by S. Cittolin

Outline

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The CMS Phase II Upgrade will provide excellent physics performance with the challenging conditions at HL-LHC

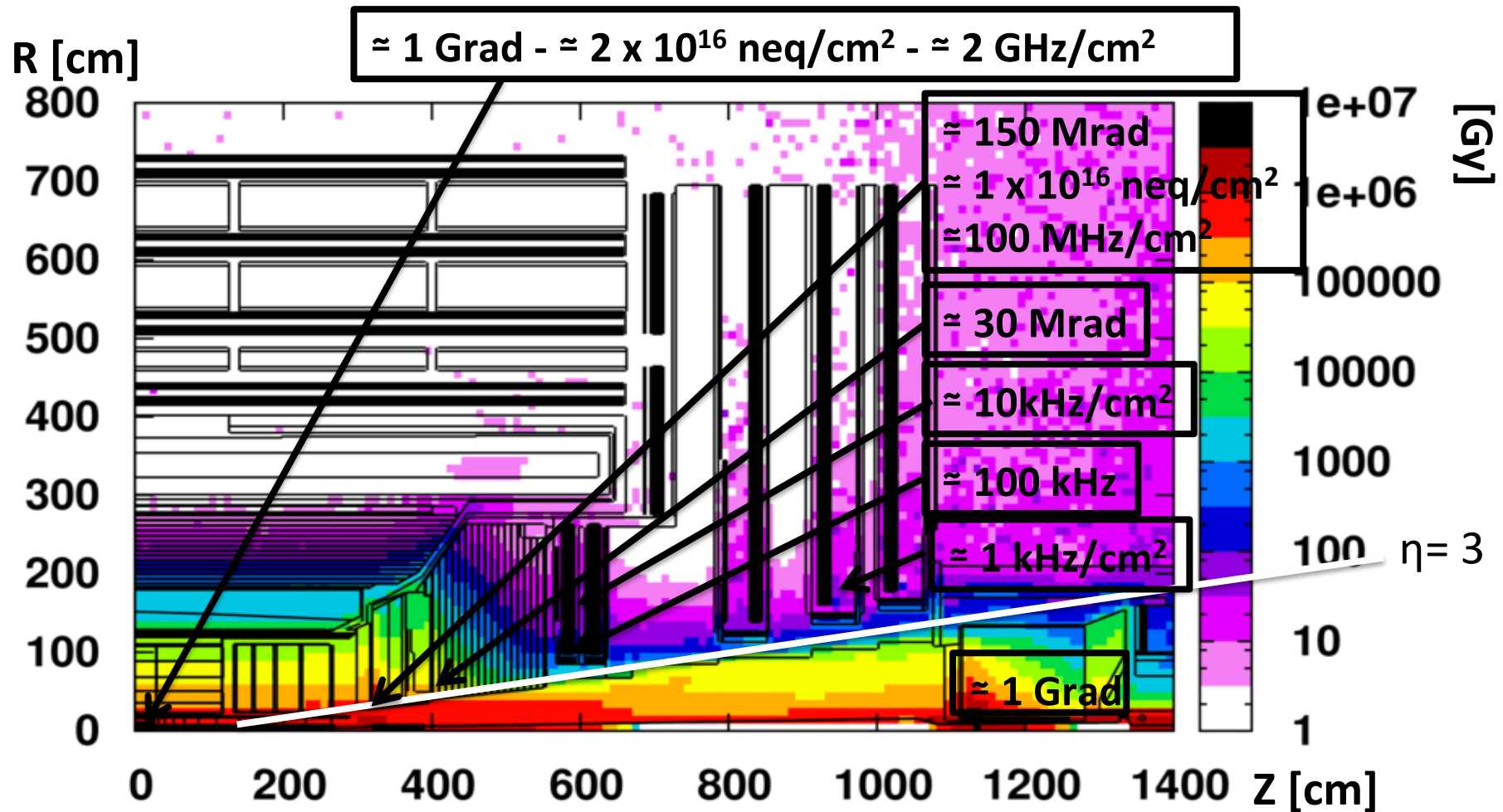
- Targeting operation up to $7.5 \cdot 10^{34}$ Hz/cm² instantaneous luminosity with leveling, a mean of ≈ 200 p-p collisions per bunch crossing



Physics requirements and performance are not discussed in this presentation, precision measurement and observation of very rare processes need at least maintaining current performance for all physics objects - above is an example of a representative physics channel

Two major motivations for the upgrades

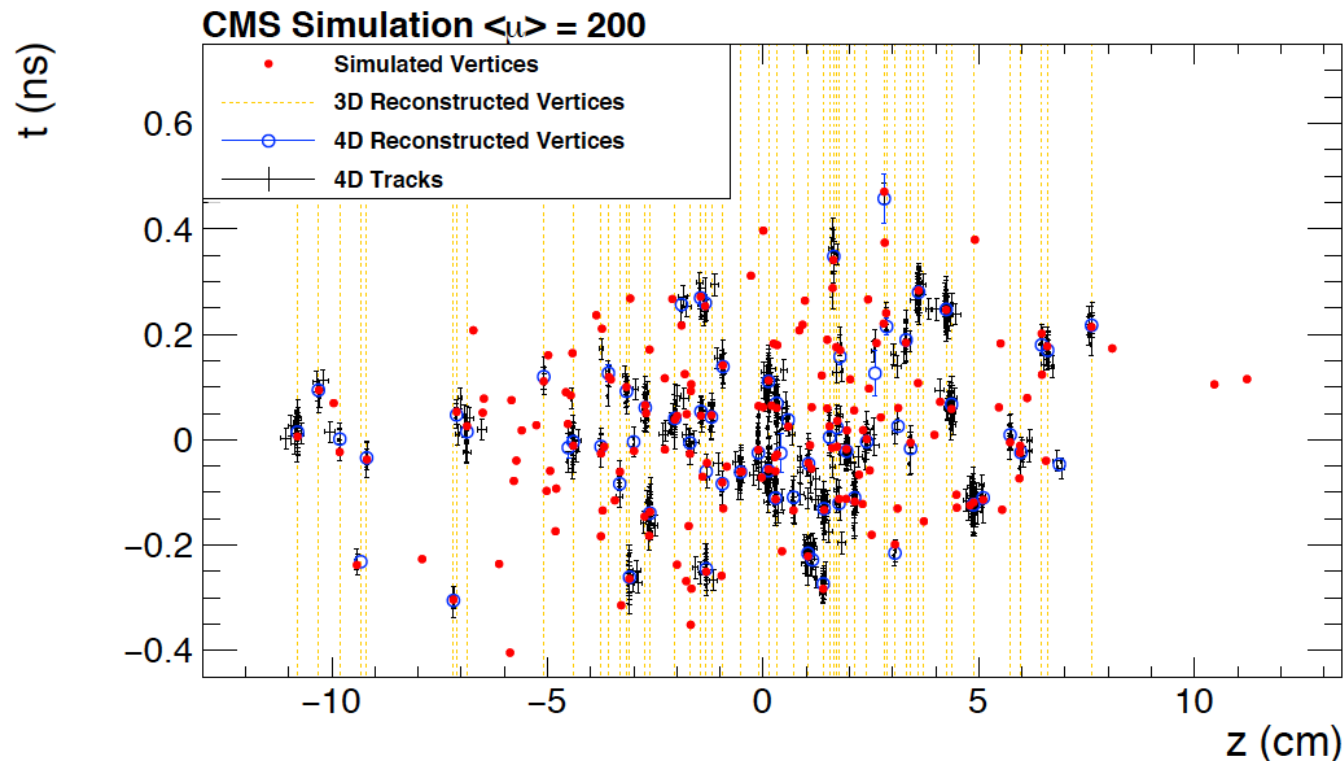
- Unprecedented radiation doses → replace Tracker and End cap Calorimeters and use new technics also for forward muon detectors
- Much higher data flows → replace most of the readout systems



CMS radiation dose map, neutron equivalent fluence and particle rates for luminosities of 3000 fb^{-1} (integrated) and $5 \times 10^{34} \text{ Hz/cm}^2$ (instantaneous)

The pileup challenge

High granularity is needed to mitigate pileup effects to select events with a hard scatter process at L1-Trigger (hardware), and to identify the associated vertex and particles - Tracker is crucial, but also full granularity/precision of other detectors (at L1-Trigger) - further mitigation of pileup effects can be obtained with precise timing



Example of the space-time structure of simulated and reconstructed vertices in a 200 pileup event for the baseline HL-LHC luminous region scenario, 3D reconstruction uses the CMS tracker upgrade with track-coordinates only and 4D augments this with a dedicated timing layer that provides a single timing measurement with precision of 20 ps (L. Gray's presentation)

Challenges for electronic systems

Reading out full data or largest possible sub-set at 40 MHz (for L1-Trigger) and minimizing the power consumption (due to increased granularity...) applies to almost all systems and as implications for electronics systems:

- Front-End designs with binary or digitized output, and data compression
- Low power consumption - example: 130 nm and 65 nm ASICs
- High inter-connection capabilities (bump-bonding, flip-chip, TSV)
- Data transfer with Optical Links in all detectors, and also with electrical links where radiation levels are too high or services must be farther to detectors
- DC/DC or Serial powering schemes, minimizing cabling/cooling material
- And radiation tolerance is needed for all on-detector systems
- Large processing power and bandwidth for data treatment in off-detector electronics
- High timing precision of clock and trigger distribution, to benefit from improved calorimeter timing precision, and possibly of other dedicated measurements

CMS Phase-II upgrades

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Trigger/HLT/DAQ

- Track information in Trigger (hardware)
- Trigger latency $12.5 \mu\text{s}$ - output rate 750 kHz
- HLT output 7.5 kHz

Barrel EM calorimeter

- New FE/BE electronics with improved time resolution
- Lower operating temperature (8°)

Muon systems

- New DT & CSC FE/BE electronics
- Complete RPC coverage $1.6 < \eta < 2.4$
- Muon tagging $2.4 < \eta < 3$

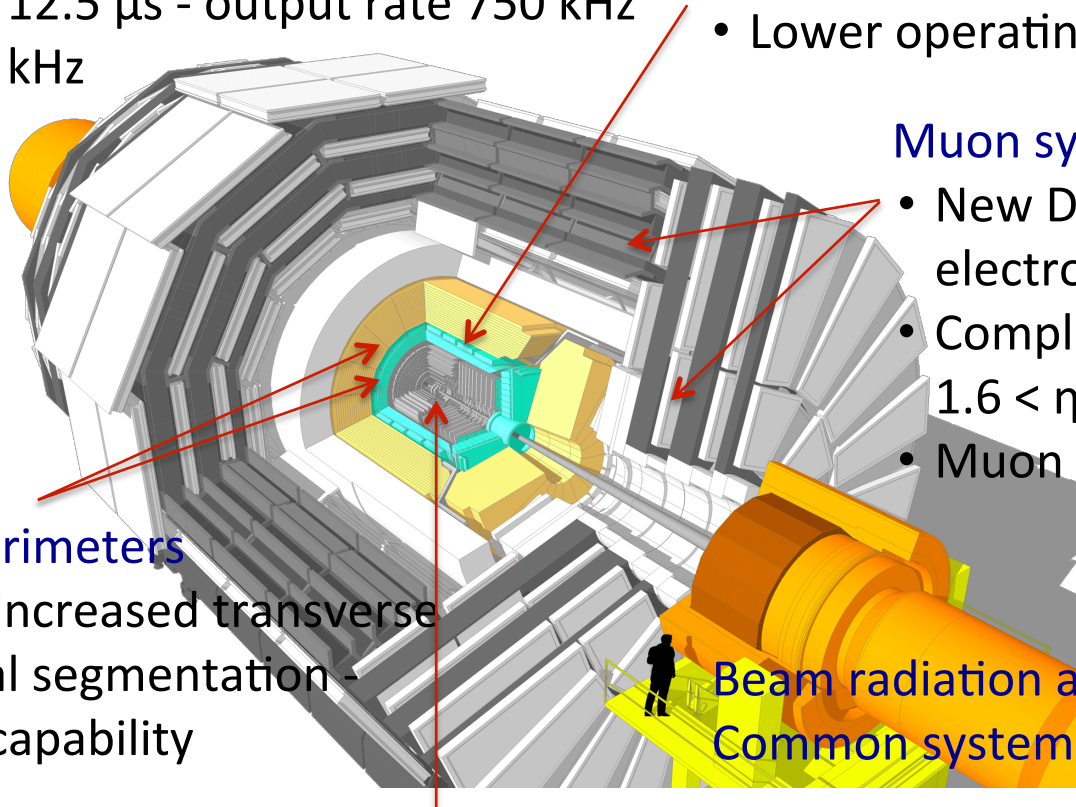
New Endcap Calorimeters

- Rad. tolerant - increased transverse and longitudinal segmentation - precise timing capability

Beam radiation and luminosity
Common systems and infrastructure

New Tracker

- Rad. tolerant - increased granularity - lighter
- 40 MHz selective readout in Outer Tracker for Trigger
- Extended coverage to $\eta \approx 3.8$



CMS Upgrade planning

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Upgrade motivations and performance of the conceptual designs are demonstrated in the Technical Proposal* and a Scope Document** (for variants of the detectors)

At the RRB of Oct. 2015 experiments were encouraged to proceed with preparation of Technical Design Reports, planning for CMS TDRs is:

- Jun. 2017 : Tracker TDR
- Sept. 2017: Barrel Calorimeters TDR - Muons systems TDR
- Nov. 2017 : Endcap Calorimeters TDR
- Trigger, DAQ and BRIL TDRs foreseen in 2019-2020

TDRs must contain sufficient progress in demonstrating upgrade feasibility through studies and R&D with demonstrator validations or tested prototypes

Presentation of detector and physics benchmarks performance

Well understood schedules, costs and resources and estimations of the risks and possible mitigations

Beyond TDRs, 3rd step of approval will be for construction, following Engineering Design Reviews, it is foreseen to start production by 2019 for major systems

* Tech. Prop. for the Phase II Upgrade of CMS CERN-LHCC-2015-010 <https://cds.cern.ch/record/2020886>

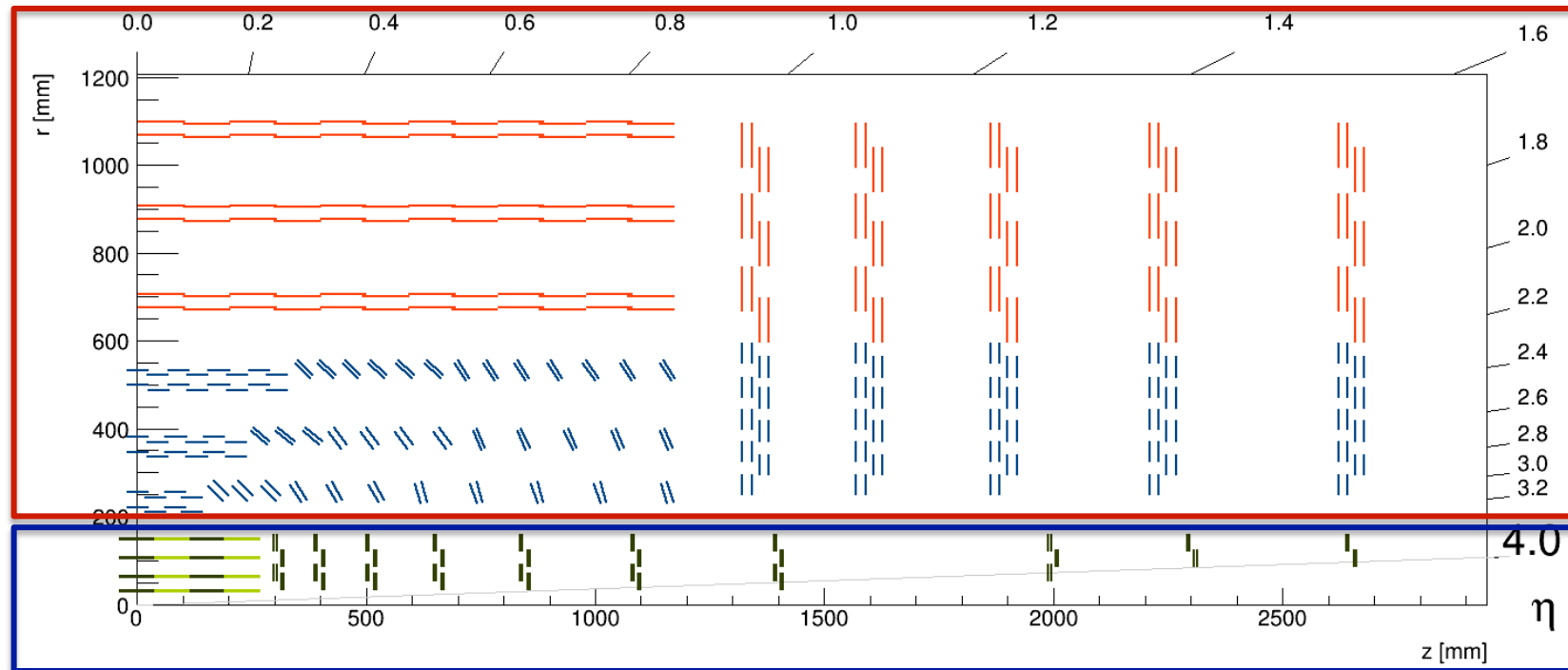
* CMS Phase II Upgrade Scope Document CERN-LHCC-2015-019 <https://cds.cern.ch/record/2055167/files/LHCC-G-165.pdf>

Tracker

Tracker design

Outer Tracker - 6(5) layers(disks) - 2 sensor modules for trigger purpose

220 m² silicon sensors \approx 200 μ m active or physical thickness - 15500 modules - 50M strips - 220M macro-pixels - 90/100 μ m pitch - 2.5/5 cm strips - 1.5 mm macro-pixels in inner layers



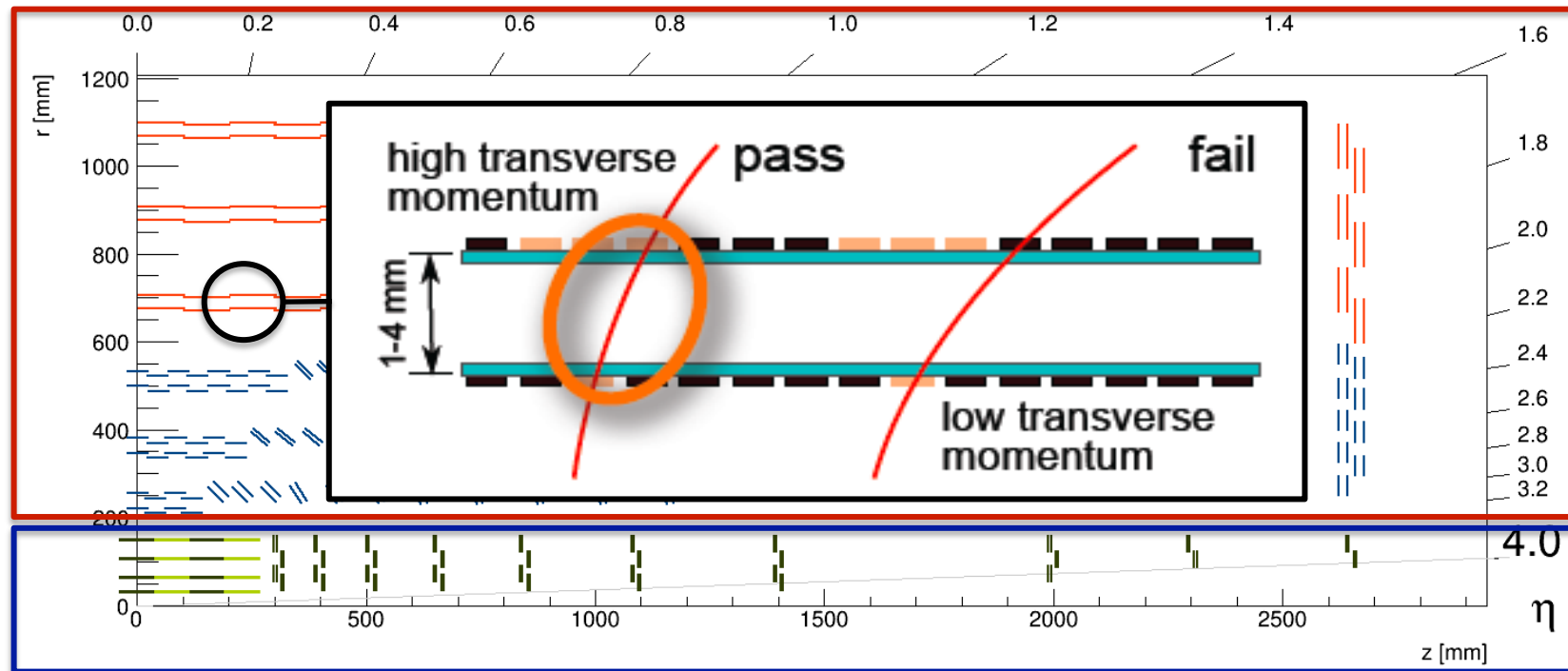
Pixel detector - 4 layers at 3/7/11/16 cm with coverage up to $\eta = 3.8$ with 10 disks
 4 m² silicon sensors \leq 150 μ m physical thickness - 50x50 to 25x100 μ m² pixels optimization for performance

(S. Mersi's presentation)

Tracker design

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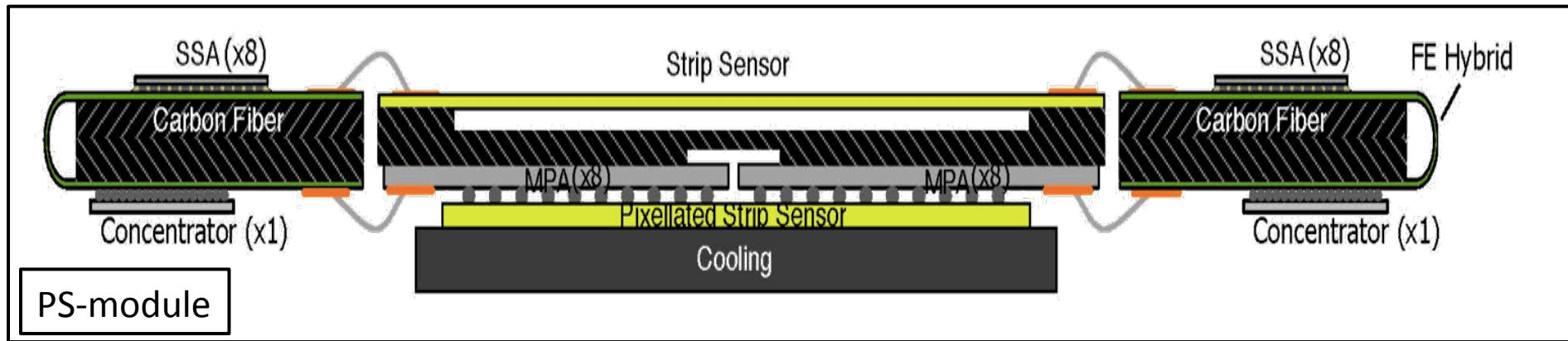
OT modules with 2 sensors spaced by few mm and readout by the same ASIC Chip measure bending of particles in high B-field and transfer hits for tracks with $P_t \gtrsim 2$ GeV at 40 MHz, track reconstruction in Back-End electronics for L1-Trigger



- Requires low-power GBT with high bandwidth to overcome performance limitations in trigger and data transfer for inner layers
- BE electronics: Associative Memories + FPGA or FPGAs only with two schemes for algorithms & cabling - requires high processing power & bandwidth, short latency for trigger object formation - demonstrators are becoming available (K. Hahn's presentation)

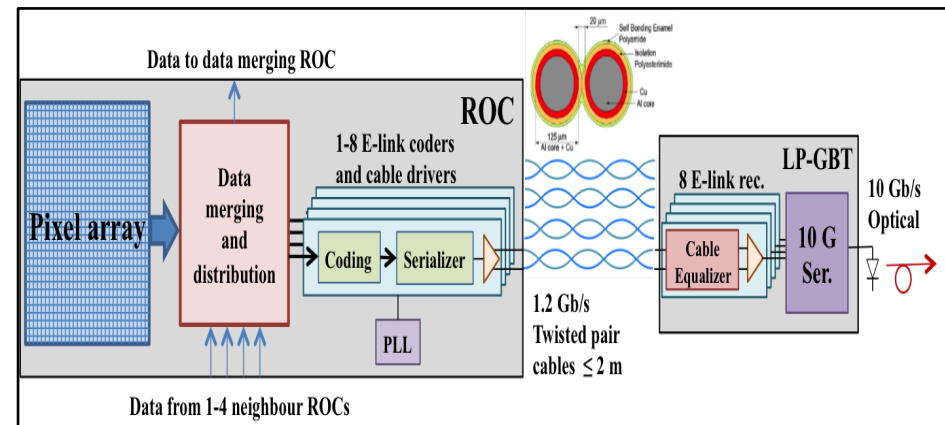
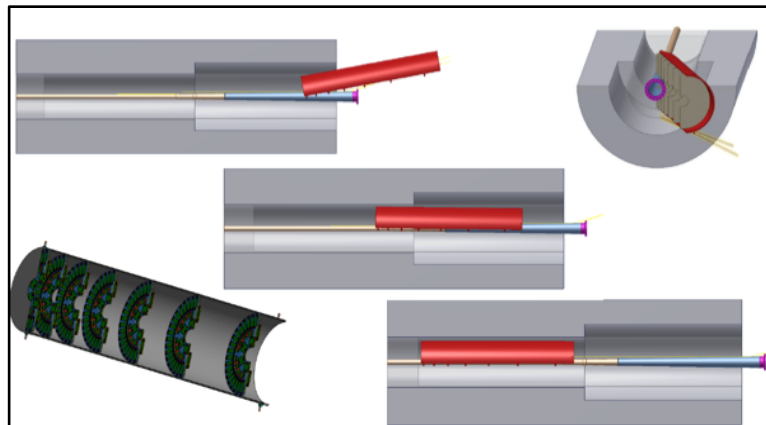
Light module & mechanical designs - CO₂ cooling (-30°) - DC/DC powering

→ Weight divided by 2 and 2 to 3 x less photon conversions compared to current tracker



- **Sensors of n-in-p type** - recently good quality n-in-p sensors produced also at INFINEON, on 8" wafers with 200 μm thickness
- **FE ASIC prototypes** available (at different stages) in 130 nm and 65 nm
- **Flex hybrid prototypes** validated for FE - investigating 2nd vendor
- **Flip-chip connection** for pixelated sensors validated at three companies
- **First power chain** demonstrator operated successfully, developing new DC/DC scheme with 3 voltages

- Radiation conditions are the most severe for sensors and readout electronics and the particle rates are the highest
- Light detector is crucial for precise measurement of track impact parameter to mitigate pileup effects



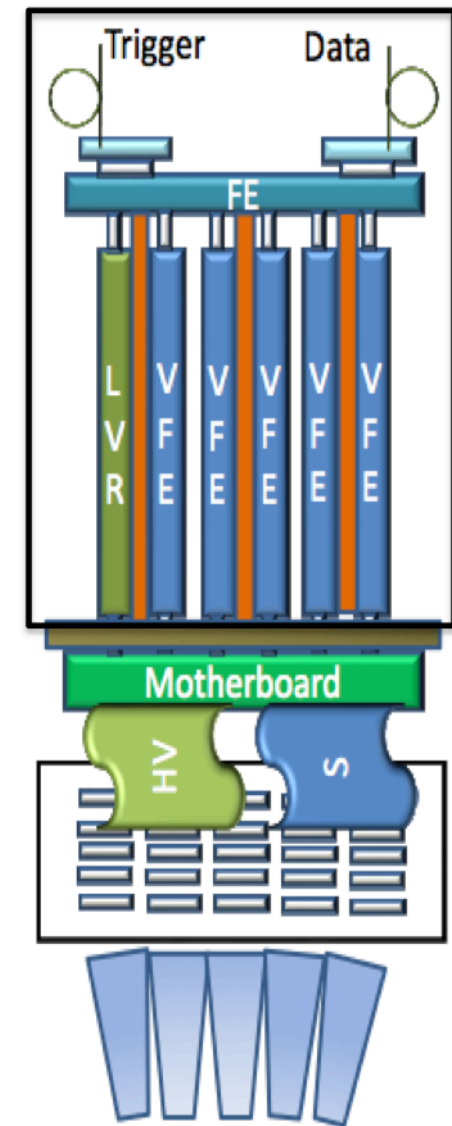
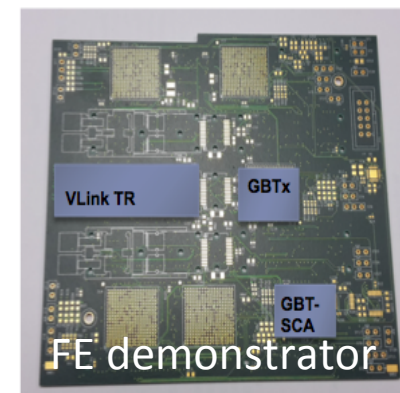
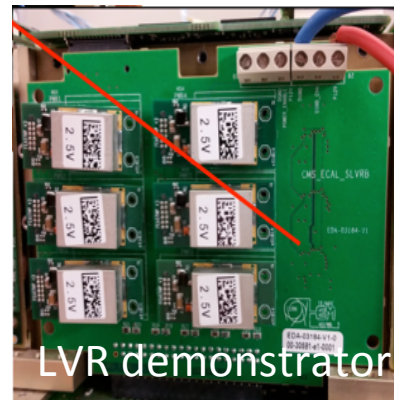
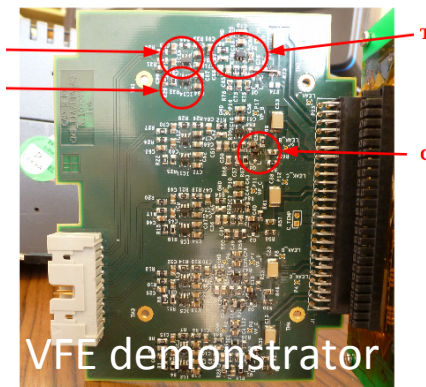
- Design being developed, particularly forward extension, interface to OT and integration
- Sensor HV isolation is being investigated for planar technology, 3D remains an option for the innermost layer - several submissions on-going or planned
- It is important to develop RD53A ASIC on schedule for TDRs and to validate the radiation tolerance with the common digital test chip
- Light electrical links with high bandwidth and serial powering are crucial to reduce cabling and amount of material

Calorimeters

Barrel Electromagnetic Calorimeter upgrade

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- **Very Front-End** pre-amplifier and ADC to mitigate noise/background effects & to improve time resolution
- **Front-End** with GBT at 10 Gbps for data transfer of crystal information at 40 MHz
- **LV boards** implementing DC/DC conversion
- **Operation at 8°** - mitigate radiation aging of APD (noise)



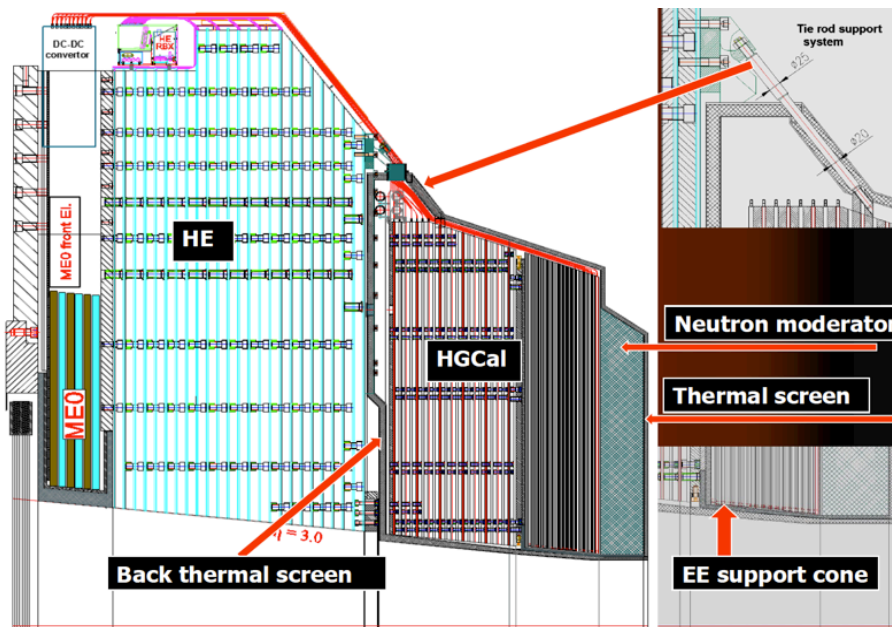
- VFE simulations of options are on-going
- Demonstrator boards for: VFE (with discrete components), FE with 5Gbps GBT and LV with DC/DC FEAST are ready for test
- Preliminary test beam results indicate that ~ 30 ps resolution with crystal + APDs could be reached at $E \gtrsim 30$ GeV

(M. Dejardin's presentation)

Endcap Calorimeter design

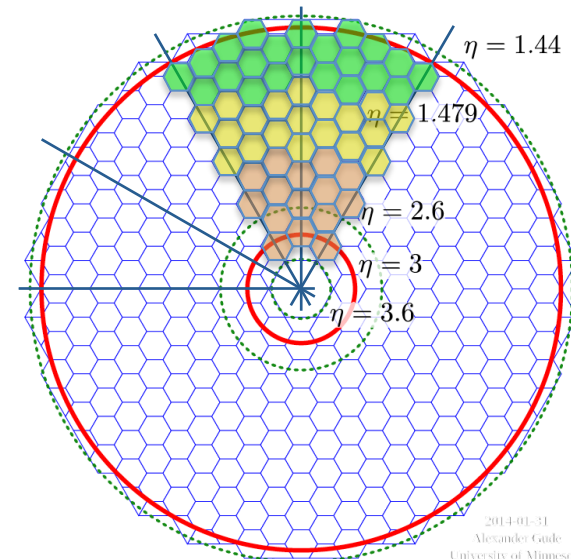
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- High Granularity Calorimeter with 4D (space-time) shower measurement
 - Electromagnetic section ($26 X_0$, 1.5λ): 28 layers of Silicon-W/Cu absorber
 - Front Hadronic section (3.5λ): 12 layers of Silicon/Brass or Stainless Steel
- Back Hadronic Calo. (BH) similar as present HE - radiation tol. - granularity $\approx x4$
 - BH (5λ): 12 layers of Scintillator/Brass or Stainless Steel (2 depths readout)



EE: 380 m² - 4.3 Mch - 13.9k modules - 16t
FH: 209 m² - 1.8 Mch - 7.6k modules - 36.5t
BH: 428 m² - 5184 SiPMs

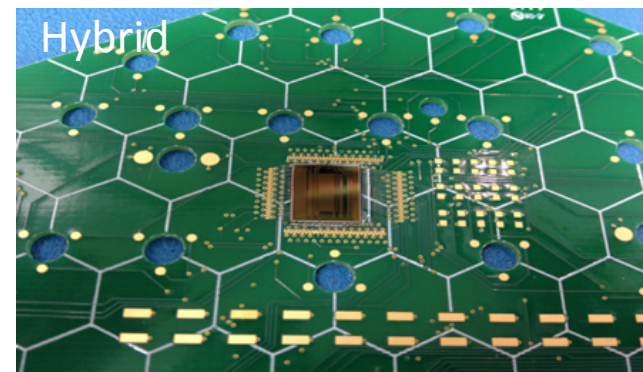
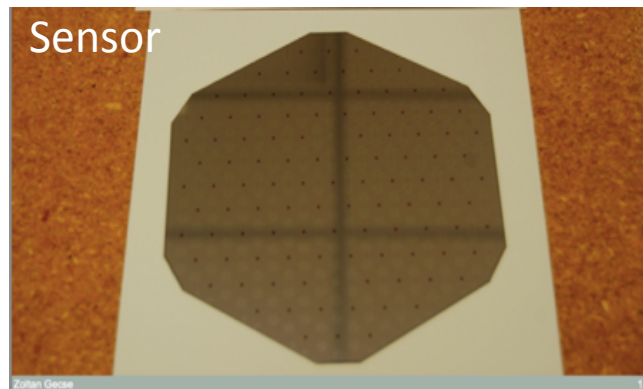
3 sensor active thicknesses 100-200-300 μm
 0.5(1) cm² pads for 100(200/300) μm



(M. Mannelli's presentation)

Endcap Calorimeter R&D

- **Si-sensors:** very good quality 6" p-in-n 128 pads received, multiple geometries & other designs 6" p-in-n 256 pads & 8" n-in-p 128 pads orders proceeding (HPK/Infineon/Novati)
- **Initial test beam:** SKIROC2-CMS (bi-polar, short shaping, fast timing, ToT) submitted,
- **Final ASIC:** 130 nm design - several options evaluated - test blocks mid-Mar. & first version Q1 2017
- **Test beams:** EE proto at FNAL (summer 2016) and EE + FH at CERN (fall 2016)
- **Measured time resolution:** ≈ 20 ps with 10 MIP signal in a single non irradiated pad
- **Radiation hard scintillating devices**

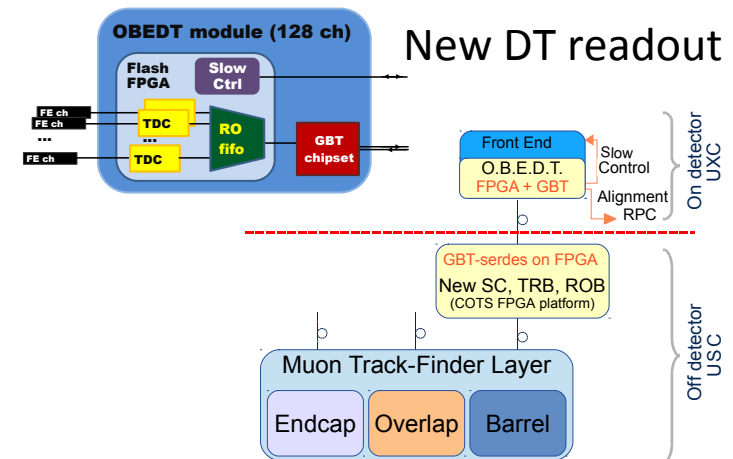
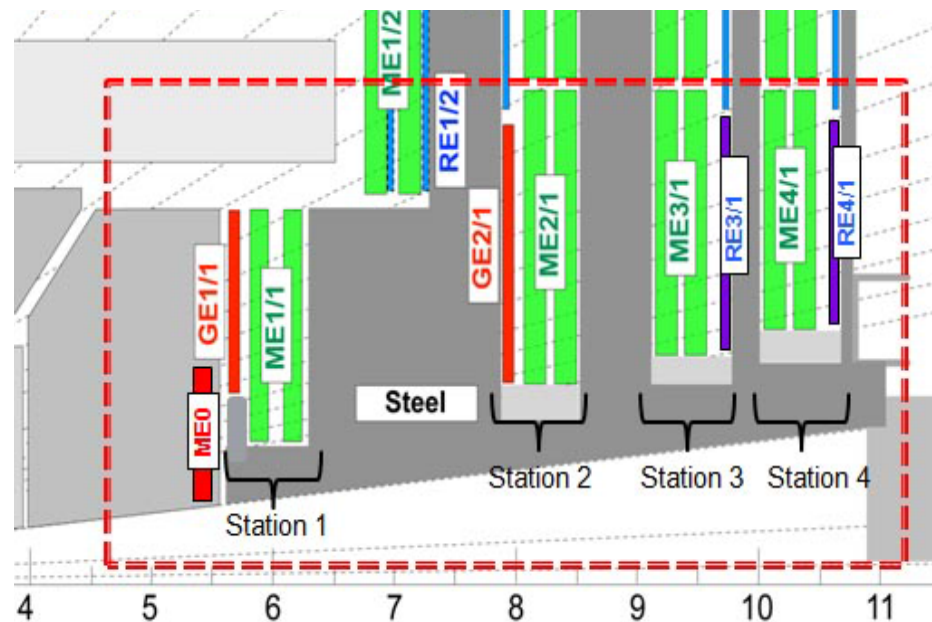


- Requires high bandwidth 10 Gbps for optical readout and also high speed electrical links for inner region of the detector - investigating options for full readout at 40 MHz
- DC/DC powering with new 3 voltages design
- Clock & Trigger distribution system with ≈ 10 ps resolution (also needed for Barrel ECAL)
- High Back-End processing power and bandwidth to exploit 3/4D at L1-Trigger level

Muon Systems

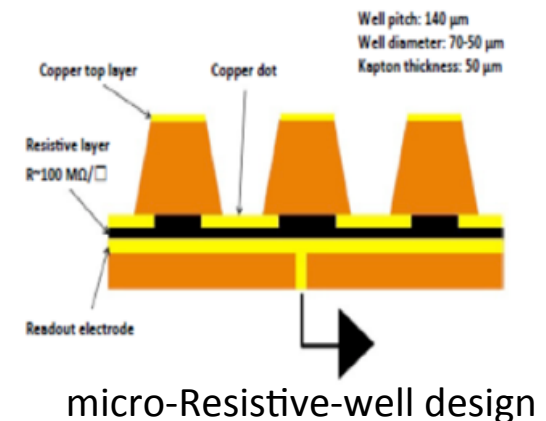
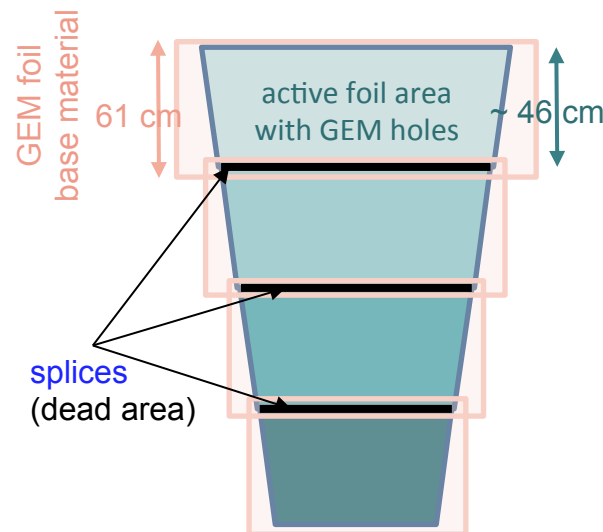
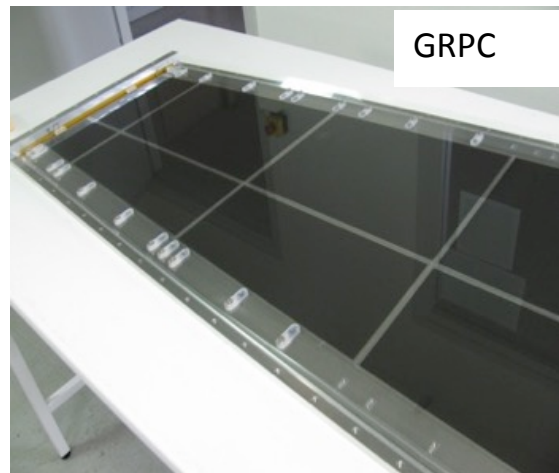
Muon system upgrades

- DT on detector electronics (minicrates) replacement - requires radiation tolerant FPGA and 40 MHz readout with GBT to remove L1-trigger limitations
- CSC readout replaced in last stations inner rings - similar to 1st station upgrade in LS1
- New chambers to complete forward region at $1.6 < \eta < 2.4$ region
 - Pair of triple GEMs in 2 first stations - high rate, and resolution for L1-trigger
 - iRPC in stations 3 and 4 - high rate, and timing resolution to reject background
- Coverage up to $\eta = 3$ - 6 triple GEMs (ME0) for μ -tagging



Muon Upgrades R&D

- Longevity of all Muon systems being evaluated at GIF++ up to 3 x HL-LHC margin
- iRPCs developments in Glass and Bakelite, and double and multi-gap designs
 - Promising results on rate capabilities with small and large prototypes
 - Test of multi-gap + “Petiroc” chip shows 60 ps resolution (H. Mathez’s presentation)
- GEMs
 - Engineering design of GE2/1, with spliced foils due to large size
 - R&D on new micro-Resistive-well design (m-R-Well) (ME0 & GE2/1), simpler assembly & good time resolution $\sigma_t < 2$ ns with eco-friendly gas (Ar/CO₂) gas

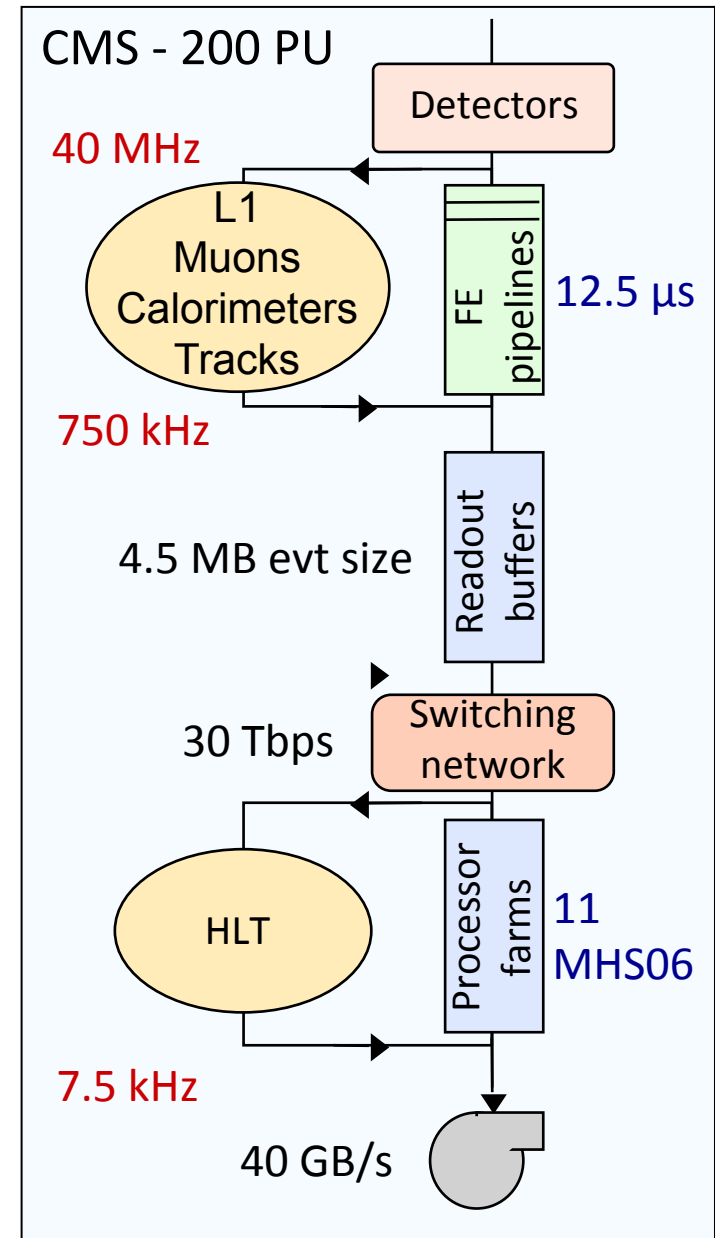


→ To alleviate work during (30 months) LS3 some of these upgrades could be anticipated in LS2 and YETS, as well as other infrastructure upgrades

L1-Trigger/HLT/DAQ

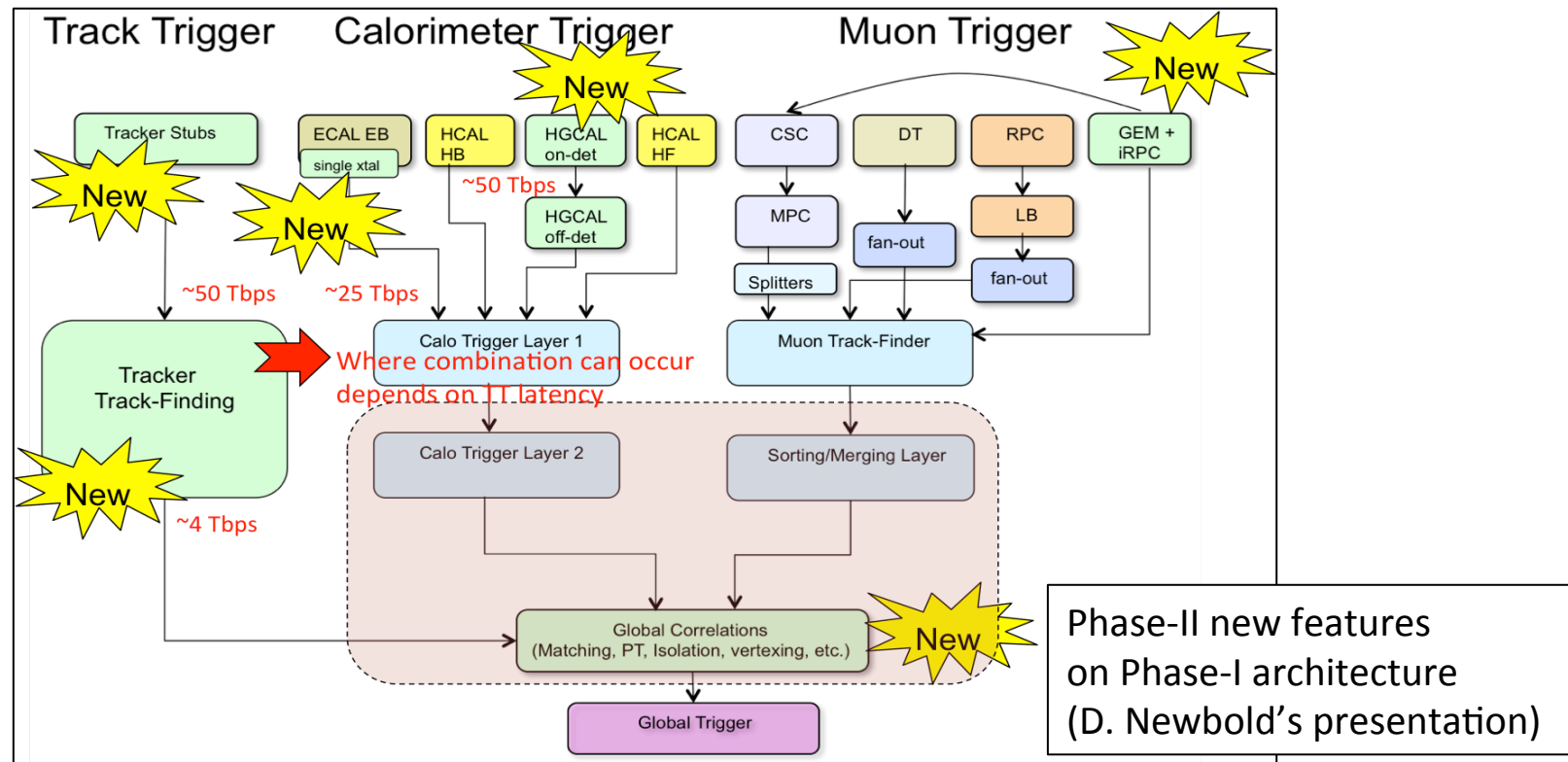
Trigger/DAQ Architecture

- **L1-Trigger**
 - 12.5 s latency, 750 kHz accept rate at 200 PU (see next slide)
- **Trigger timing, throttling and control**
 - High bandwidth bi-directional link allowing trigger information to steer readout
- **DAQ**
 - Similar event builder, HLT & storage as present
 - Increase bandwidth - 800 links x 100 Gbps to provide 30 Tbps throughput at 30% occupancy
- **HLT**
 - Processing power scales as PU x L1 rate ≈ 52 wrt Run 2 at 200 pileup - need to develop improved software using new computing technics beyond gain at constant resources
 - HLT rejection 1/100 (as current system)



Trigger/DAQ Architecture

Simulation work is on-going to establish requirements for trigger primitives of each detector and when combinations occur - latency for tracks and EC primitives and performance will determine hardware implementation (E. Perez's presentation)



→ For implementation need to identify commonalities across projects, define requirements and specifications for hardware, firmware and software platforms - identify technical options and streamline development efforts

Summary

CMS has a well understood set of upgrades to deliver the physics program at the HL-LHC (described in a Technical Proposal and a Scope Document)

The work is proceeding to further optimize designs for performance and costs in preparation of TDRs, on a timescale of two years for the main construction projects; benefit of a dedicated detector for improved pileup mitigation through precise time association with vertices is investigated

The ACES workshop is a great opportunity to streamline efforts through common approaches and developments

The 3rd ECFA workshop Oct. 3-6, 2016, will be an other opportunity to discuss the entire HL-LHC program: physics perspective, interface of accelerator and experiments, detector designs and performance, common and dedicated experiment R&Ds in all areas