IP blocks and design sharing

Michael Campbell

7th March 2016

Outline

- Brief summary of activities in the CERN Microelectronics Section (EP-ESE-ME)
- Motivation for IP block repository
- Boundary conditions
- Proposal
- Summary of reactions

ME Section Structure March 2016

Jorgen Christiansen
Elia Conti
Moritz Horstmann
Luis Jara
Sara Marconi

Kostas Kloukinas
Wojciech Bialas
Alessandro Caratelli
Davide Ceresa
Gert Olesen
Anna-Maria Tyrovouzi

Walter Snoeys
Cesar Marin
Costanza Cavicchioli
Inkyung Hwang
Chaosong Gao
Cyril Grassot
Daehyeok Kim
Thanu Kugathasan
Herve Munier
Aurelien Neveux
Jerome Rousset
Ping Yang

Michael Campbell
Jerome Alozy
Rafa Ballabriga
Iraklis Kremastiotis
Xavi Llopart
Tuomas Poikela
Edinei Santin
Lukas Tlustos
Pierpaolo Valerio
Winnie Wong

Paulo Moreira
Rui Francisco
Szymon Kulis
Pedro Leitao
Christian Paillard
David Porret

Federico Faccio
Stefano Michelis
Giacomo Ripamonti

Paul Aspell
Mietek Dabrowski

Jan Kaplon

Staff
Student/Fellow
CERN User

Activities in the ME Section

- Common projects (useful for all detectors)
  - Technology support and foundry services
  - Radiation hardness qualification/monitoring of CMOS processes
  - High speed data links
  - DCDC convertors

- Experiment specific activities
  - Muon detector readout for CMS
  - Tracker readout for CMS
  - Full custom front-end design (ATLAS and CMS)
  - RD53 – very rad hard pixel detector development (ATLAS and CMS)
  - Monolithic pixel detector development for Alice
  - Medipix and related hybrid pixel readout

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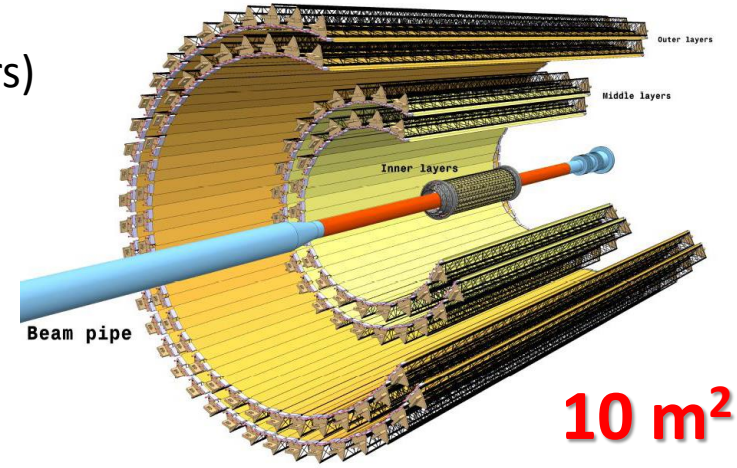
FULL SCALE PROTOTYPES

Construct 7 layers (3 inner layers, 4 outer layers)



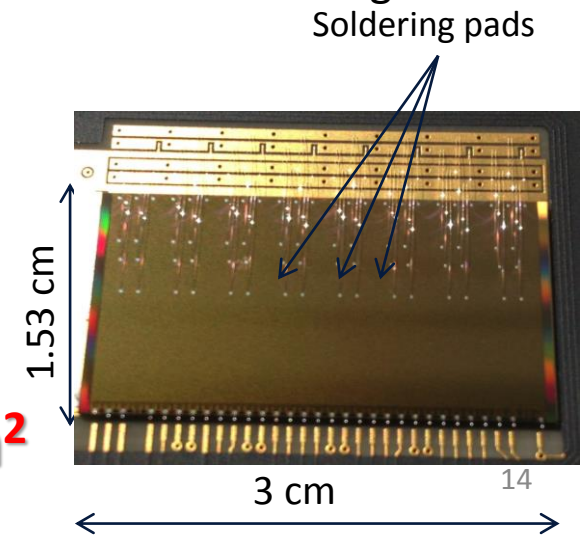
10 m²

Building block: full scale prototype chip: ALPIDE

Designers from 7 institutes : CERN/INFN/WUHAN/YONSEI/NIKHEF/IRFU/IPHC:

G. Aglieri, M. Bonora, A. Collu, Y. Degerli, C. Flouzat, D. Gajanana, C. Gao, F. Guilloux, S. Hristozkov, D. Kim, T. Kugathasan, A. Lattuca, M. Lupi, S. Lee, D. Marras, C. Tobon, G. Mazza, H. Mugnier, J. Rousset, G. Usai, P. Yang, A. Dorokhov, H. Pham, W. Snoeys

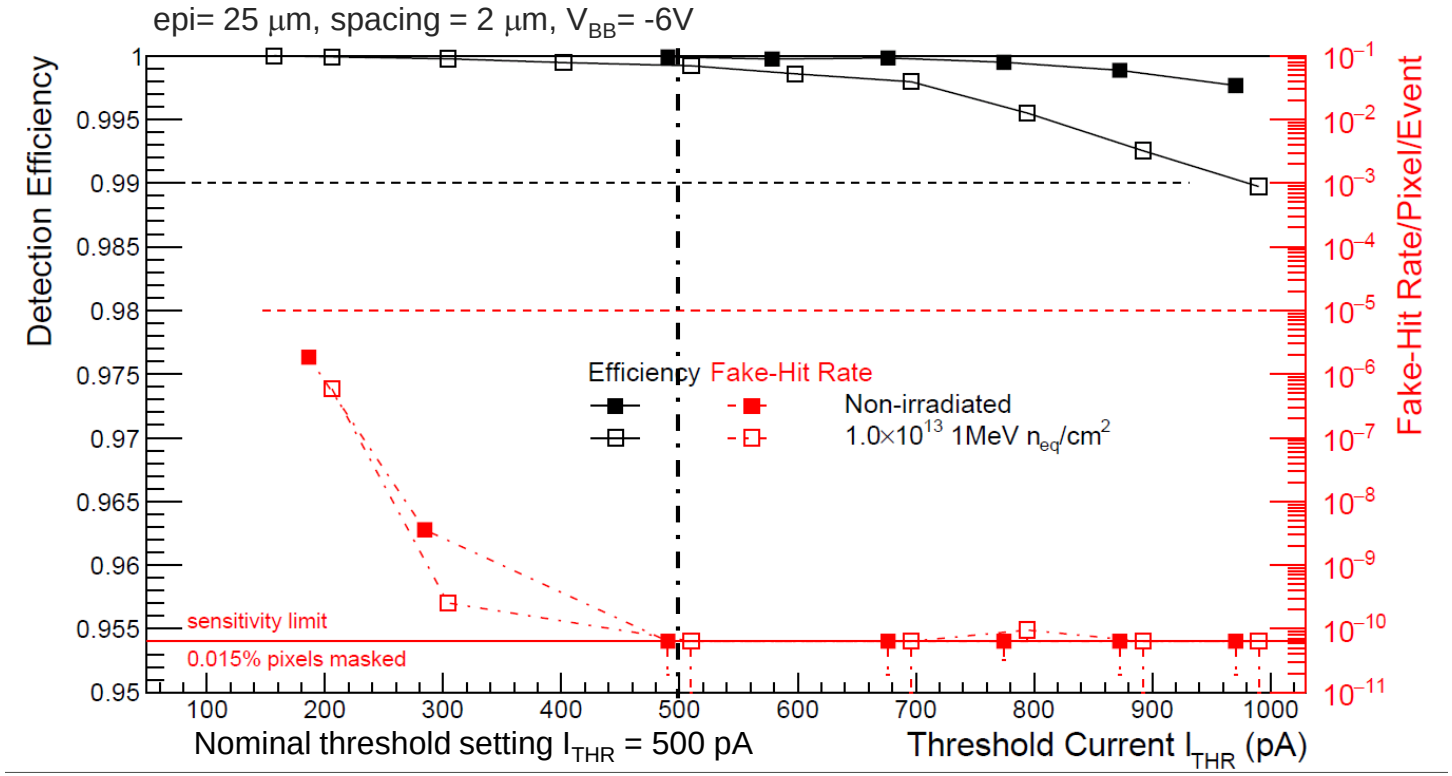
- 40 nW in-pixel amplifier/comparator allows architectures other than rolling shutter
- Hit driven readout (priority encoder)
- Power consumption < 35 mW/cm²
- Integration time ~ 4 µs
- chip size: 15 x 30 mm²
- ~ 500 000 pixels of 28 x 28 µm²
- Soldering pads over the pixel matrix



4.5 cm²

pALPIDE-2 Test Beam Results

Detection Efficiency and Fake Hit Rate before and after irradiation



$\varepsilon_{det} > 99\%$ @ $\lambda_{fake} << 10^{-5}$ / event/pixel -> large margin over design requirements

Measurements on chips with 25 μm high-resistivity epitaxial layer, thinned to 50 μm, -6 V reverse bias

1 non irradiated and 1 irradiated with $1.0 \cdot 10^{13}$ 1 MeV n_{eq}/cm^2

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Timepix3

Pixel matrix	256 x 256
Pixel size	55 x 55 μm^2
Technology	CMOS 130 nm
Measurement modes	• Simultaneous 10 bit TOT and 14 + 4 bit TOA • 14 + 4 bit TOA only • 10 bit PC and 14 bit integral TOT
Readout type	• Data driven • Frame based (both modes with zero suppression)
Dead time (pixel, data driven)	>475 ns (pulse processing + packet transfer)
Output bandwidth	40 Mbits/s – 5.12 Gbits/s
Maximum count rate	0.4 Mhits/mm^2/s (data driven mode)
TOA Precision	1.56 ns
Front end noise	60e- RMS
Minimum threshold	~500 e-

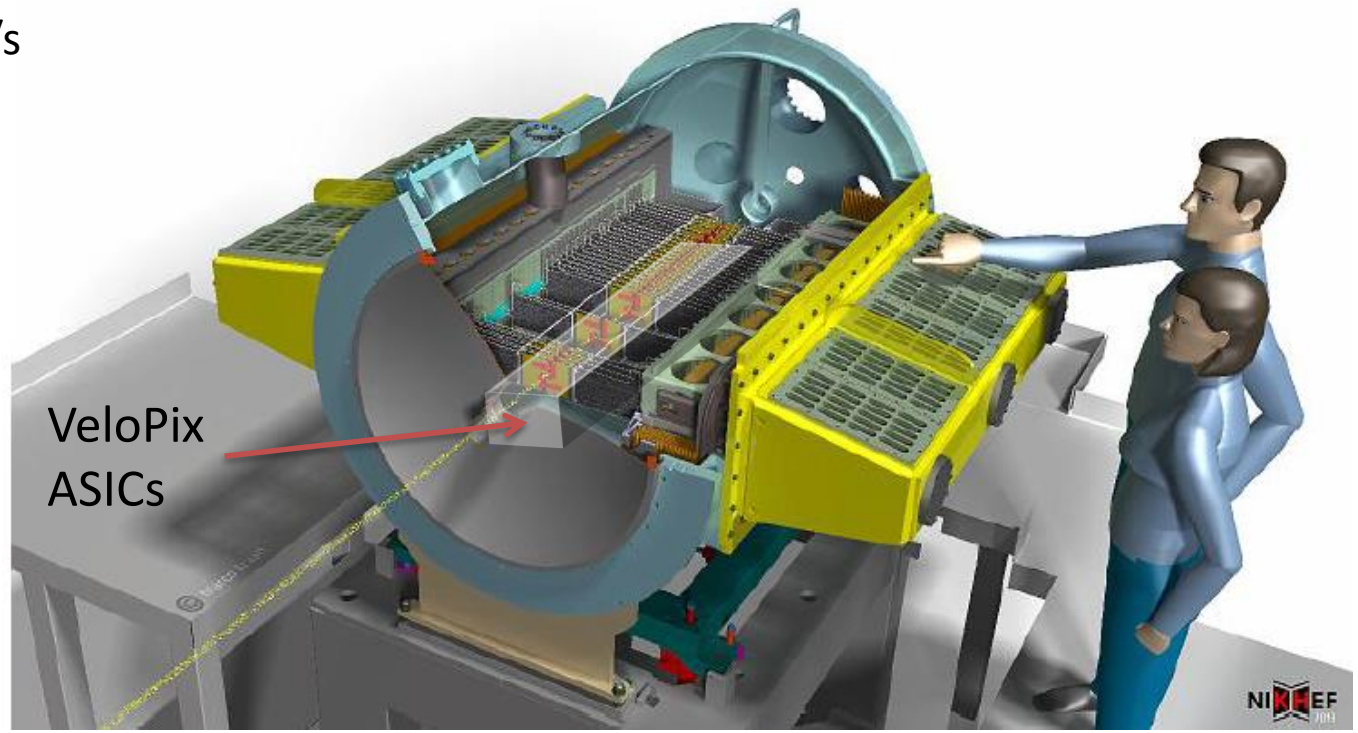
Designed in the context of the Medipix3 Collaboration together with Nikhek and Bonn

VeloPix

- Hybrid pixel detector (HPD) Readout ASIC for the LHCb VELO upgrade
- The ASIC reads out all bunch crossings at 40 MHz
- Installation planned for LS2

<u>The VELO upgrade:</u>

- Approx. 2.85 Tbit/s
- 26 module pairs
- 624 ASICs
- 41 Mpixels*



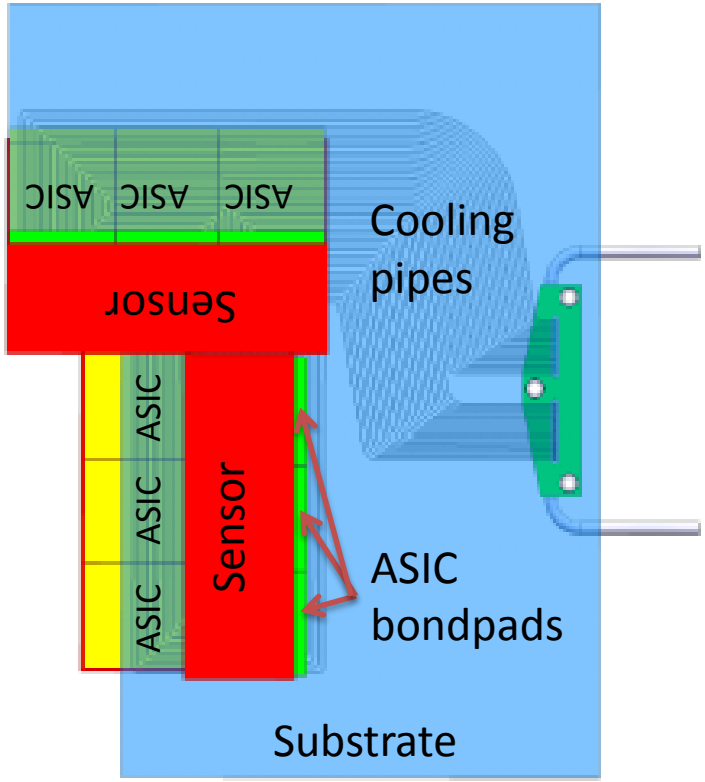
*Nokia Lumia 1020 (2013)
also has 41 MP camera

VELOPIX

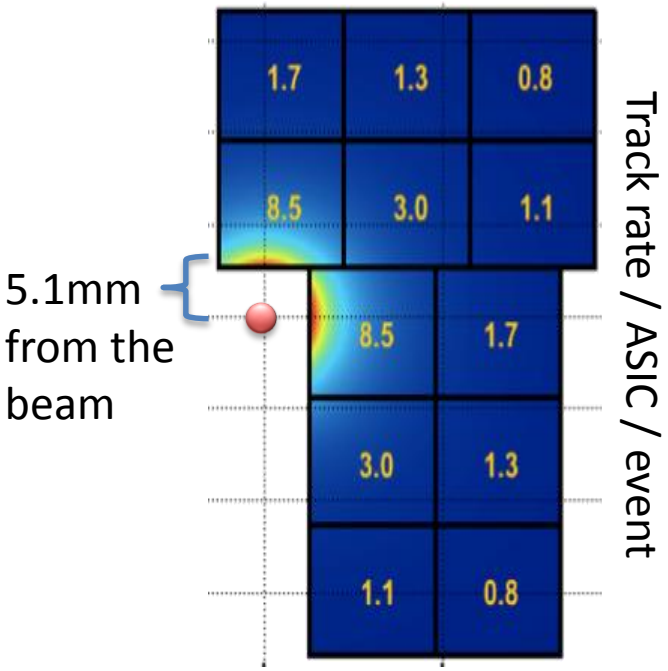
Pixel matrix	256 x 256
Pixel size	55 x 55 μm^2
Technology	CMOS 130 nm
Measurement modes	• Binary output @ 20 Gbps • 6 bit TOT or 6bit PC @ 640 Mbps
Readout type	• Data driven with 0-suppression @20 Gbps • Frame based (only through slow control)
Dead time (pixel, data driven)	Limited by analog pulse processing
Output bandwidth	5.12 Gbps – 20.48 Gbps
Maximum count rate	4 Mhits/mm^2/s (data driven mode)
TOA Precision	25 ns with on-pixel timewalk correction logic
SEU Robustness	Fully triplicated control logic, clock trees, reset and configuration registers
Front end noise	60e- RMS
Minimum threshold	~500 e-

VeloPix ASIC module (12 ASICs)

Module of 12 VeloPix ASICs:



Track rates for module:



Highly non-uniform radiation dose:
8×10^{15} to 2×10^{14} n_{eq}/cm^2

Peak rates:

Hottest chip 15.1 Gbits/s

hottest module: 61.2 Gbits/s

Medipix3 work with CLICdp

- CLICpix2
  - 2nd version of CLICpix with larger matrix
  - 65nm CMOS
  - 128 x 128 pixels on 25μm pitch
  - 5-bit ToT, 8-bit ToA, Power pulsing etc
- C3PD
  - AMS 180nm HV-CMOS
  - HV-CMOS pixel detector/readout
  - Stand alone readout of compatible with CLICpix2
- Through Silicon Vias
  - Feasibility of post processing demonstrated with good yield
  - RO wafer thinning to 50μm works
  - Medipix4 Collaboration will deign 4-side tile-able chips

Motivation for IP Block sharing

- During LHC-1 sharing of blocks was mostly within sub-detector groups or from CERN to outside institutes.
- Licensing was based on ‘gentlemen’s agreements’
- Significant duplication of effort

- RD-53 have agreement between member institutes but limited to RD-53 efforts
- For a more general purpose repository there is a need to solve the ‘engineer at the University of Saint-Genis’ problem

Boundary conditions

- Cadence Europractice licenses:
  - "Europractice Cadence tools may not be used for any commercial purposes, including contract design and re-assignment of IP to any third party." extracted from Cadence license statement
  - We will need a 'Cadence Variation Agreement' for those institutes wishing to contribute to and/or benefit from access to the repository
- We will start with TSMC 130nm and 65nm only
  - Only available to TSMC MTUA signatory institutes
- Export regulations
  - Rad hard blocks need to be labelled as such and only made available to institutes in Wassenaar Arrangement Countries.

Proposal

- Repository to be managed by IMEC
- Access to repository to be limited to academic and research institutes
- Only abstract views available (like ARM)
- IMEC would add layout and rerun DRC (and LVS?) at submission
- IMEC would be responsible for maintenance of repository blocks (for Cadence upgrades etc)
- The designer name and institute will be associated with each block

Proposal (contd)

- IMEC will maintain a database for the blocks used which is accessible to member institutes (may help motivate “engineer from University of St. Genis”)
- Reference/acknowledgement to the repository in academic publications will be obligatory
- At submission IMEC and the submitting institute will decide % IP contributions for various partners
- In case of subsequent commercialization (and always subject to Cadence VA agreement) these %’s used for royalty distribution.

Reactions from community members (not already addressed)

- Fairly general recognition for need/usefulness to do something
- Going to 65nm and beyond we will need to learn to share effort
- Why limit it to HEP only?
- But quite a few reservations too related to ‘paradigm shift’ for our community

Reservations/Alternatives

- Request for more ‘liberal disclosure’ approach with access to full layout
- A ‘brokerage site’ permitting one-on-one agreements
- Open hardware type license? Apparently incompatible with Cadence/Europractice

- It is my understanding that most or all of these suggestions will be in contradiction with Europractice license

- Some people/groups will never submit a chip without having full layout access to layout

Practical

- Need to define “common layout style” (which routing layers, block heights etc)
- Detailed data sheets and documentation
- How do we pay IMEC? Should blocks be ‘paid’ to compensate for time saved?
- How about analog blocks as well as digital?

Questions/Discussion