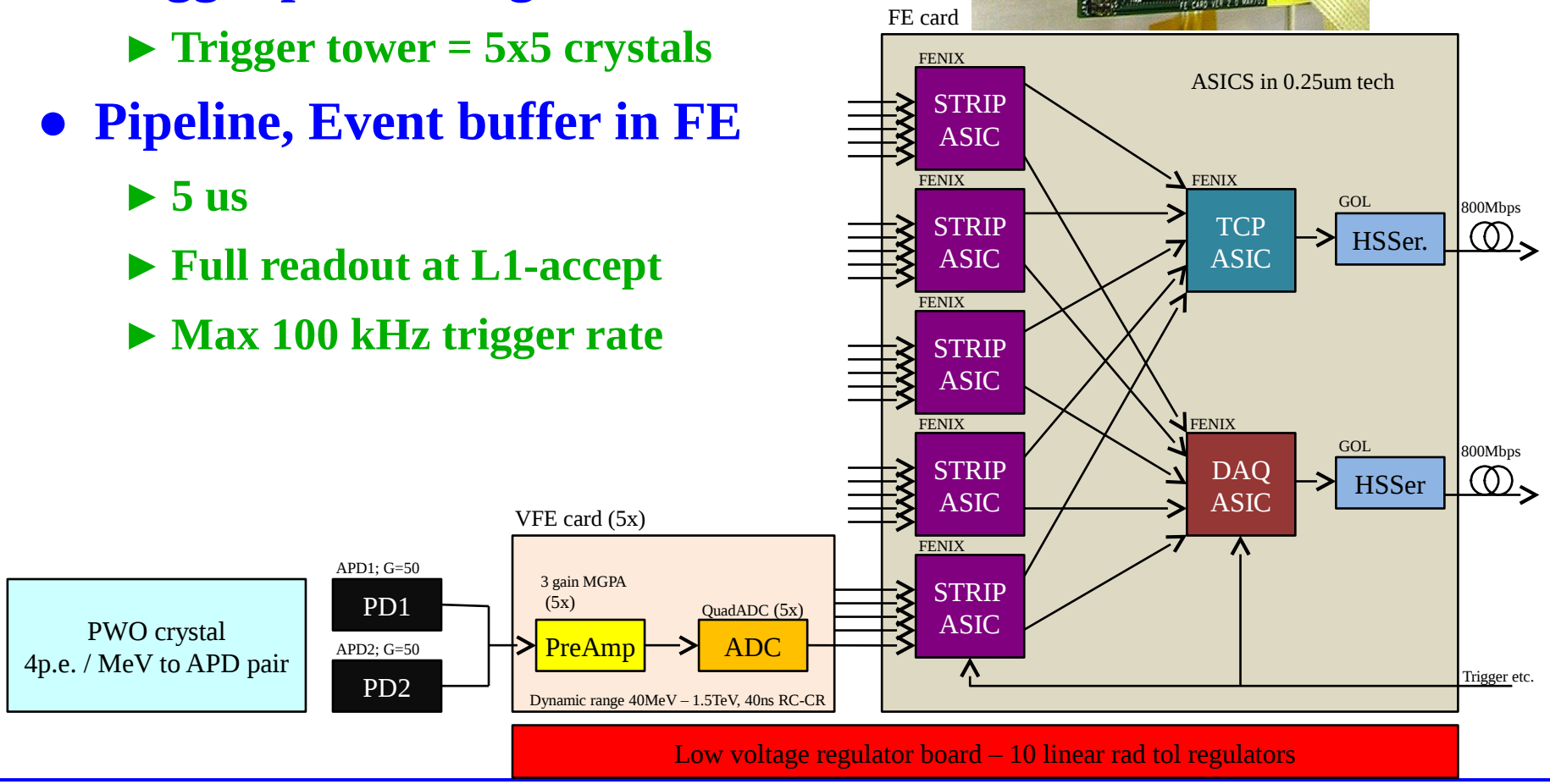
CMS-ECAL barrel upgrades for HL-LHC

- Legacy system
  - Today
  - Expected performances at LS3
- Upgrade constraints
  - Bounding conditions
  - Aging mitigation
  - Trigger constraints
  - Spike rejection
  - New features
- Upgrade scenarios
- On-going R&D
  - VFE
  - LV
  - FE
- Planning

Marc Dejardin
Irfu/SPP CEA-Saclay

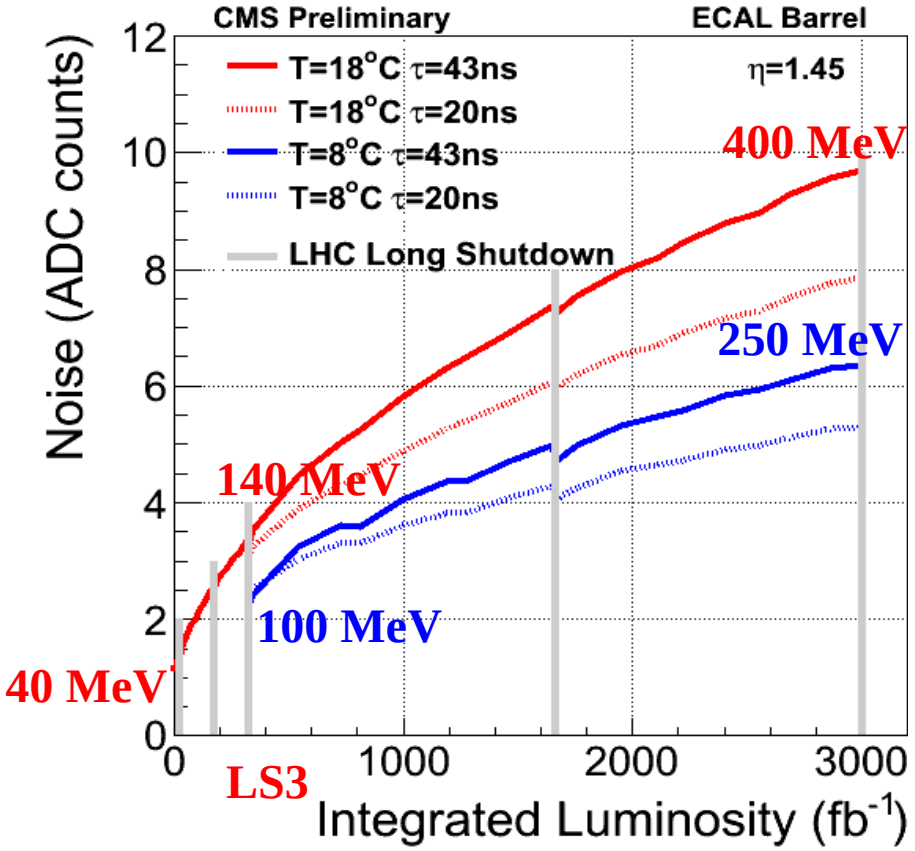
Legacy system

- **Modularity**
  - **25 channels = 1 Readout unit**
- **Features**
  - **Trigger primitive generation**
    - **Trigger tower = 5x5 crystals**
  - **Pipeline, Event buffer in FE**
    - **5 us**
    - **Full readout at L1-accept**
    - **Max 100 kHz trigger rate**



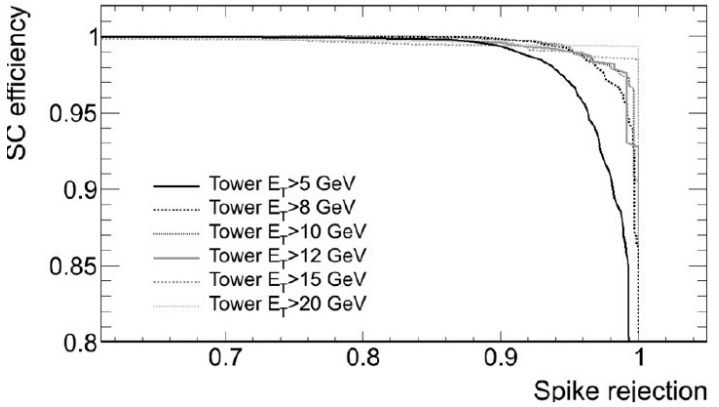
By LS3

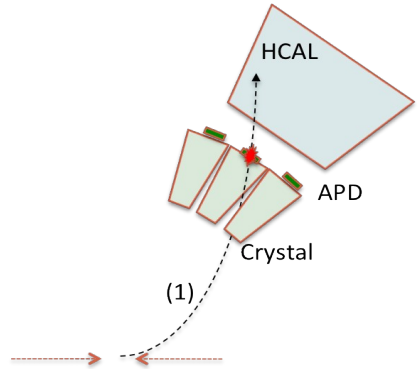
- **Noise**
  - **Evolution assuming present VFE design**



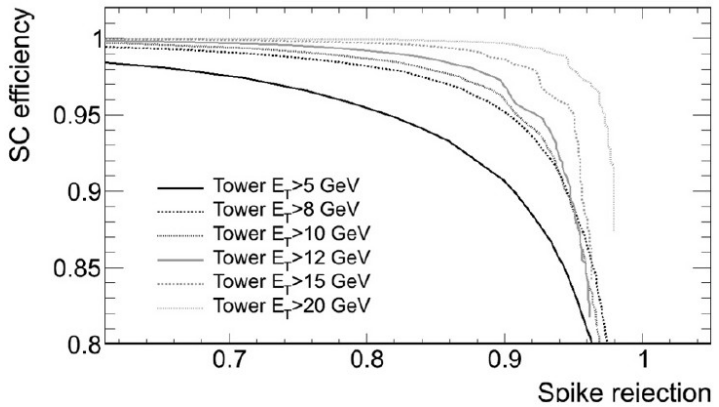
- **Spike rejection @L1**
  (direct energy deposition in APD)
  - **Online rejection= O(95%)(2012)**
  - **Sensitive to PU & APD I_{leak}**
    - ► **Sustainable up to LS3**

2012C conditions





300fb^{-1}, <PU>=70



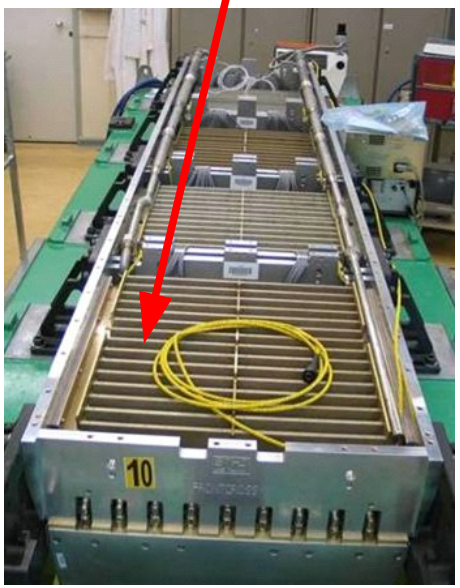
Upgrade requirements

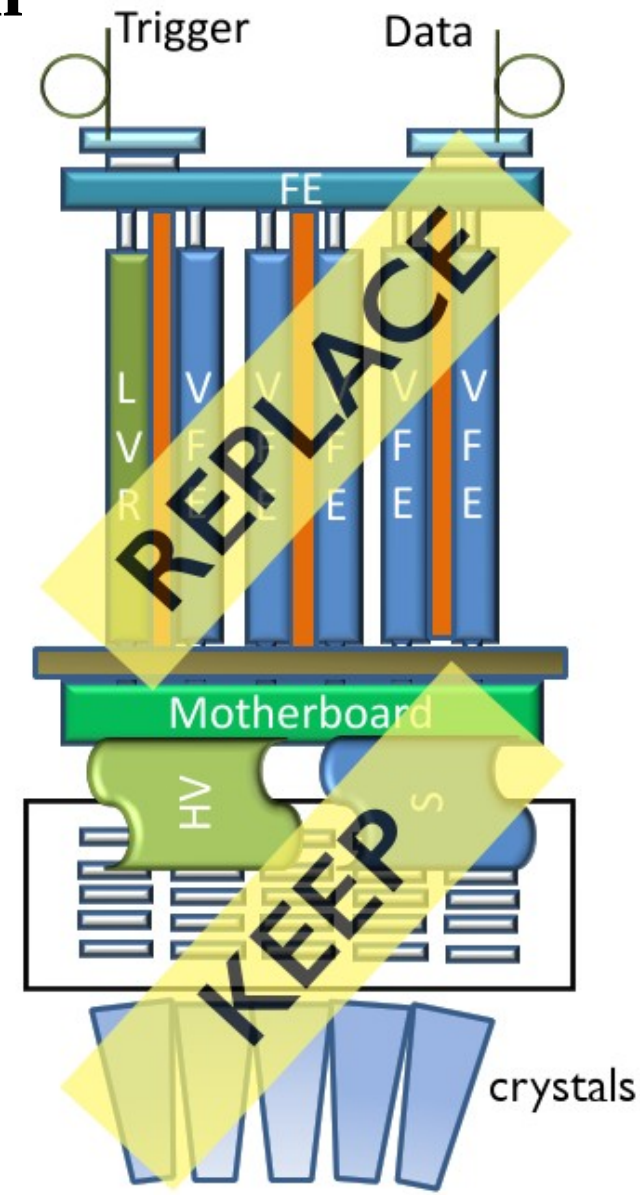
- Installation completed during LS3
- Comply to new trigger requirements
  - 12.5 µs latency (5 µs today)
  - 750 kHz L1 rate (100 kHz today)
- Mitigate spikes signals
  - Expect ~1 spike /bunch crossing
- Mitigate APD radiation damage
  - APD leakage current up to 200uA
    - ► Parallel noise increase /Worsen the spike signal tagging
- Mitigate Pileup
  - Out-of-time
  - In-time
- Maintain/Improve system reliability
  - Failure mitigation scheme
- All in one :
  - Try to restore initial ECAL performances

Boundary conditions

- **Keep the mechanical structure as-is**
  - **Cooling system**
  - **Mother boards**
  - **Signal paths and connectors**

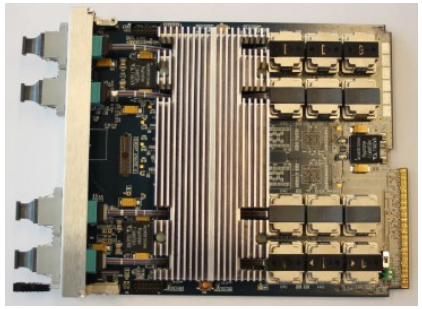
You have to plug here !





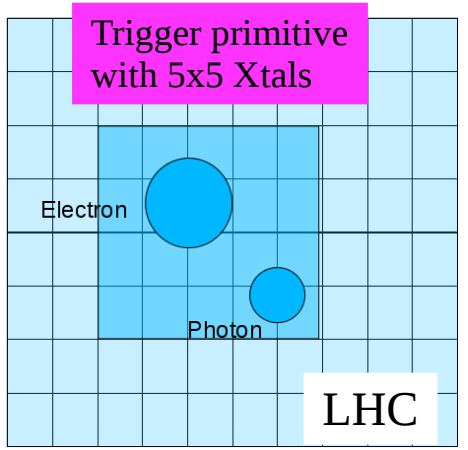
- **Use back-end complying to CMS standard**
  - **e.g.: x-TCA**

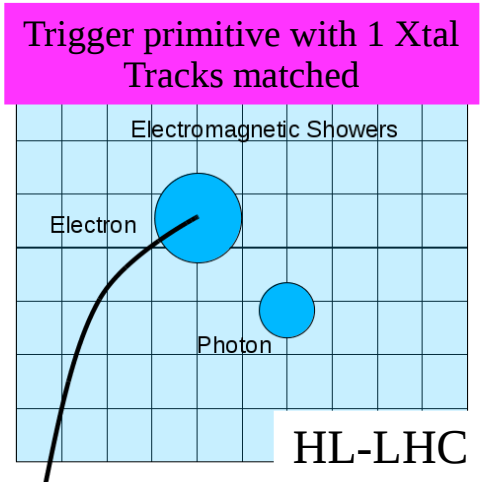
You have to read-out here !



Upgrade concepts

- **Put all algorithmic in OD electronics**
  - **Trigger-less FE**
- **Single crystal information available at L1**
  - **Synchronous readout of all crystal information**
    - ► **Improve trigger efficiency**
    - ► **Correlation with tracker info**
- **Reduce ECAL working temperature**
  - **8 °C instead of 18 °C**
    - ► **APD Leakage current /2** ☺
    - ► **Light yield +30%** ☺
- **Reduce signal shaping time**
  - **Decrease parallel noise contribution**
    - ► **Goes like $\sqrt{\tau}$**
  - **Improve OOT pileup mitigation**

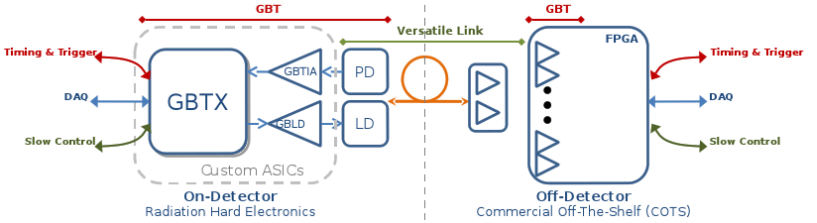




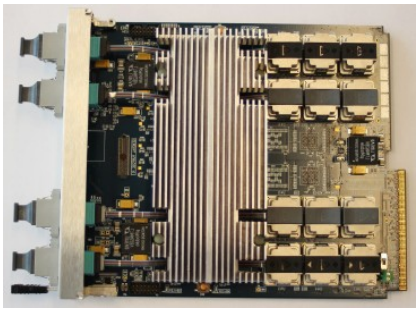
The way to go

- **Don't reinvent the wheel**
  - **Use common developments as much as possible**
    - ► **DC-DC converters**

    - ► **Optical links (lpGBT)**



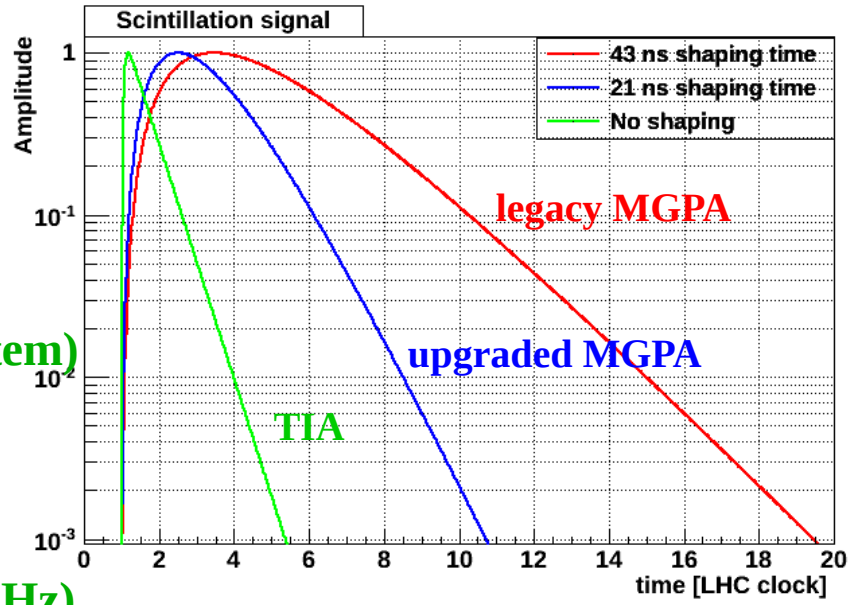
    - ► **Off detector electronics**
      - **Common development with HGCAL, HB ?**
      - **Efficient calorimeter trigger generation**



- **Concentrate efforts on ECAL specific features**
  - **Optimize APD signal reconstruction**
    - ► **Mitigate leakage current increase**
    - ► **Improve spike signal mitigation**
    - ► **Improve pileup mitigation → Add timing information**

APD signal conditioning

- **Reminder:**
  - **Shaping as short as possible**
    - ► Decrease parallel noise (APD leakage current mitigation)
    - ► Mitigate OOT pileup
- **Options:**
  - **CR-RC shaper MGPA-like**
    - ► Reduced shaping time
      - e.g: $\tau_{CR\text{-}RC}$ ~ 20 ns (~40 ns in legacy system)
    - ► Trade-off with ballistic deficit
  - **Trans-impedance amplifier (TIA)**
    - ► Shaping defined by TIA bandwidth (<50 MHz)
    - ► Hopefully more information on signal at high frequency
  - **Gated charge integrator (GQI)**
    - ► Enhanced version of QIE
      - resolution/radiation hardness



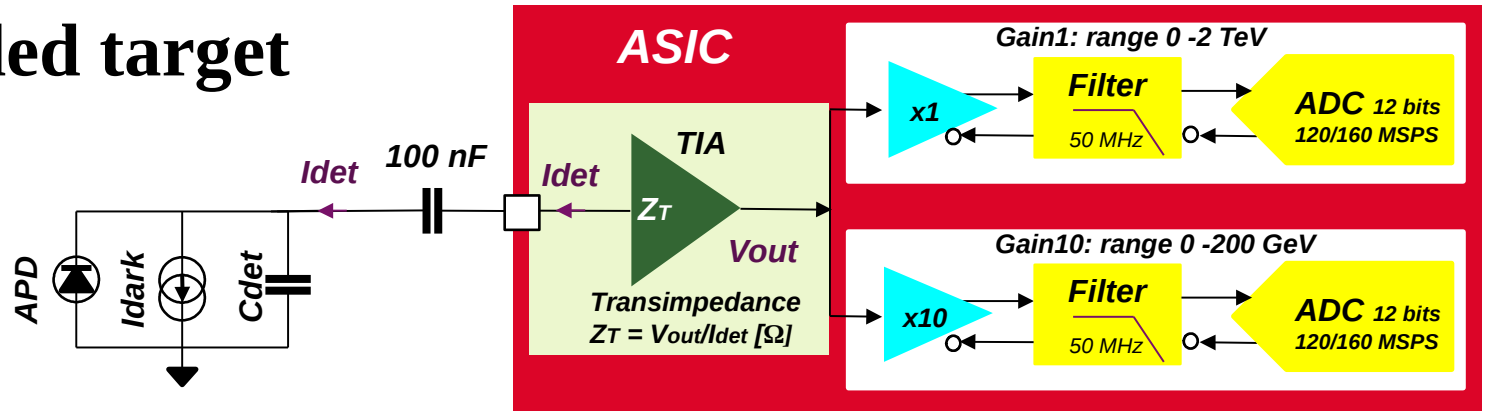
Example: TIA R&D

- **Design of TIA asic in TSMC 130 nm technology**

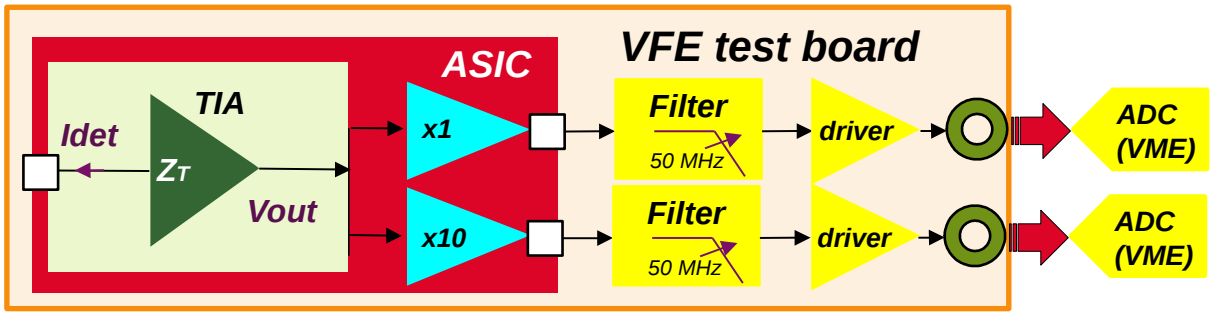
(P. Baron Irfu/SEDI CEA-Saclay)

  - **Specifications :**
    - C_{det}=200 pF, I_{leak} from 10 uA to 100 uA
    - E_{max} = 2 TeV, E_{min}=100 MeV, 2 outputs : G1 and G10
    - Bandwidth <50 MHz

- **Intended target**

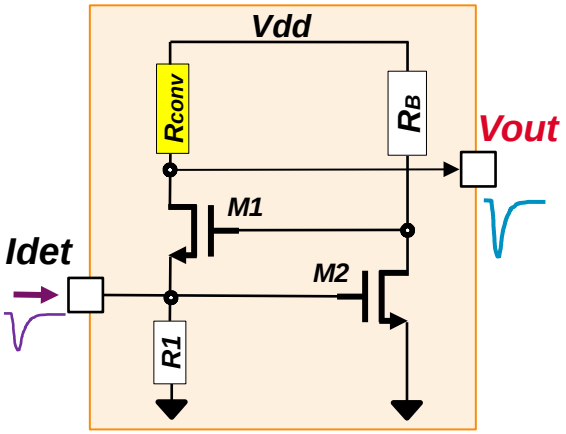


- **Prototype**

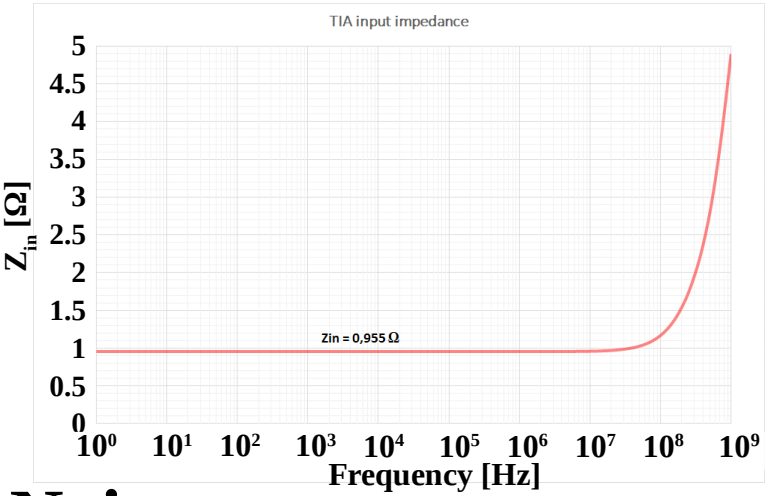


TIA architecture and performances (sim.)

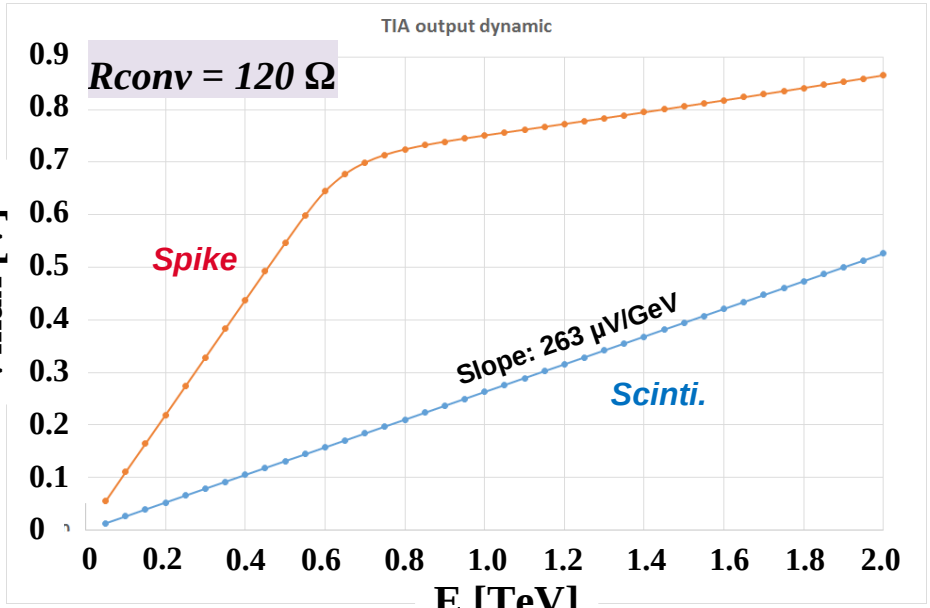
- **Regulated common gate**



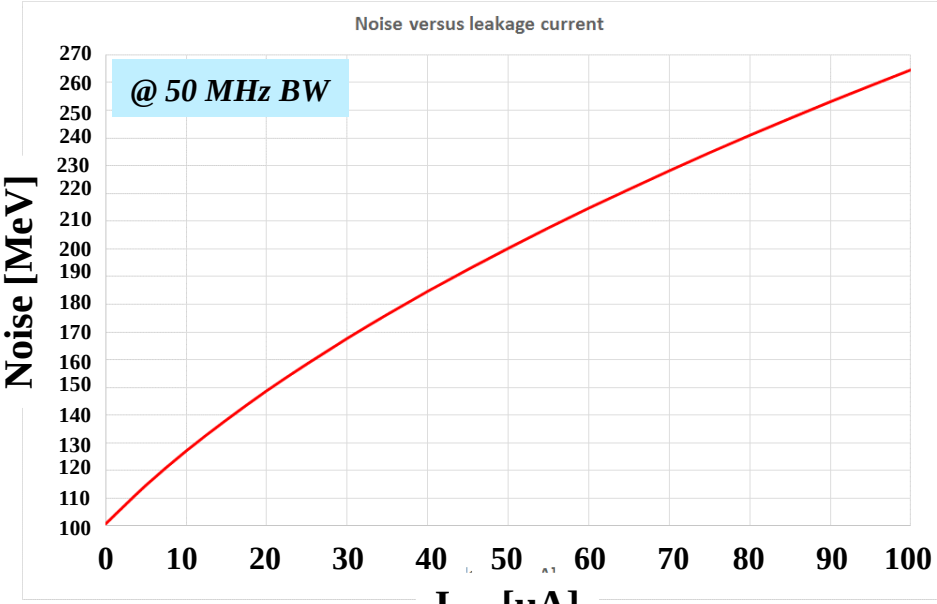
- **Low input impedance**



- **Dynamics**

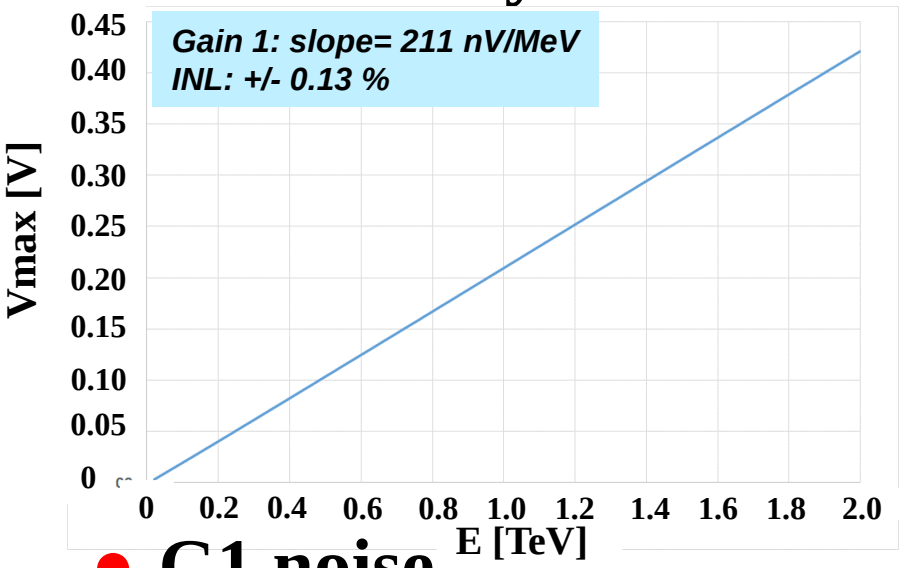


- **Noise**

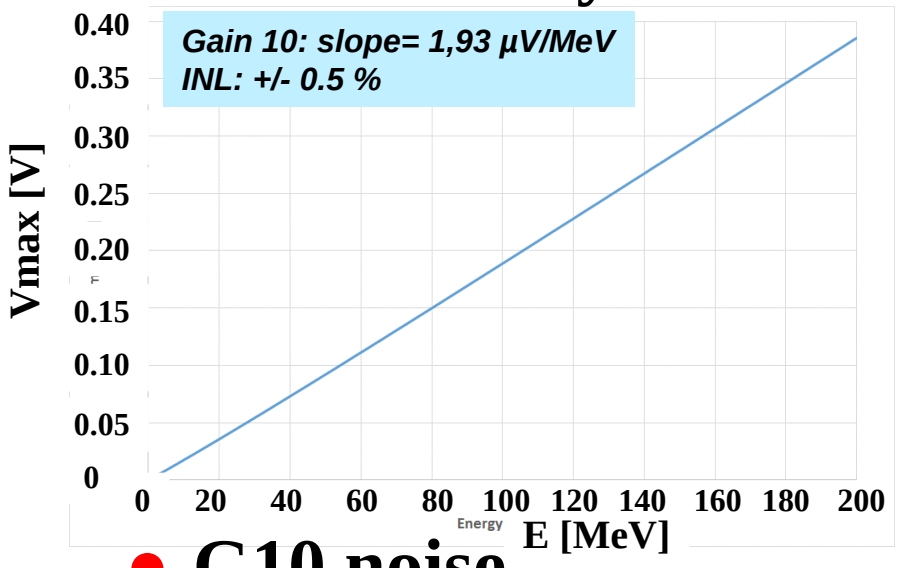


G1 and G10 outputs performances (sim.)

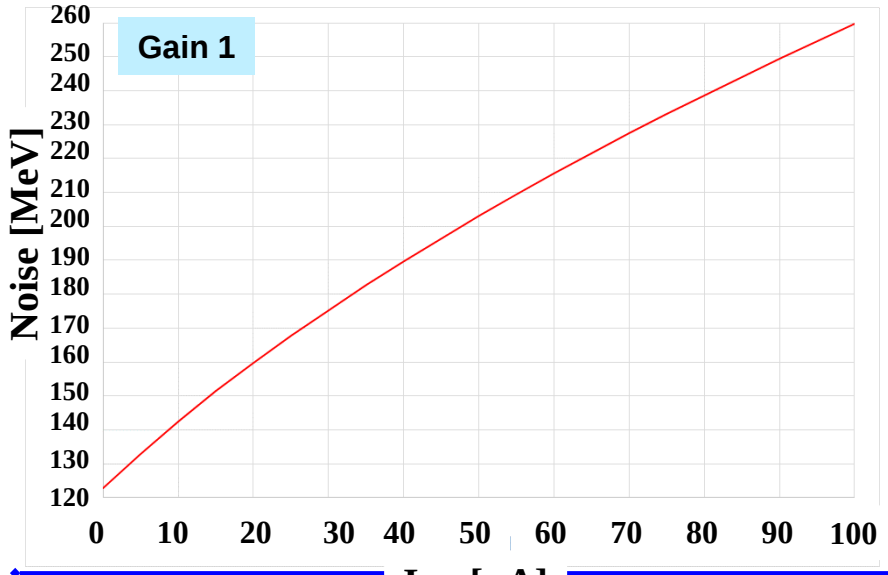
- **G1 linearity**



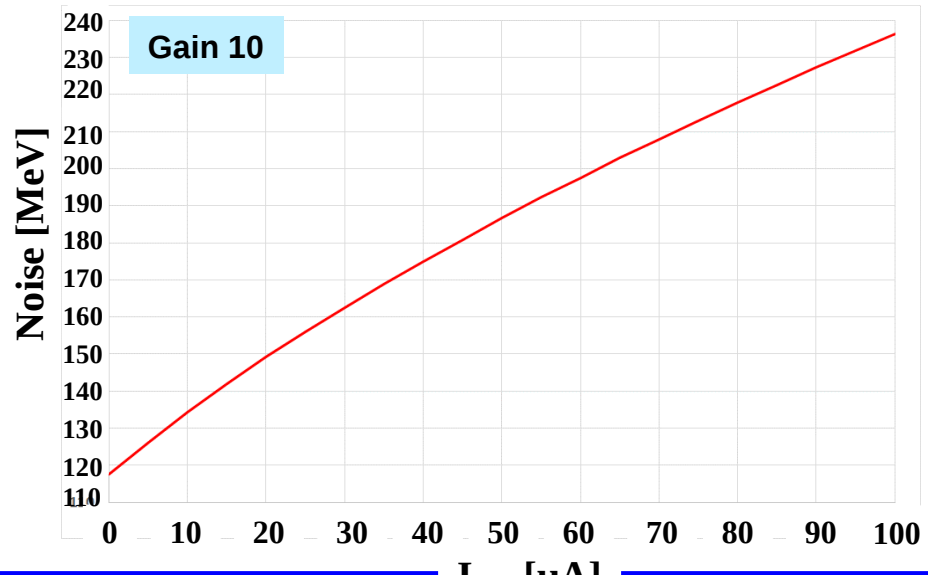
- **G10 linearity**



- **G1 noise**

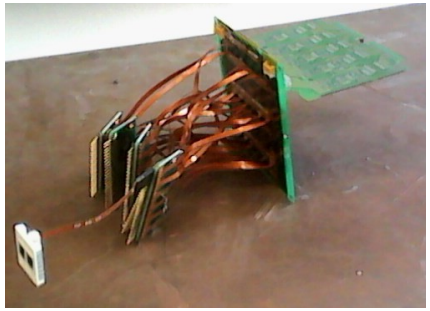


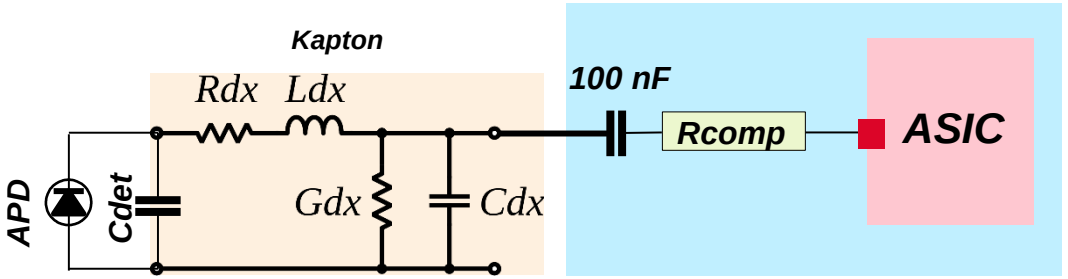
- **G10 noise**



System performances (sim.)

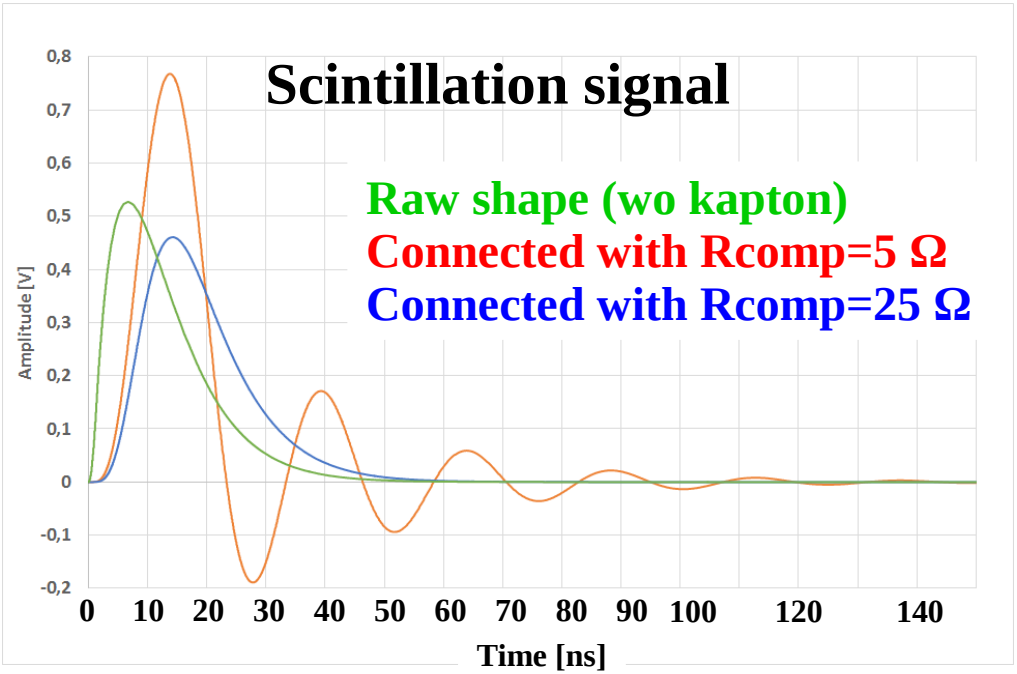
- **Connect TIA to ECAL barrel**
  - **Add connection strip lines (a.k.a. kaptons)**





Kapton Line parameters:
R = 0,05 Ω/cm;
L = 3,75 nH/cm;
C = 2,4 pF/cm
Length: 20 – 30 cm

Deal with 75-100 nH connections



Drawback:

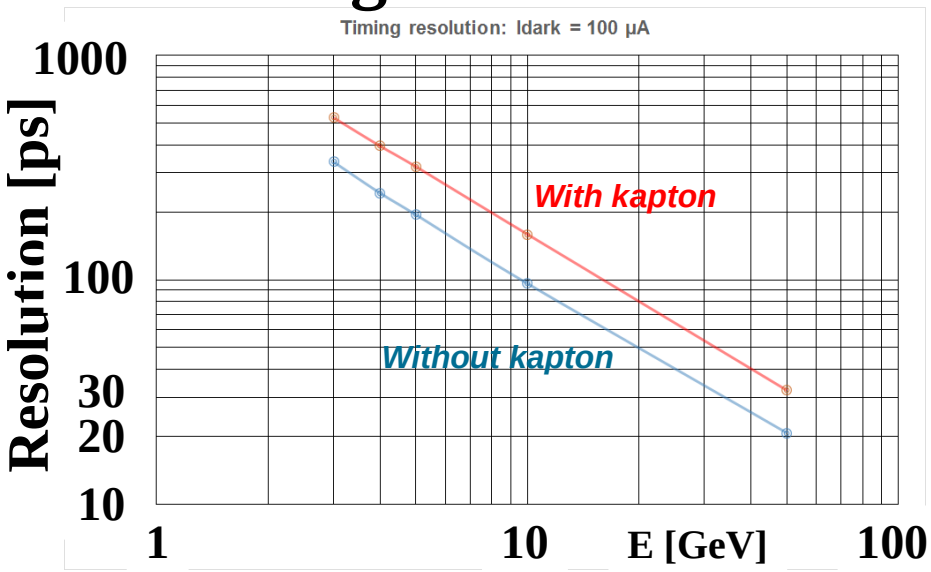
Noise ↑ (Ileak = 0 µA); Bandwith ↓; Timing↓

But:

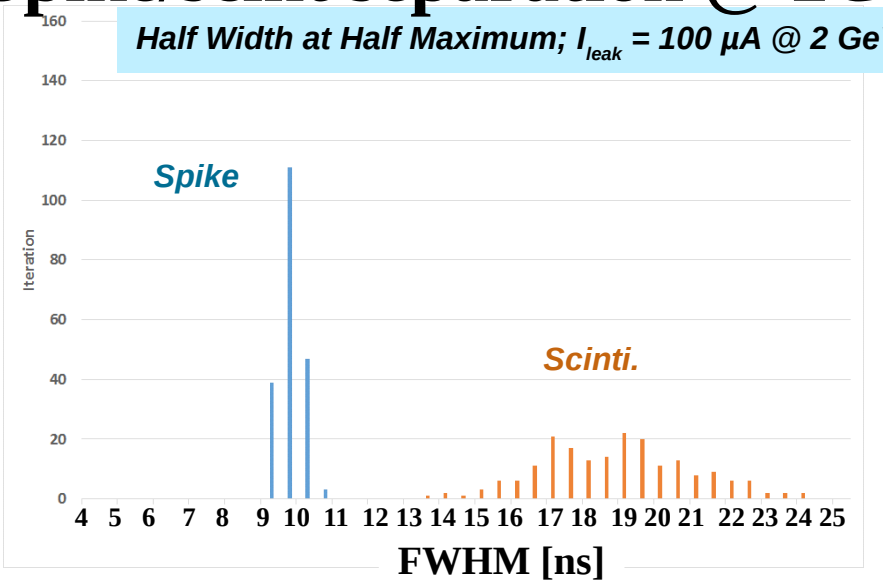
Noise ↓(Ileak > 10-20 µA) since Bandwith ↓

System performances
Worse conditions: End of HL-LHC (sim.)

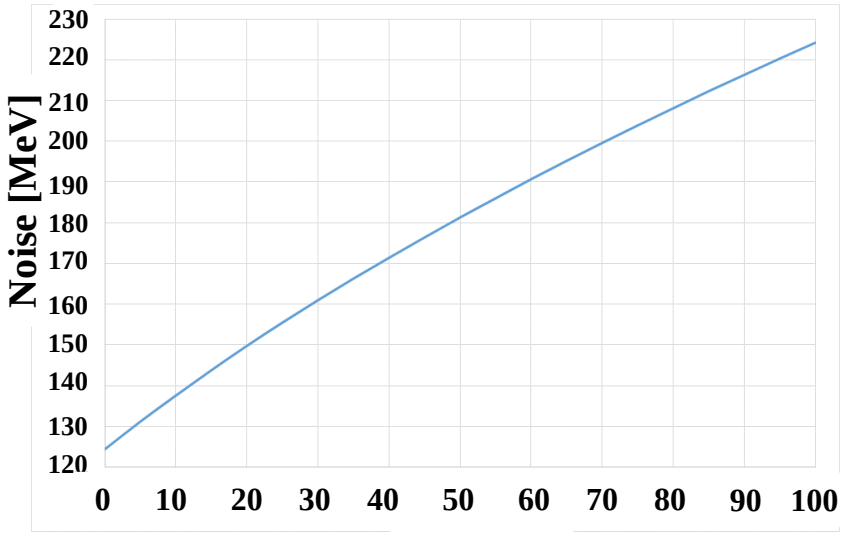
Timing resolution



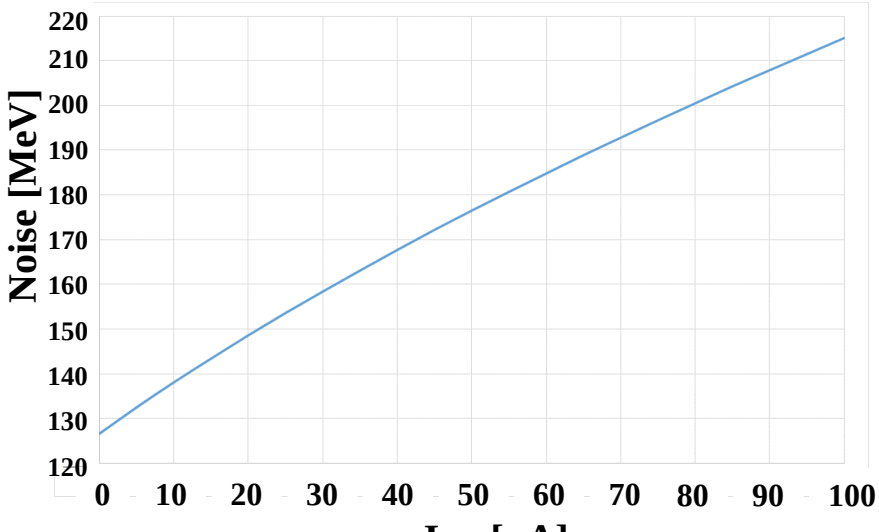
Spike/scint separation @ 2GeV



G1 noise

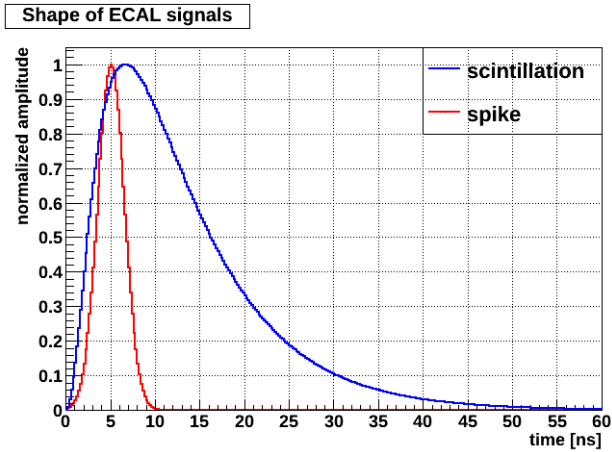


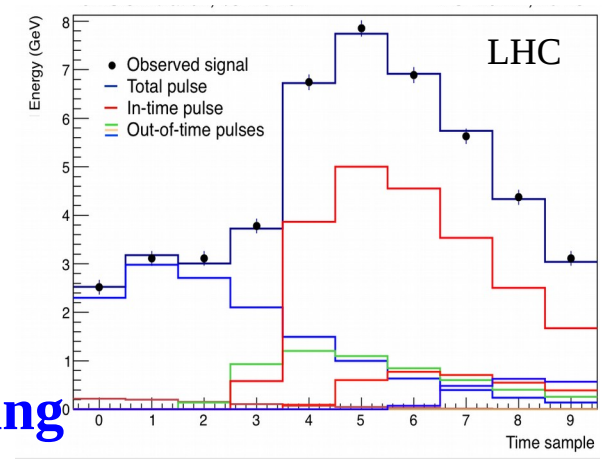
G10 noise

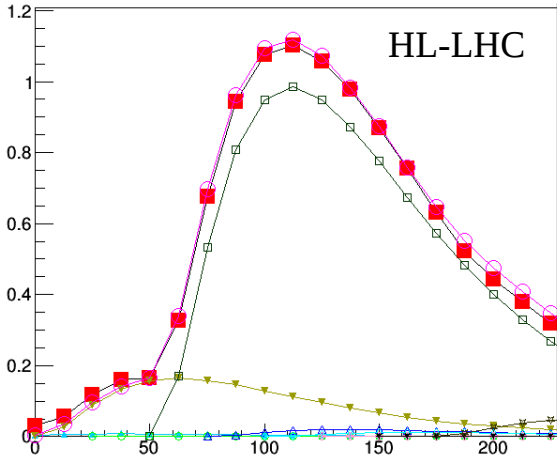


APD signal digitization

- **Prepare for best online and offline analysis**
  - **Provide enough information for**
    - ► **Online spike tagging**
      - **Shape analysis**
    - ► **Timing measurement**
    - ► **Offline energy reconstruction with Pileup**
      - **Multifit algorithm**





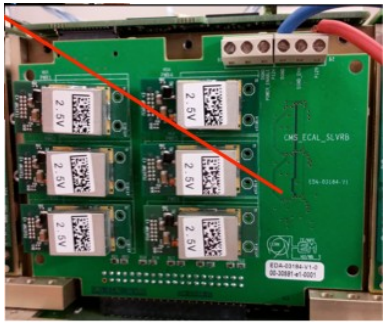


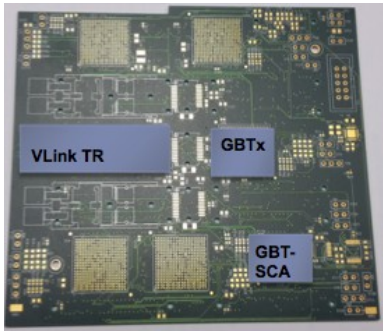
  - **Investigate signal over-sampling**
    - ► **Benefits/costs of 80/160 MHz sampling**
      - **System performances gain**
      - **ADC design/cost**
      - **Data rate/volume**

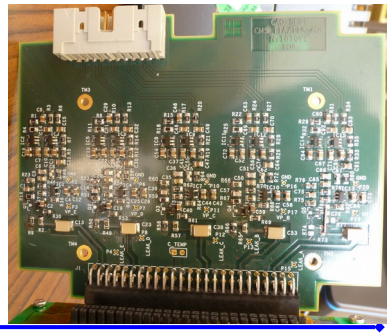
Ongoing work

- **Investigating use of commercial ADC core**
- **Check DC/DC converters compatibility with ECAL and CMS**
  - **Magnetic field**
  - **Induced noise on legacy system**
- **Get experience with GBT links**
  - **Upgraded FE board for legacy system**
- **Prepare test beam campaign to check working hypothesis**
  - **Prototype VFE with op-amp TIA**

► **Check APD noise model, Ultimate timing resolution**







Forthcoming major milestones

- **Summer 2016: First Comprehensive Review**
  - **Evaluate concepts of VFE upgrade**
- **Q3 2017: Technical Design Report (TDR)**
  - **Evaluate technical specifications and expected performances of VFE, LVR, FE**
  - **Evaluate feasibility of SM cooling**
  - **Evaluate trigger strategy and online/offline performances**
- **Q3 2019: Engineering Design Report (EDR)**
  - **Technical validation of VFE, LVR and FE prototypes**
- **Q1 2021: Electronic System Review (ESR)**
  - **Assess readiness for production**

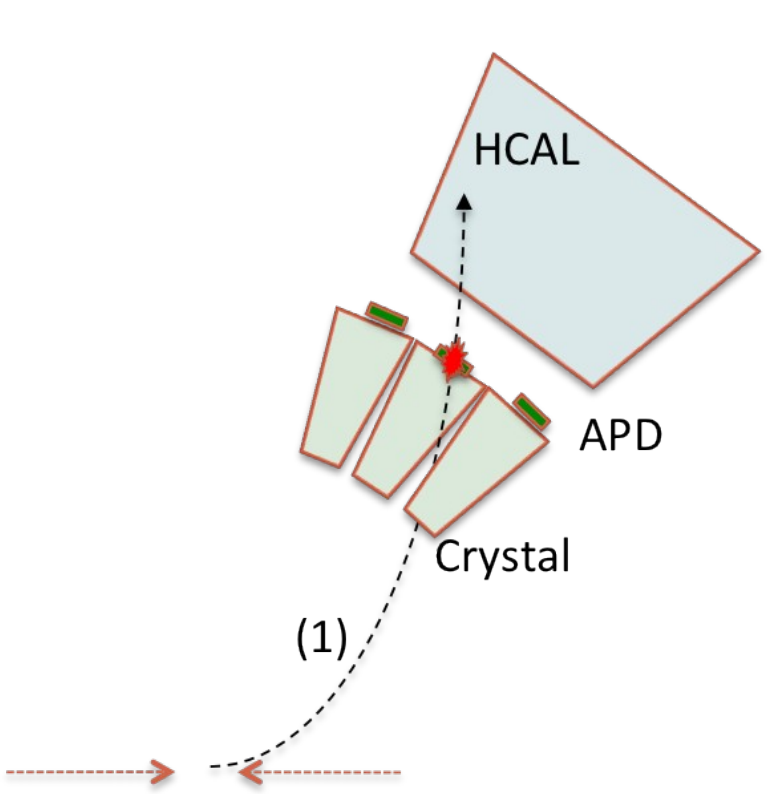
Conclusions

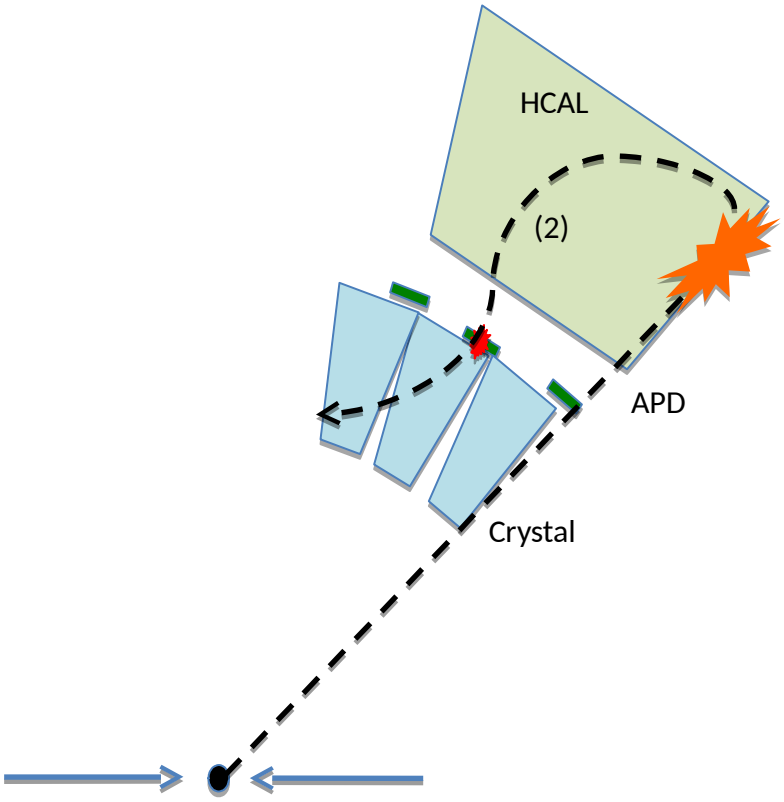
- CMS barrel calorimeter upgrades project well defined
- Ambitious upgrade program
  - Recover ECAL performances after 10 years of running
  - Prepare detector for a new decade of data taking
  - Read enough information from detector to be versatile
  - Export all algorithms to back-end electronics
    - ► Freedom to tune algorithm to follow detector aging
    - ► Adapt to unforeseen “features”
- Rely on development from third party
  - DC-DC converters
  - lpGBT

Backup

CMS ECAL Barrel Anomalous events:
Spikes

Hadrons interacting with the APD's causing anomalous high E deposits



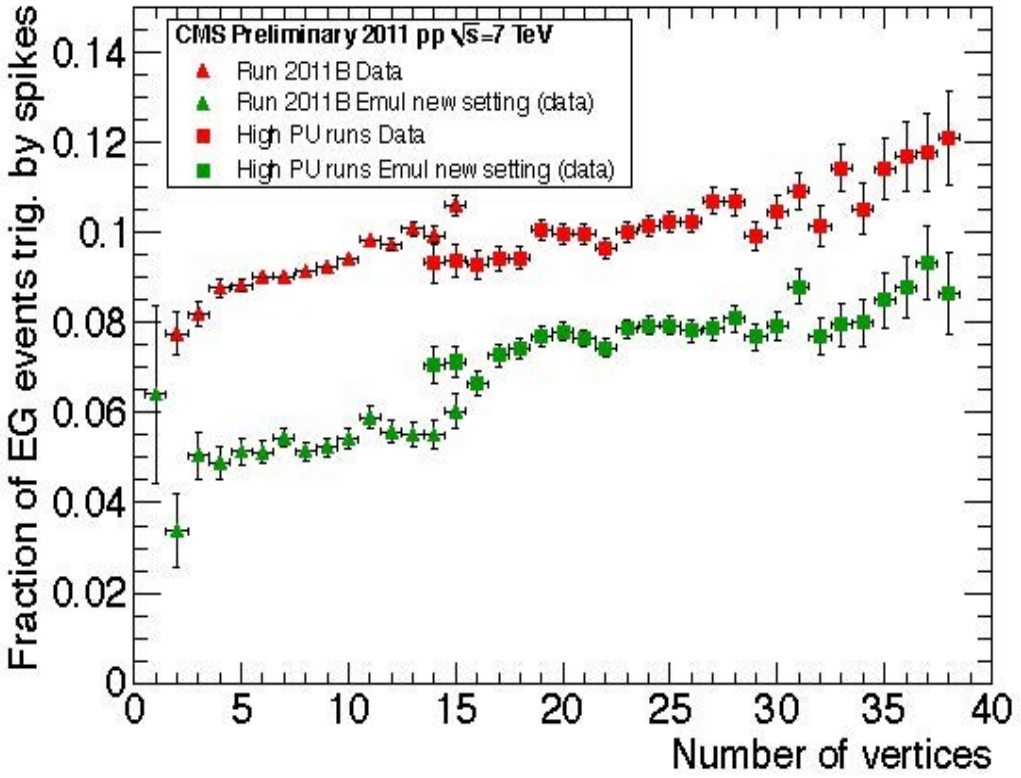


Hadrons come from primary interaction and backsplash

M. Hansen, CERN. magnus.hansen@cern.ch

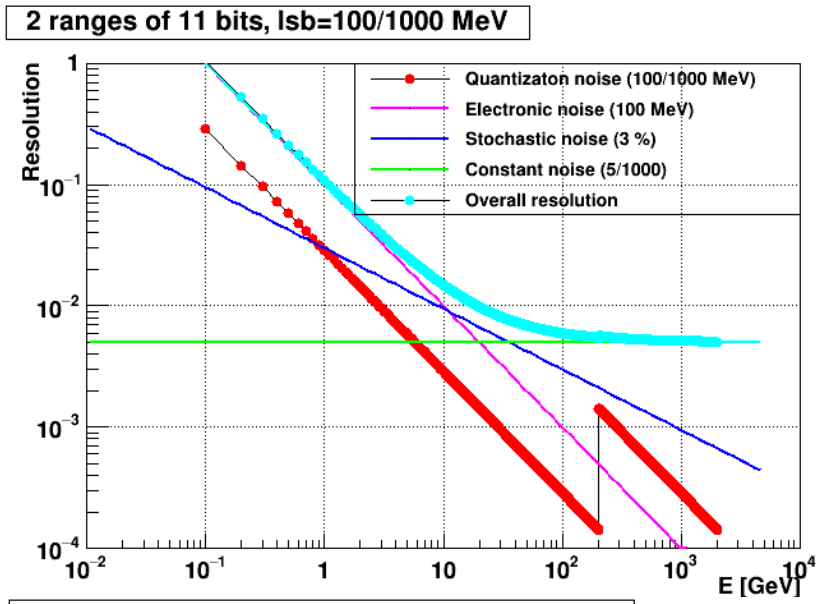
Spike rates

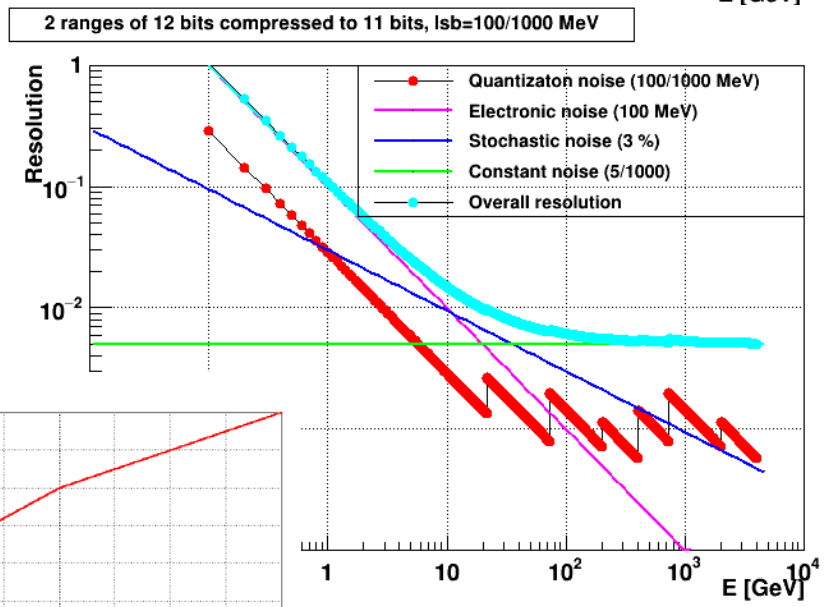
- L1 Spike rejection in 2012 O(95%)
  - Rate sustainable up to LS3 with somewhat raised channel threshold
- Legacy Spike Rejection Algorithm is sensitive to PU (see plot ->)
- Exploring improvements having access to full granularity of data in the trigger path
  - Single crystal readout
- Exploring pulse-shape variables to provide an additional efficiency/rejection safety margin
  - Analogue Signal Processing

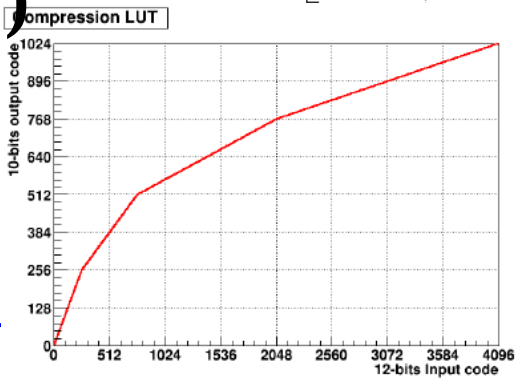


Data rate

- **Hypothesis :**
  - **Oversampling @ 160 MHz**
- **12 bits + 2 gains = 13 bits/sample**
  - **10.4 Gb/s per VFE board**
    - ► **Above GBT capabilities**
- **11 bits + 2 gains = 12 bits/sample**
  - **9.6 Gb/s per VFE board**
    - ► **At the edge of GBT capabilities**
- **12 bits + 2 gains + digital compression (LUT) = 11 bits/sample**
  - **8.8 Gb/s per VFE board**
    - ► **Fit in 1 GBT link**







Timeline of High Level Milestones

Q2 2016: **VFE.HL.2016.1: Draft initial VFE ASIC specifications**

Q4 2016: **LVR.HL.2016.1: Demonstrate feasibility of EB electronics with DC/DC convertors instead of LV regulators**

VFE.HL.2016.2: Define final VFE ASIC specifications - commence design

Q1 2017: **FE.HL.2017.1: First FE demonstrator with 5 Gb/s links**

Q3 2017: **REV.HL.2017.1: Technical Design Report**

LVR.HL.2017.1: Test beam appraisal of LVR board - benchmark performance

Q1 2018: **VFE.HL.2018.1: First prototype of VFE board available with new ASICs**

Q1 2019: **FE.HL.2019.1: First FE prototype with 10 Gb/s links**

LVR.HL.2019.1: Final validation of LVR board - demonstrate performance

Q3 2019: **VFE.HL.2019.1: Validation of overall concept (VFE+FE+LVR)**

REV.HL.2019.1: Engineering Design Report

Q2 2020: **VFE.HL.2020.1: Accelerated ageing and radiation exposure of all 3 boards**

OD.HL.2020.1: Validation of OD readout design

Q4 2020: **VFE.HL.2020.2: Test-beam verification of all components in SM, at lower temperature.**

Q1 2021: **REV.HL.2021.1: Electronics Systems Review** (readiness for production)