Status of the ATLAS New Small Wheel Frontend Electronics

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On behalf of the ATLAS Muon Collaboration

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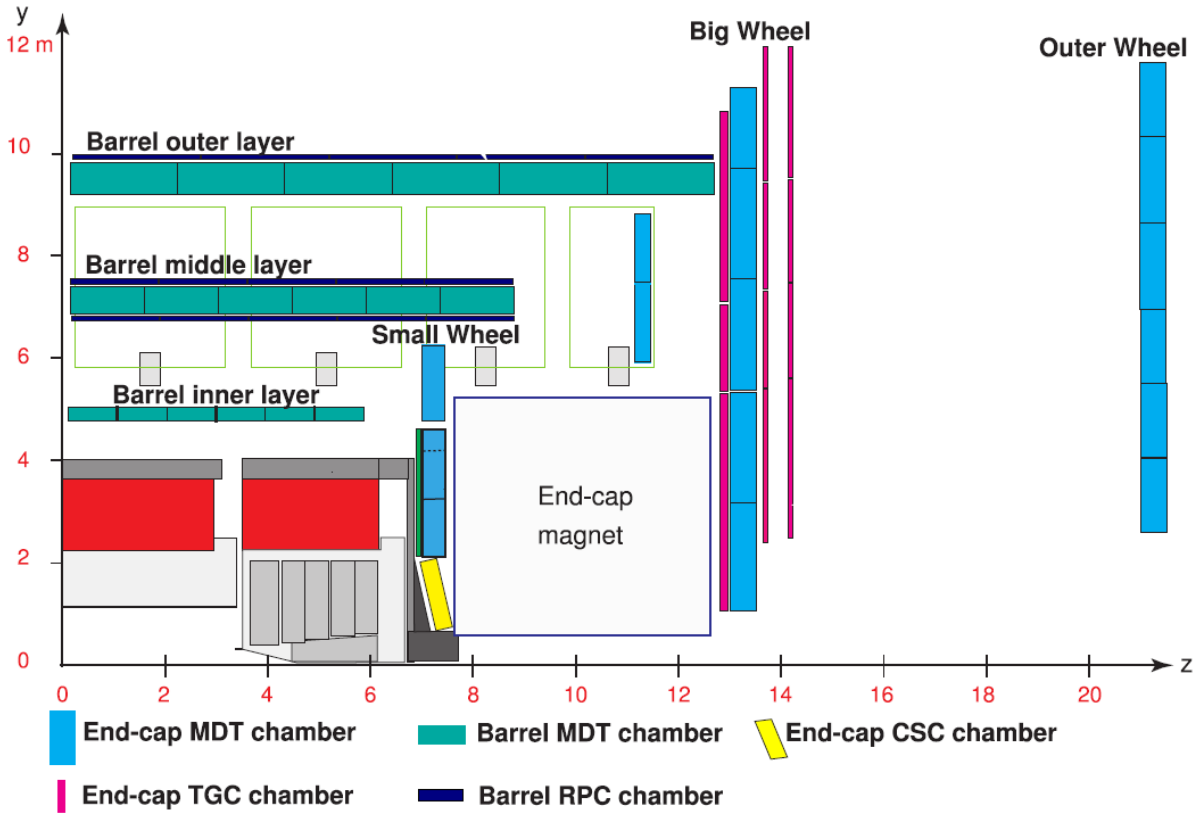
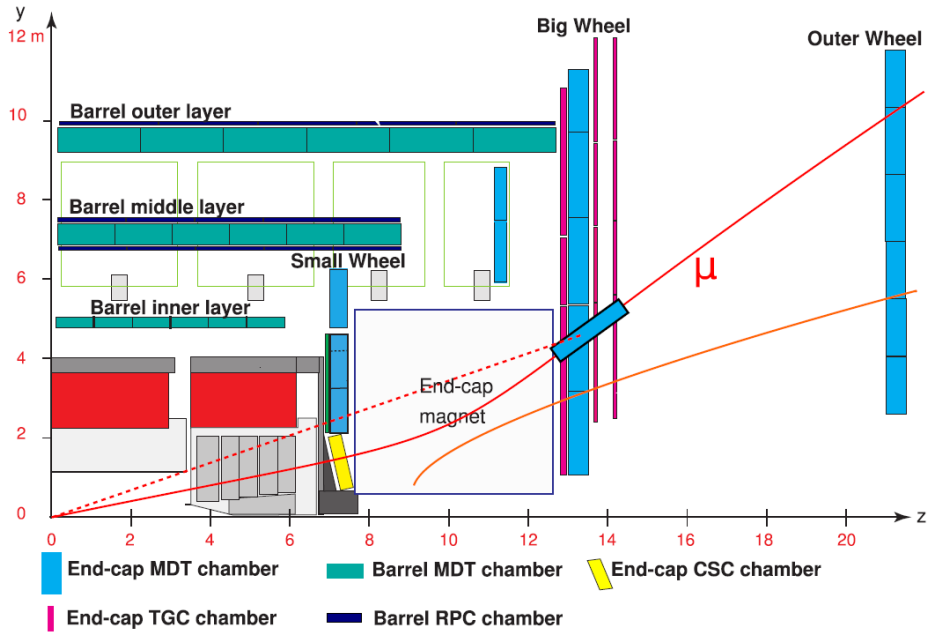
Introduction

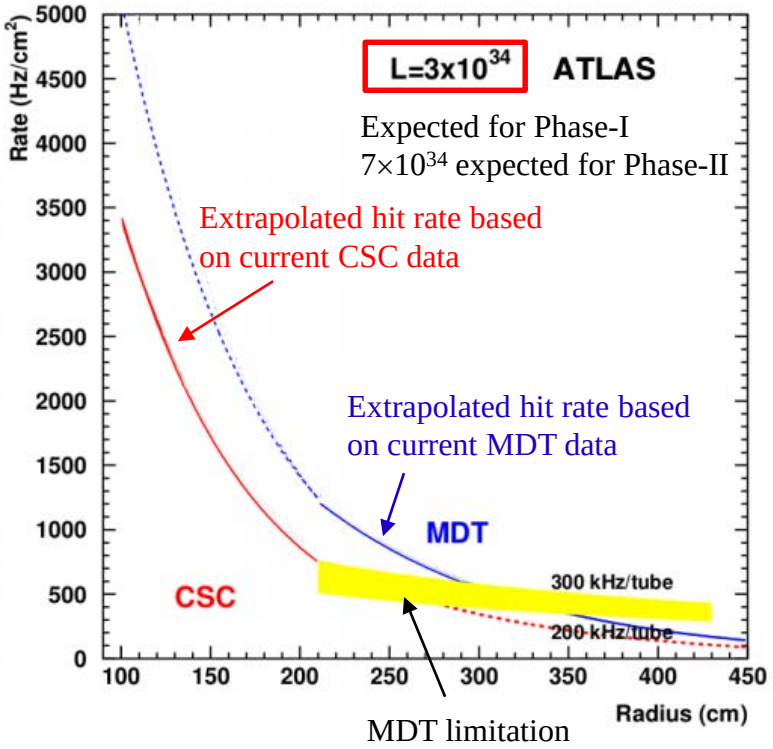
- ATLAS has the world's biggest muon spectrometer and can measure muon p_T with a resolution of 10% at 1 TeV
  - Precision tracking chambers: MDT for $|\eta|<2.5$, CSC for $2.5<|\eta|<2.7$ in SW
  - Trigger chambers: RPC in the barrel, TGC in the endcap



Introduction

- Problems with the current spectrometer in the endcap:
  - LV1 muon triggers rely on the BW TGC → most muons found at LV1 are fake
  - Large hit rate expected at the HL-LHC → low MDT hit and track segment efficiencies

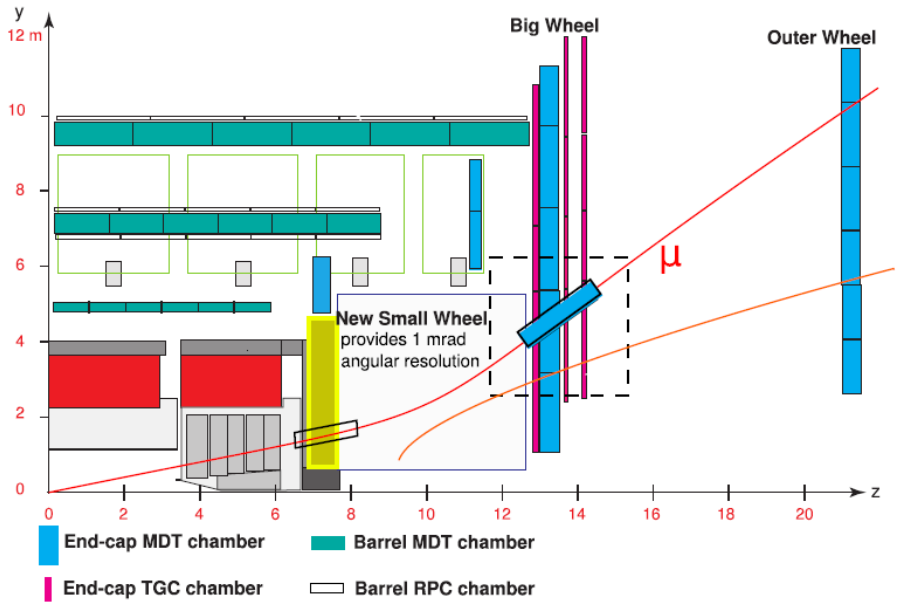


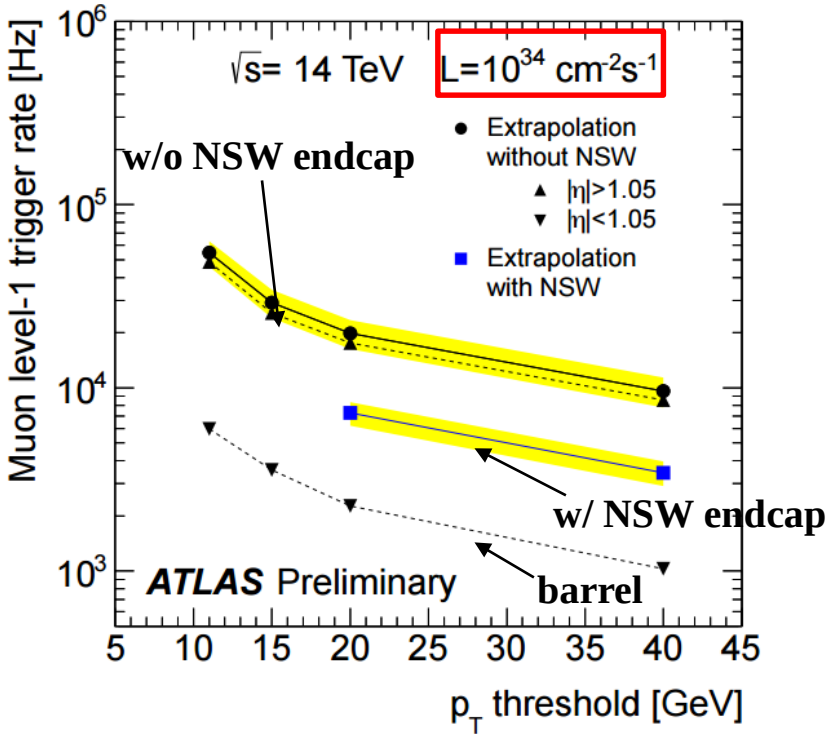


- About 90% of muons found by L1_MU11 do not have matched offline muons

New Small Wheel

- Replace the present SW detector with a NSW detector for the Phase-I upgrade
  - Provide a segment measurement at NSW with an angular resolution of 1 mrad
  - Replace MDT+TGC with MM+sTGC that can work at 15 kHz/cm^2

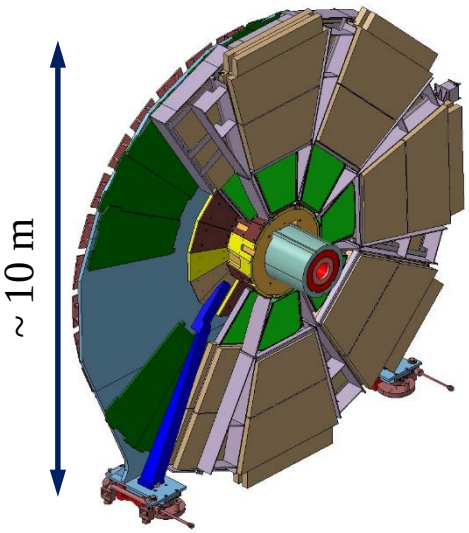


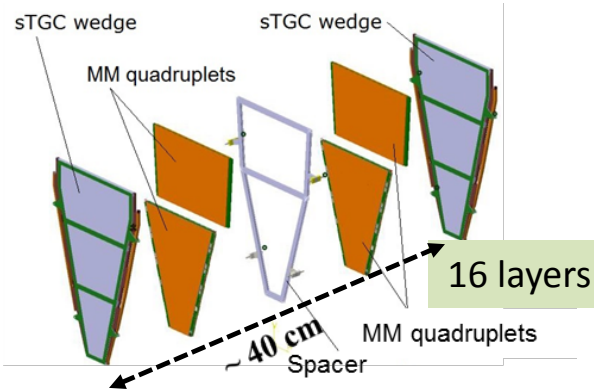


- Accurate online segment measurements at NSW together with BW segments to eliminate non-IP originating backgrounds

New Small Wheel Technologies

- Micromesh Gaseous Structure Detector, Micromegas (MM)
- Small-strip Thin Gap Chamber (sTGC)

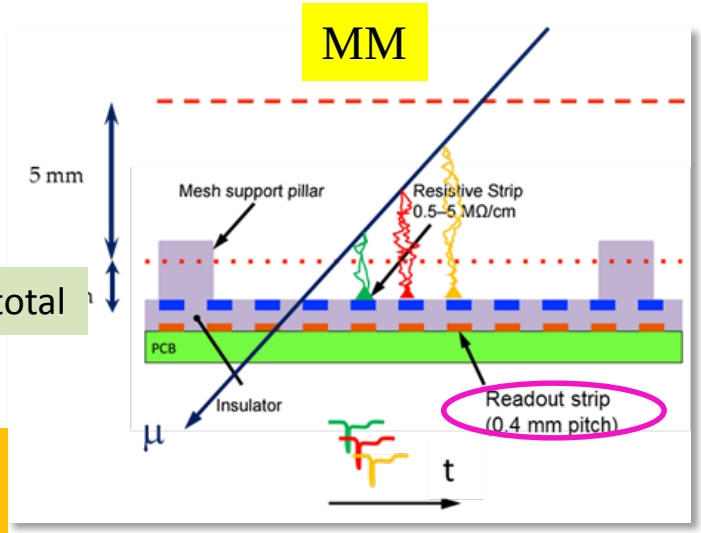


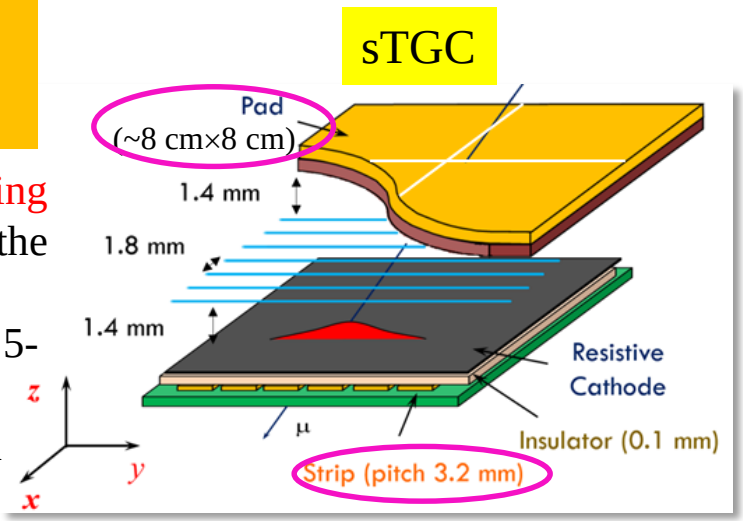


16 layers in total

Readout channels:
- MM: ~ 2.1 M
- sTGC: 280k (strip) + 46k (pads) + 28k (wires) = 354k

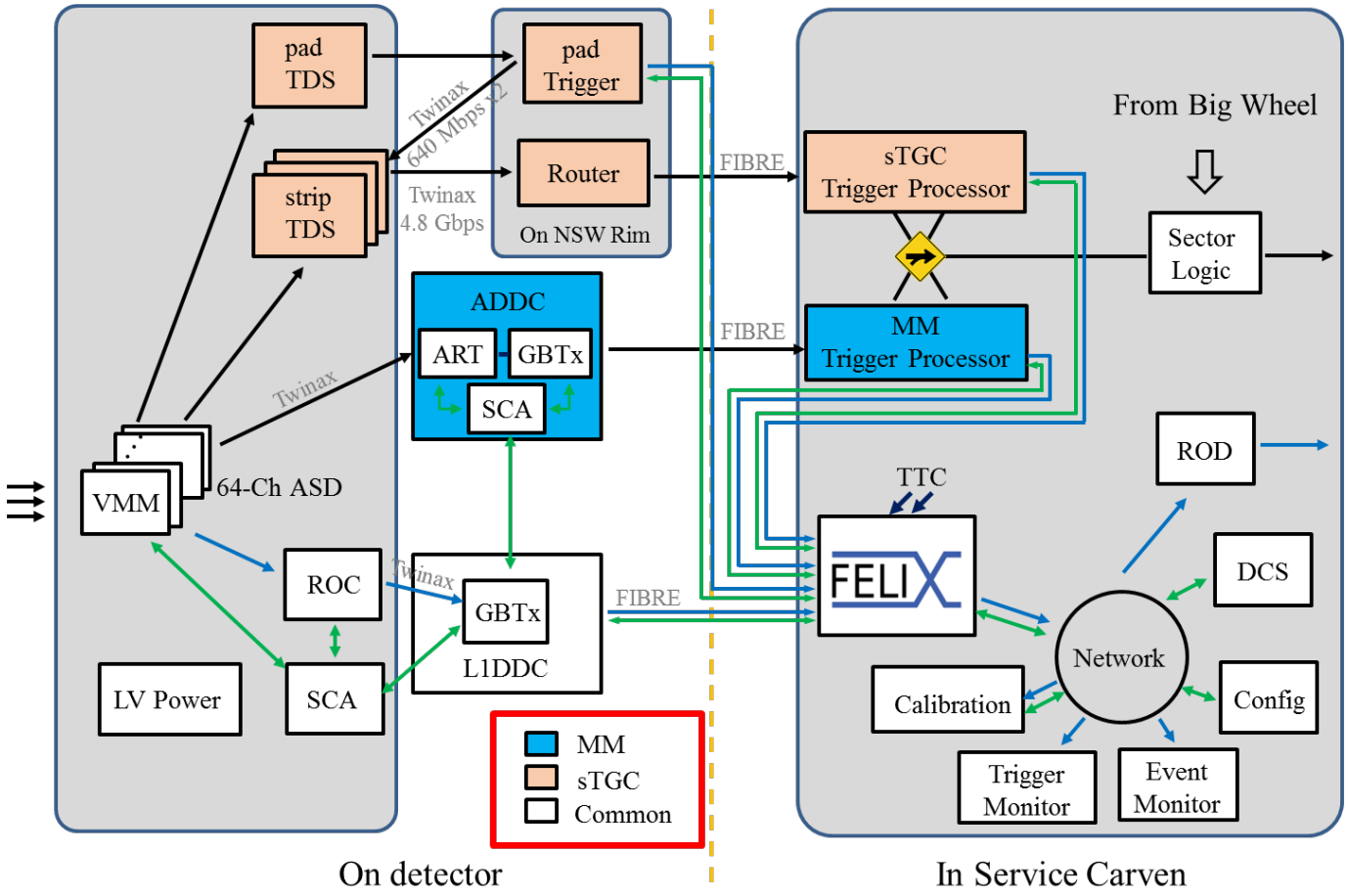
~50 kW for frontend electronics





- Both detectors will be used for trigger and precision tracking
  - MM trigger: use the first arriving strip to determine the hit position
  - sTGC trigger: use centroid-finding for charges from 5-7 strips to determine the hit position
  - Precision tracking: precision charge readout from all fired strips for both detectors

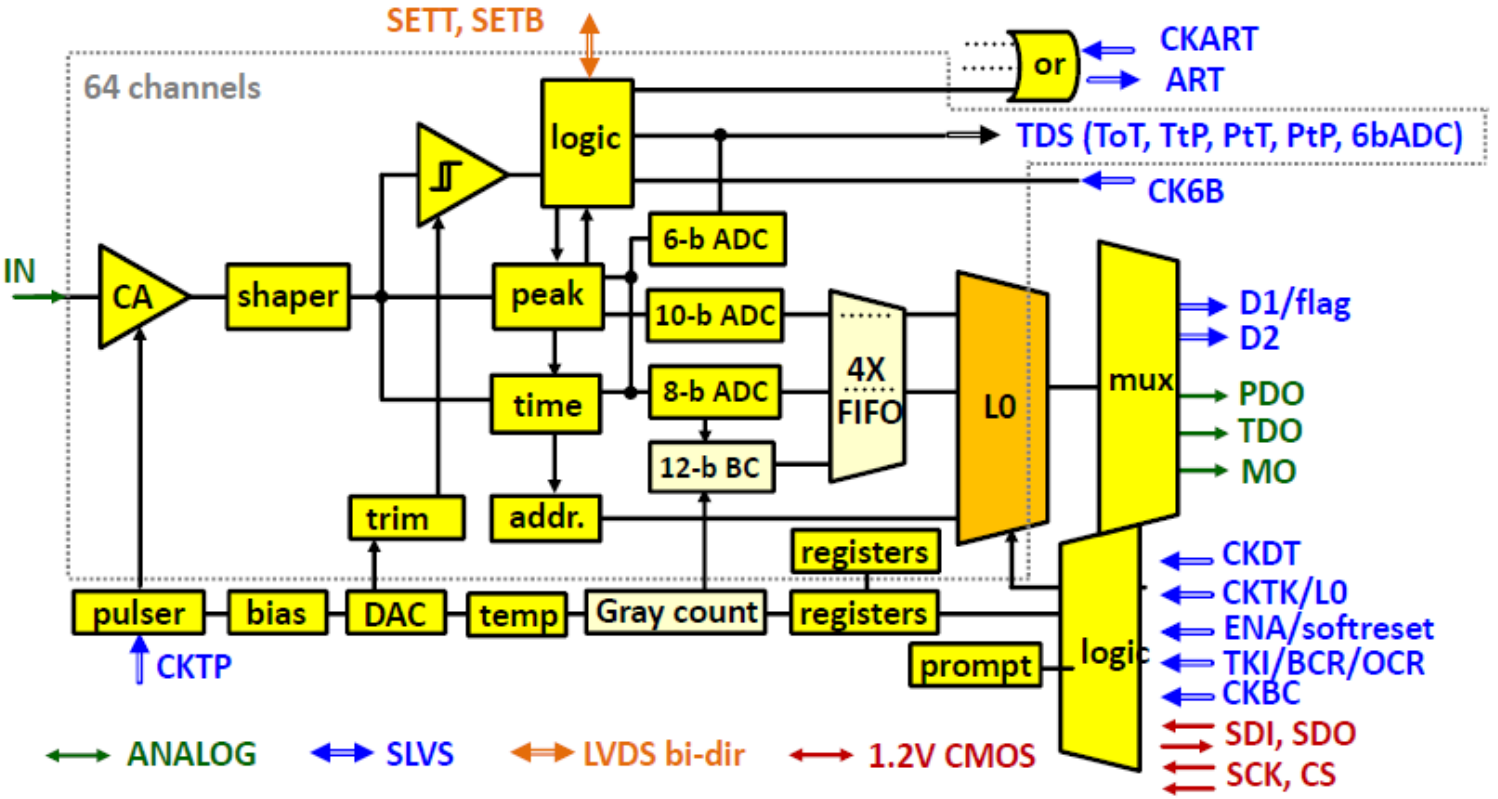
NSW Trigger and Readout



- 4 custom ASICs: VMM, ROC, TDS, ART
- 4 custom on-detector boards: L1DDC, ADDC, MM FEB, sTGC FEB,
- 2 custom on-rim boards: pad trigger, router (plus a GBT board for configuration)
- 2 custom on-USA15 boards: sTGC trigger processor, MM trigger processor

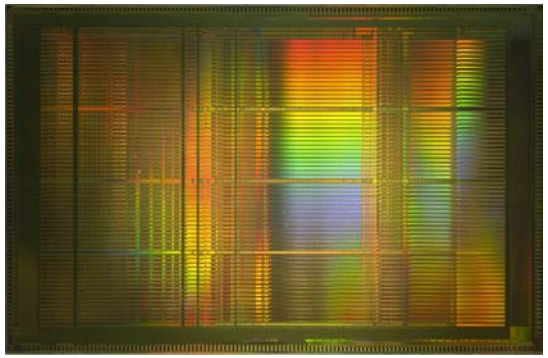
VMM

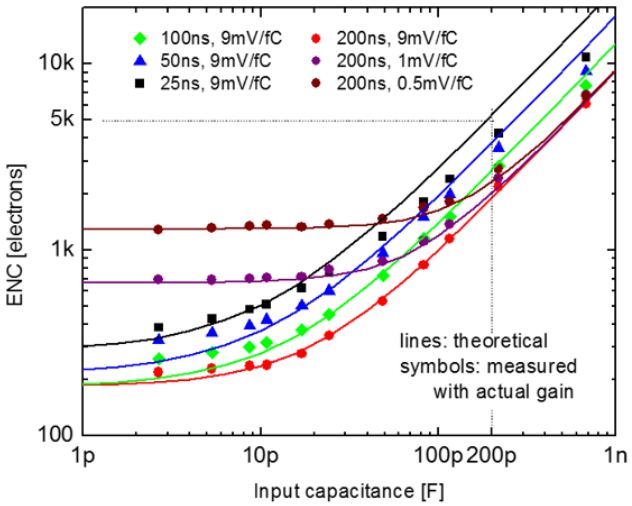
- The VMM is the common frontend ASIC for both MM and sTGC (pad, strip, wire)
- It provides amplification, shaping, peak height measurement and timing functionality

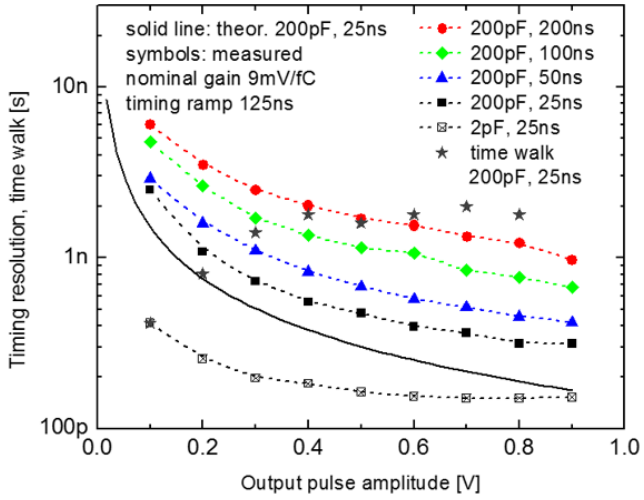


- Adjustable peaking time (25-200 ns), gain (0.5-16 mV/fC), polarity, and input capacitance (sub-pF to nF)
- Four modes: two-phase analog (not used in NSW), continuous digital, direct readout, and ART

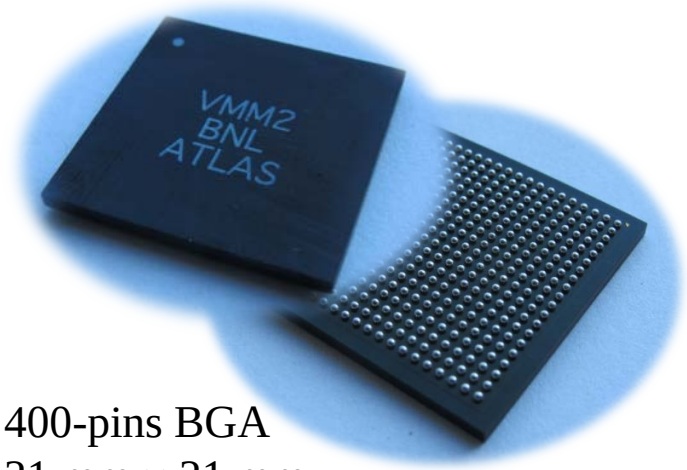
VMM







VMM2 (2014)
115 mm², > 5M MOSFETs (>80k/ch.)

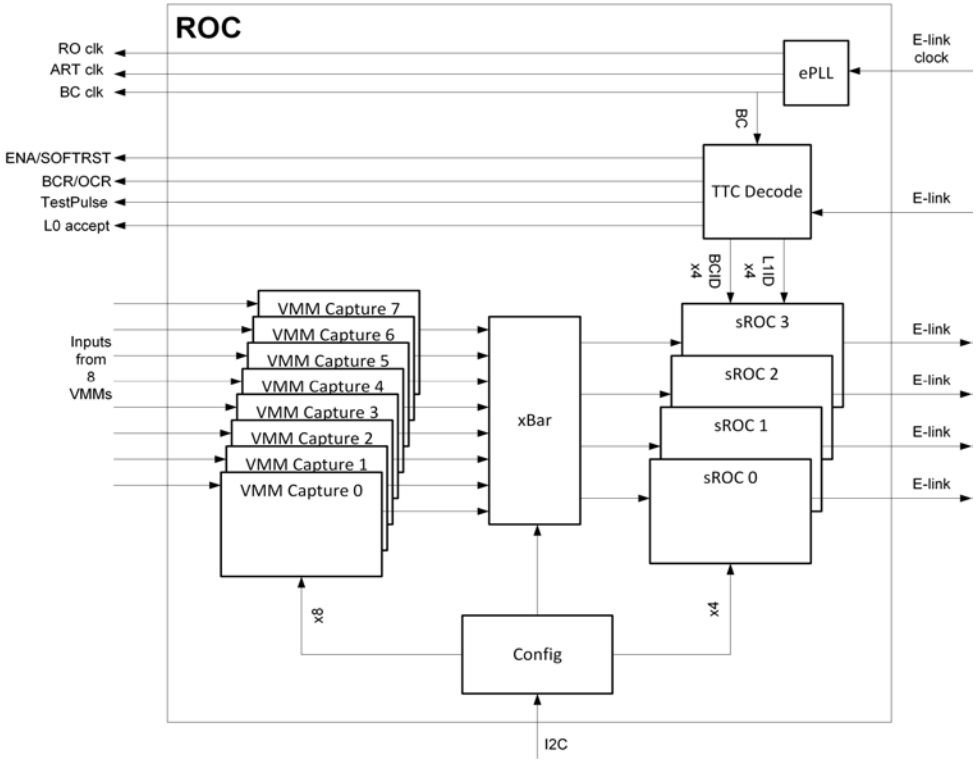


400-pins BGA
21 mm × 21 mm

VMM3, 130 mm², > 6M MOSFETs
To be submitted this March

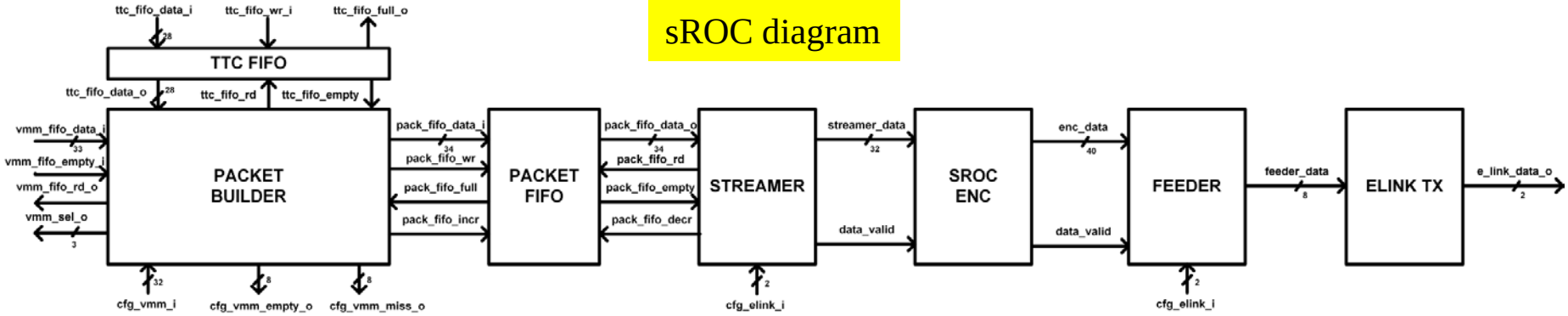
- L0 handling, SEU-tolerant, deeply revised front-end for sTGC signals, SLVS IOs, various additional functions, various fixes
- input from many collaborators with a broad range of expertise

Common Readout: Read Out Controller



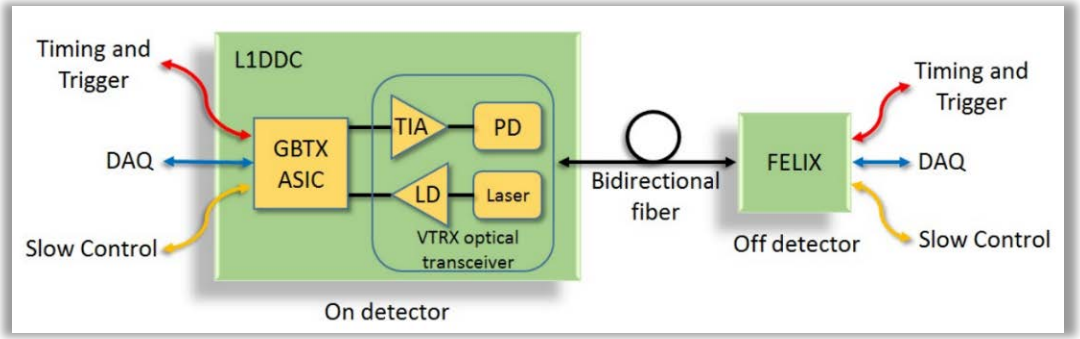
- Responsible for the precision readout after L1A
- Compatible with Phase-II upgrade:
  - Input packet rate: 1 MHz
  - Mean packet length: 20 hits
  - Trigger rate: 400 kHz
  - Trigger latency: 60 us
  - E-Link output rate: 320 Mbps
- To be submitted this May

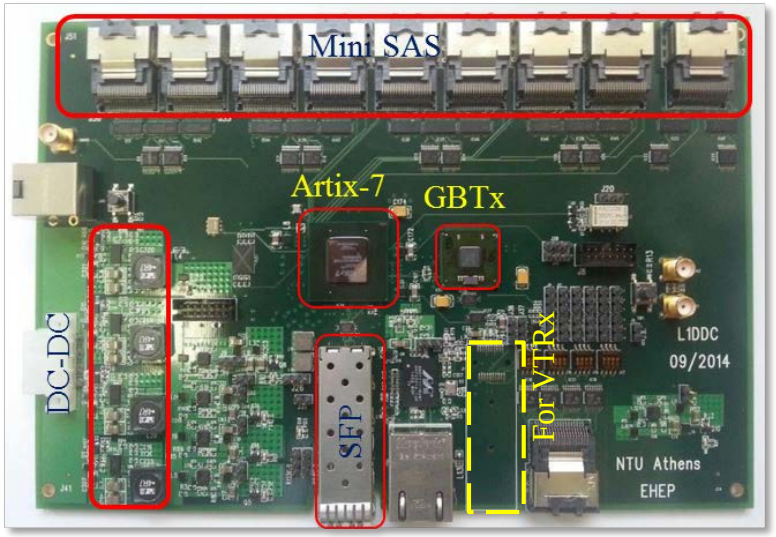
sROC diagram



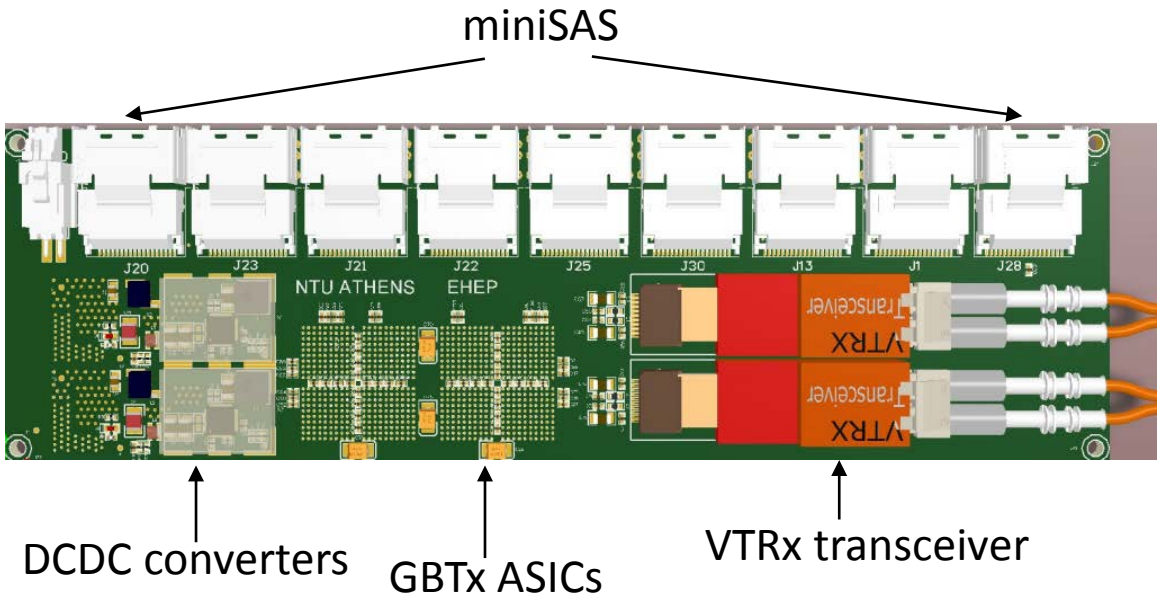
Common Readout: L1 Data Driver Card

- L1DDC: aggregates and transmits L1 readout data from FEBs to FELIX; also used for TTC distribution and config./monitoring





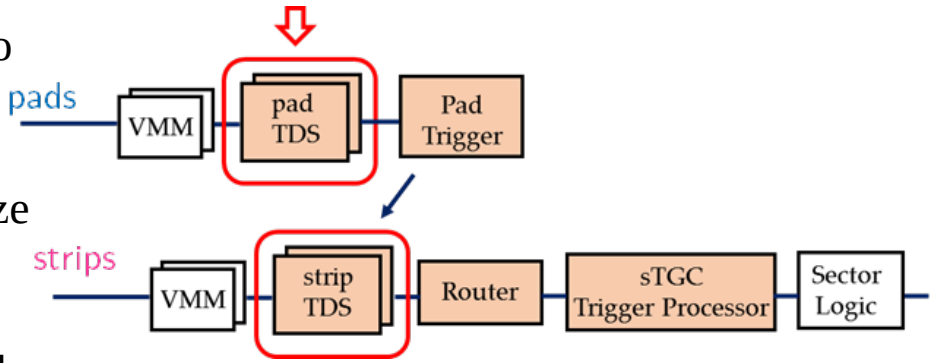
L1DDC v1 board



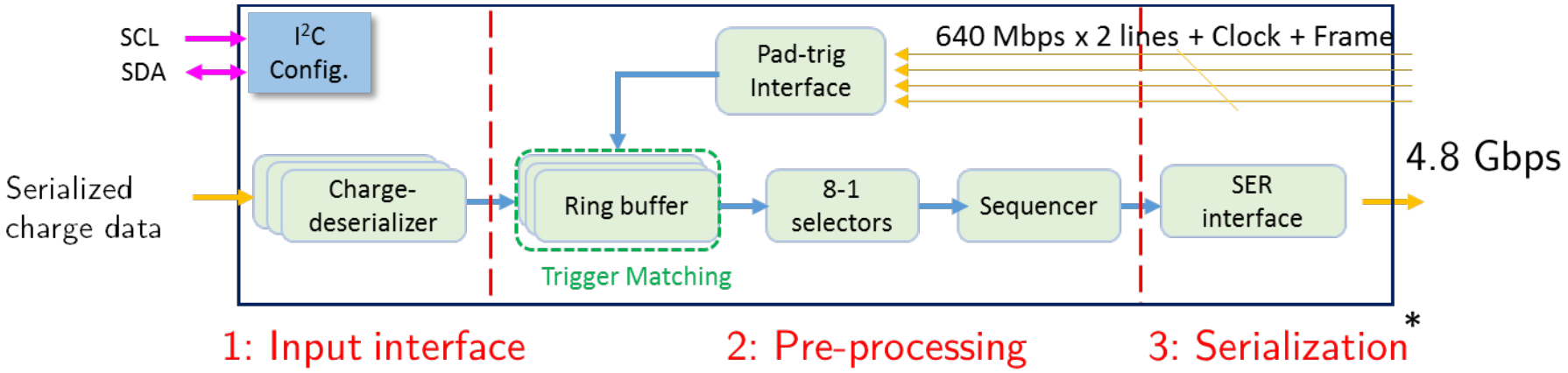
- Implement with GBTx, VTRx and FPGA
- Link with miniSAS verified
- GBTx configuration firmware developed

sTGC trigger: Trigger Data Serializer

- Two operation modes:
  - Pad-TDS: send each pad firing status to pad trigger
  - Strip-TDS: prepare strip trigger data, perform pad-strip matching and serialize the charge for strips in the ROI
- Output data rate: 4.8 Gbps
- Low and fixed latency needed (40 ns for pad-TDS and 75 ns for strip-TDS)
- Radiation tolerant
- 128 channels with individual programmable delay (pad-mode only)



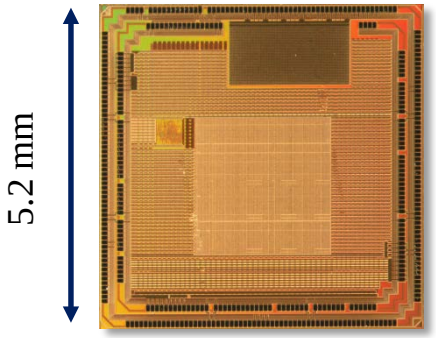
Strip-TDS block diagram



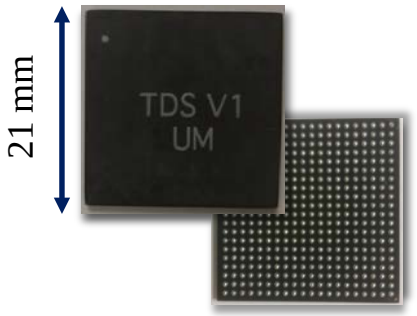
sTGC trigger: Trigger Data Serializer

- IBM 8RF-DM 323, 130 nm CMOS, 1.5 V
- Die size: 5.2×5.2 mm^2 with >3M transistors
- 400-pins BGA package (21×21 mm^2)
- All logics verified and excellent serializer performance obtained

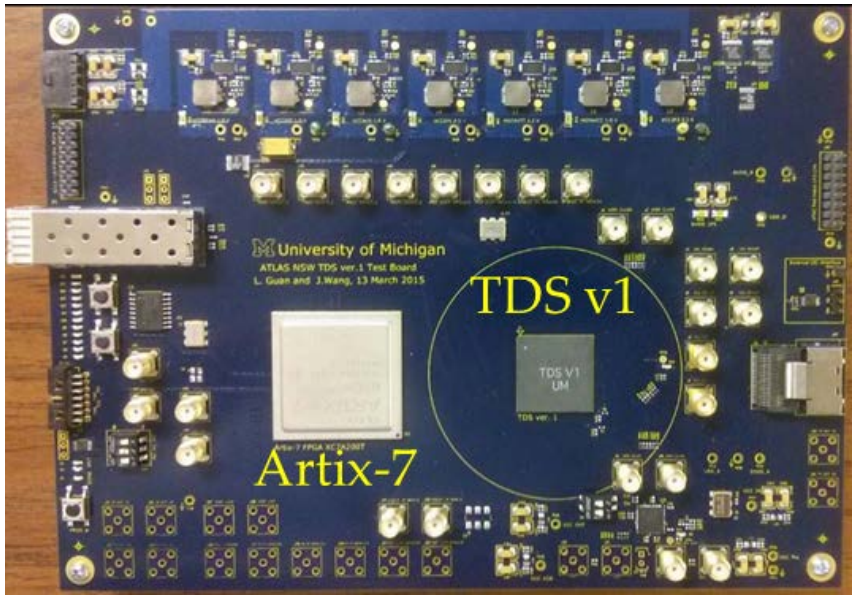
TDS v1 silicon die



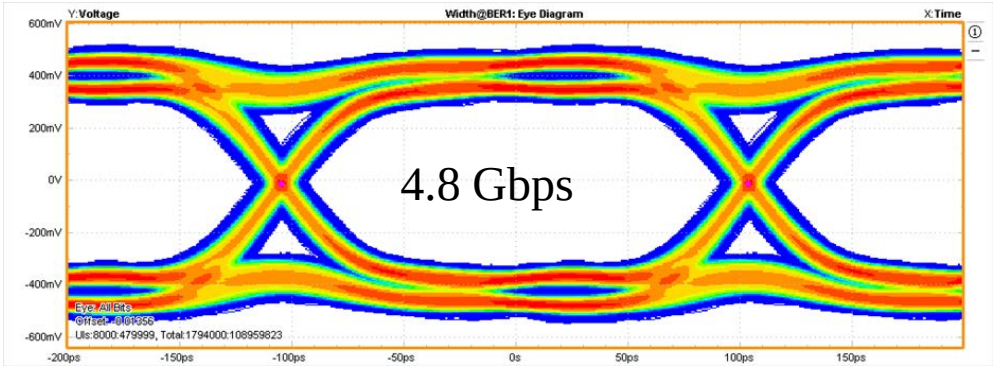
ASIC package



TDS v1 test board



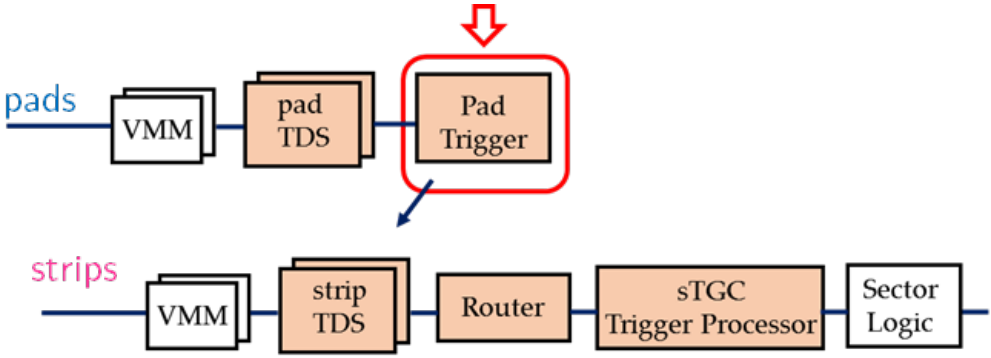
TDS eye diagram

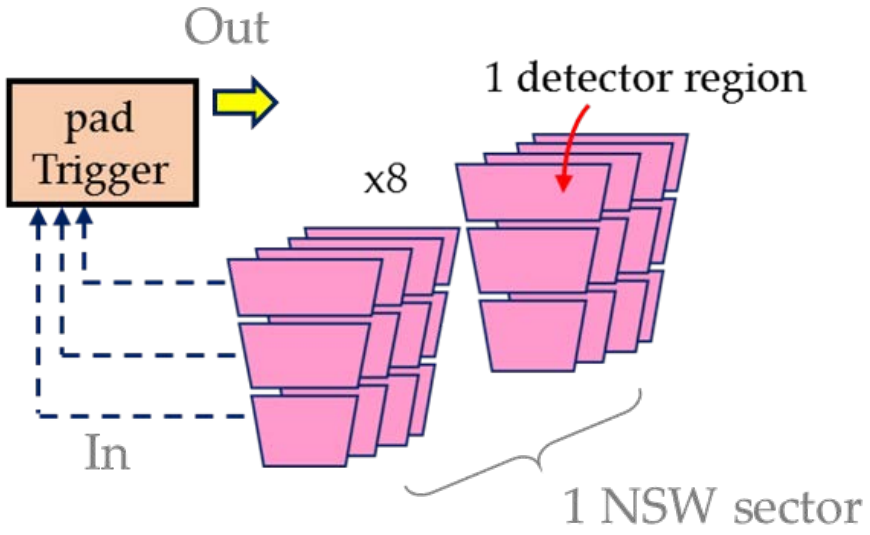


- TDS V2 prototype submitted and will have a joint production with VMM3

sTGC trigger: Pad Trigger Board

- Receive pad firing information from all eight layers
- Perform two 3-out-of-4 pad coincidences per BC to form pad trigger road (tag BCID and define strip band to be read out)
- Send up to 3 trigger candidates (RoI) per sector per BC to strip-TDS
- Send pad firing information after L1A for monitoring

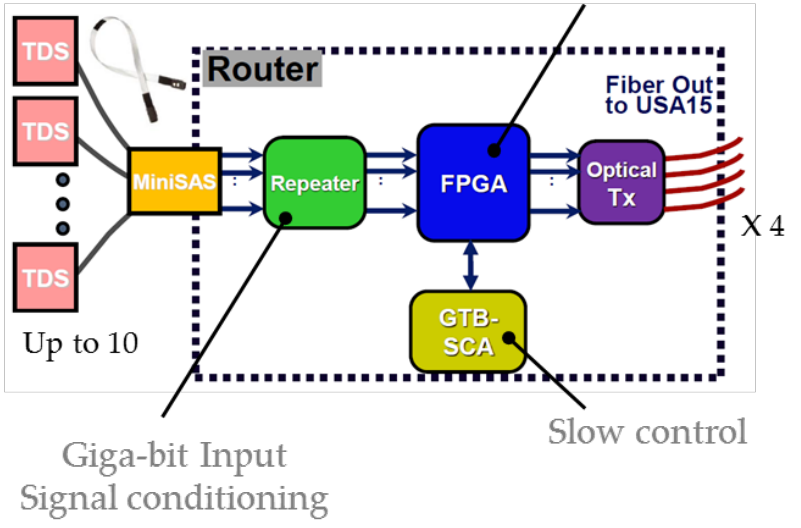


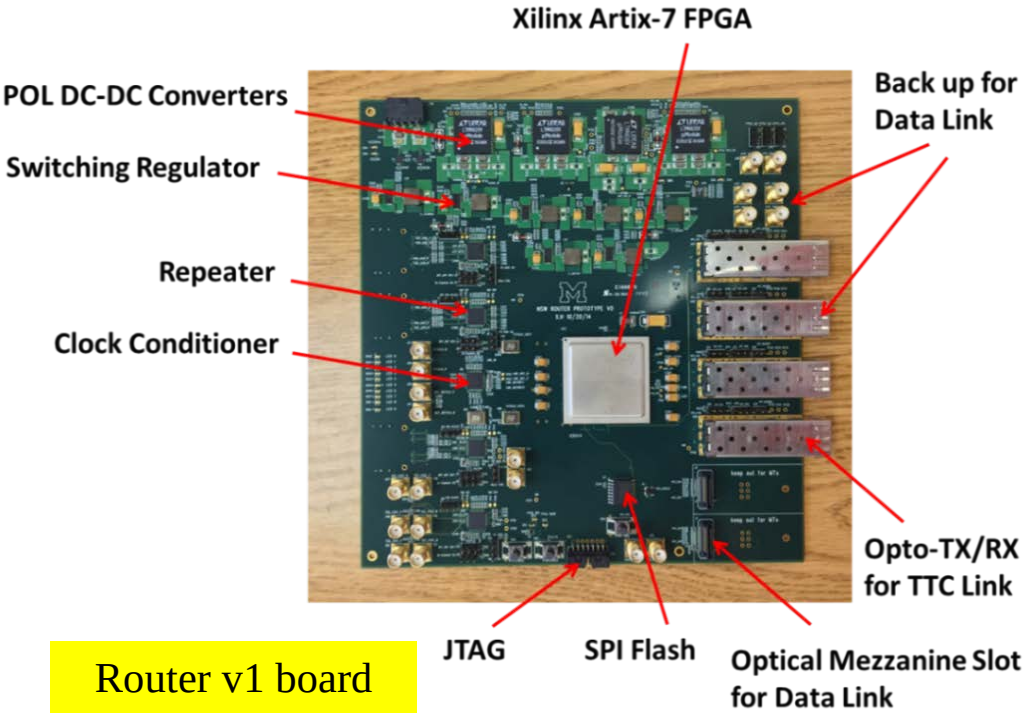


sTGC trigger: Router

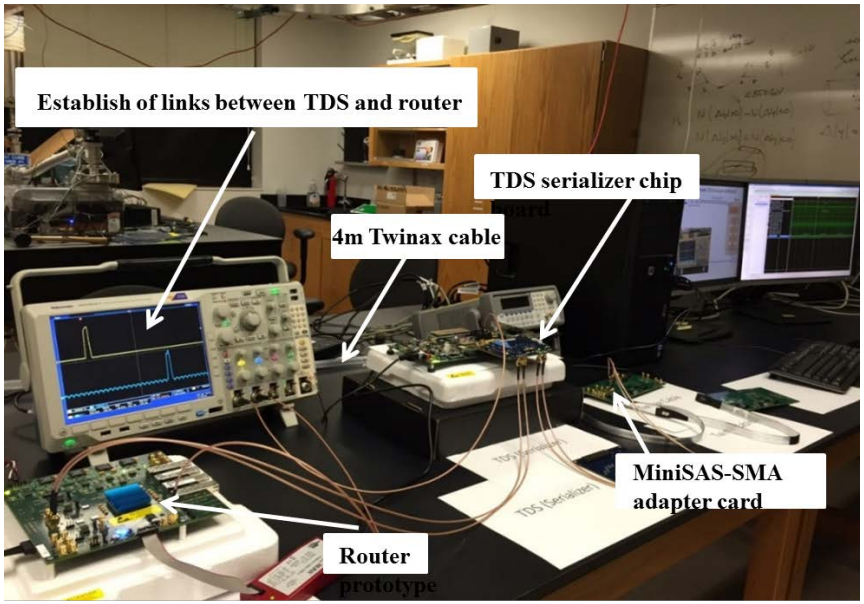
- Collect data from up to 10 TDSs, drop NULL packets and transmit data to sTGC trigger processor via optical fibers
- Low and fixed latency
- High speed stable links
- Radiation tolerant

Baseline: Artix-7



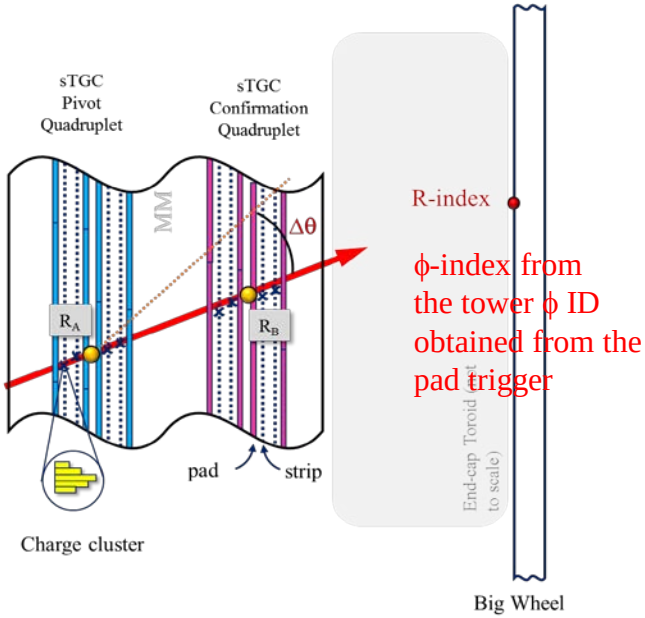


Router v1 board

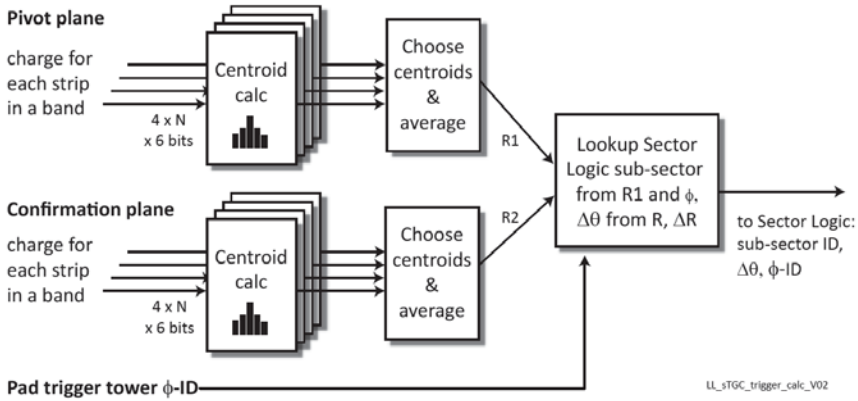


sTGC trigger: Trigger Processor

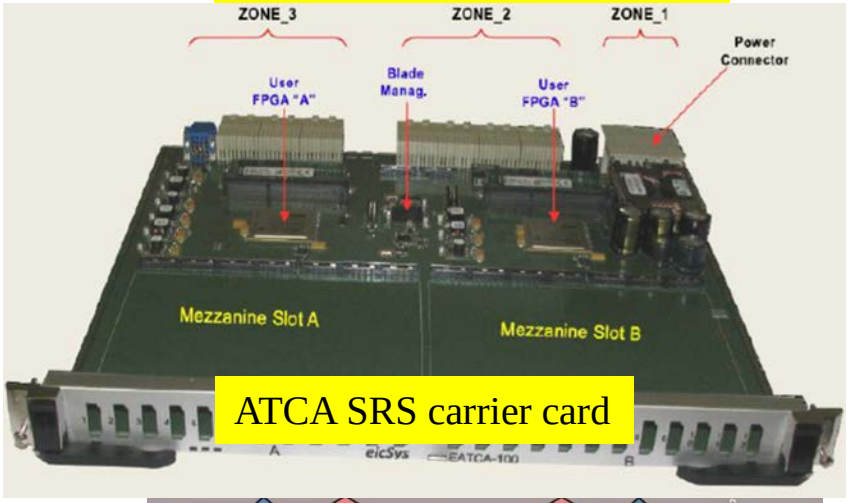
- Receive strip data from the Router, perform cluster centroid finding for both quadruplets, and determine the segment pointing direction

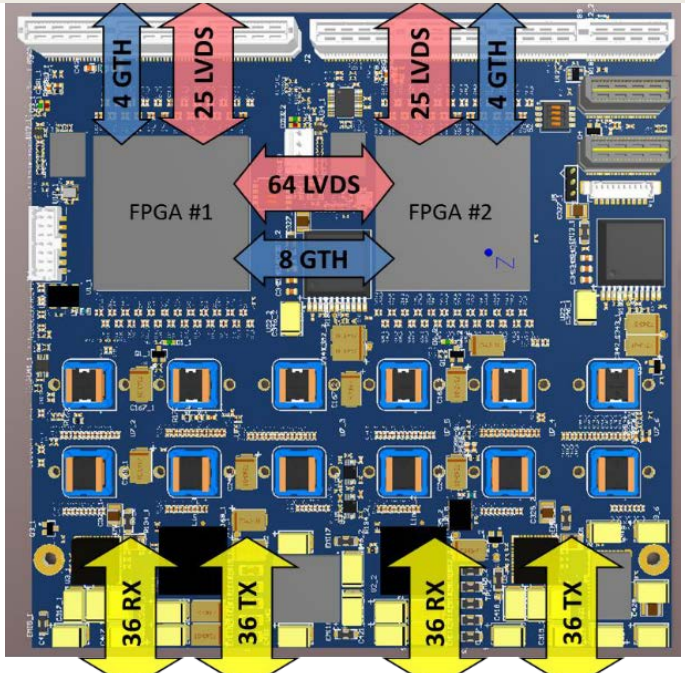


ϕ-index from the tower ϕ ID obtained from the pad trigger



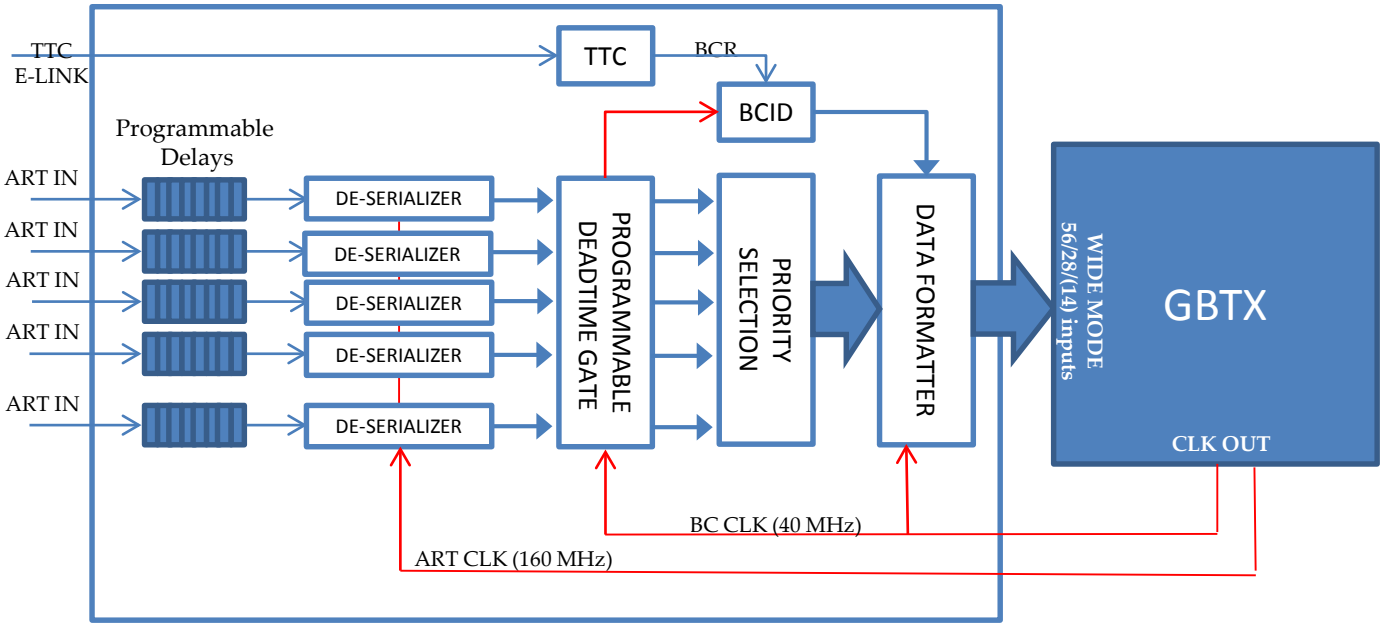
Common sTGC/MM trigger processor board

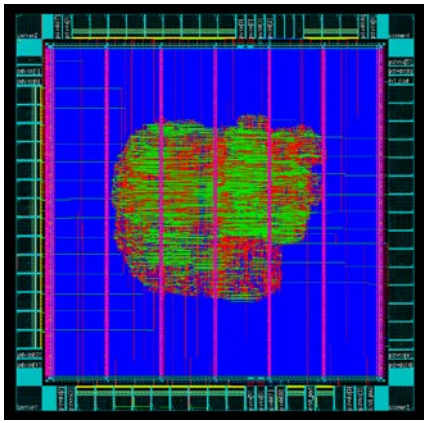




MM trigger: Address in Real Time

- >2M readout channels for MM, hard to use all of them at LV1
- Fine pitch (~0.5 mm), use the first threshold-crossing strip
- Each ART ASIC encodes up to 8 addresses in real time from up to 32 VMMs and transmits them synchronously to the MM trigger processor



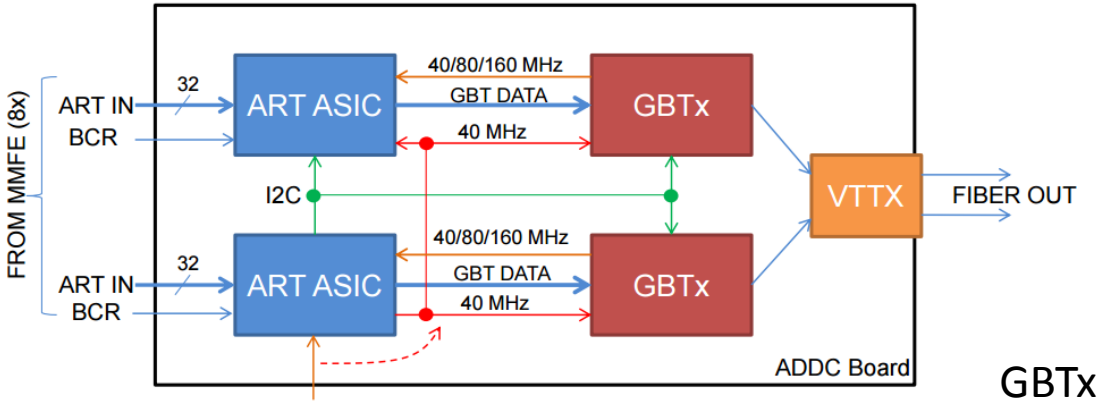


- Core: ~ 1.8 x 1.8 mm^2
- Die: 3.5 x 3.5 mm^2
- To be submitted this May

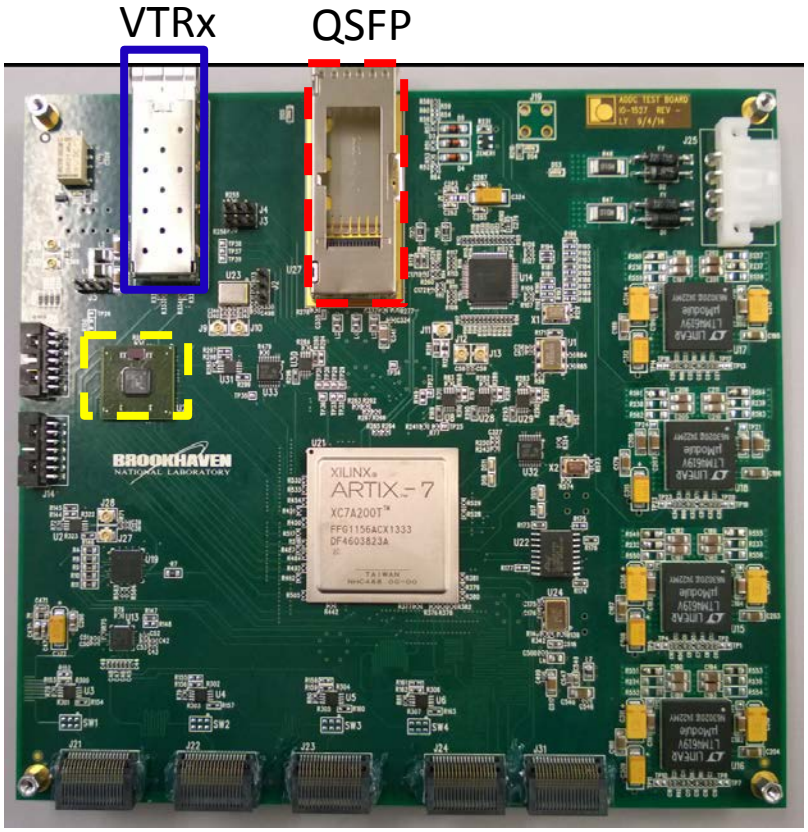
Block	Description
Programmable delays	Adjust input signal phase to avoid FF violations due to delay on cables
ART De-Serializers	Recover 6-bit ART data from ART stream
Programmable deadtime Gate	Temporarily (few BC) mask VMM channels after a hit.

Block	Description
Hit Selection	Priority-based hit selection. Selects up to 8 hits from 32.
TTC Block	Recover BCR from TTC stream
BCID Counter	Generate internal BCID
Output Format	Format data for GBTx transmission

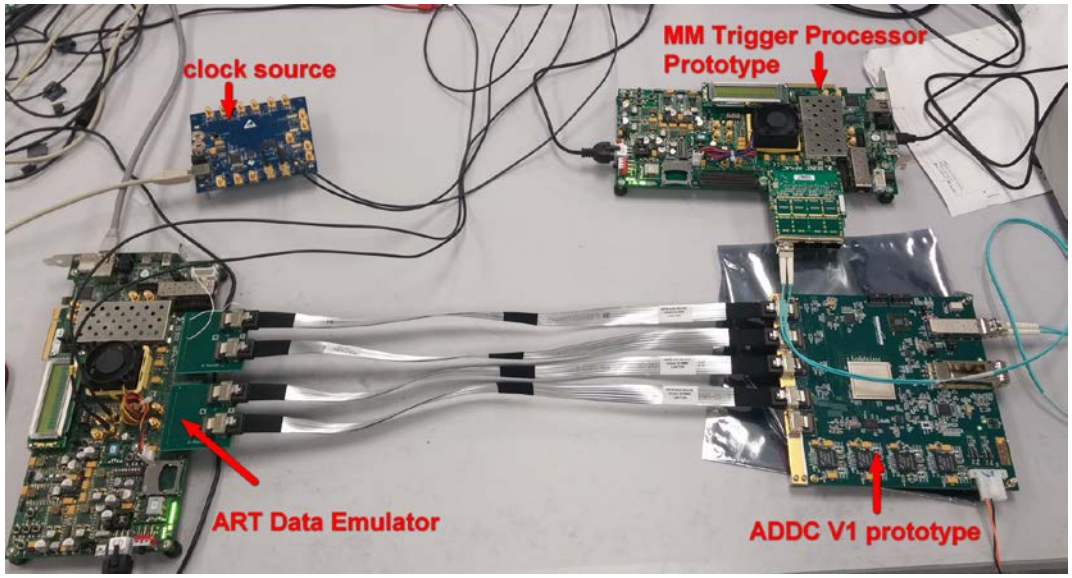
MM trigger: ART Data Driver Card



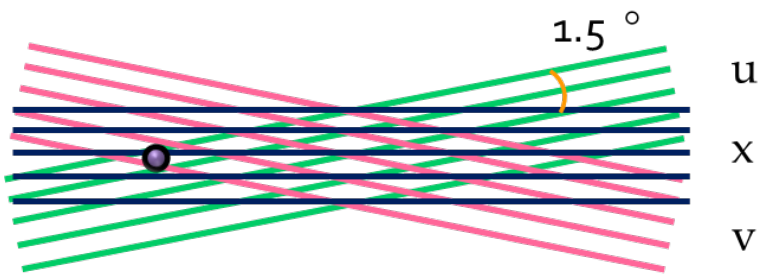
e-link @ 80Mbps from L1DDC



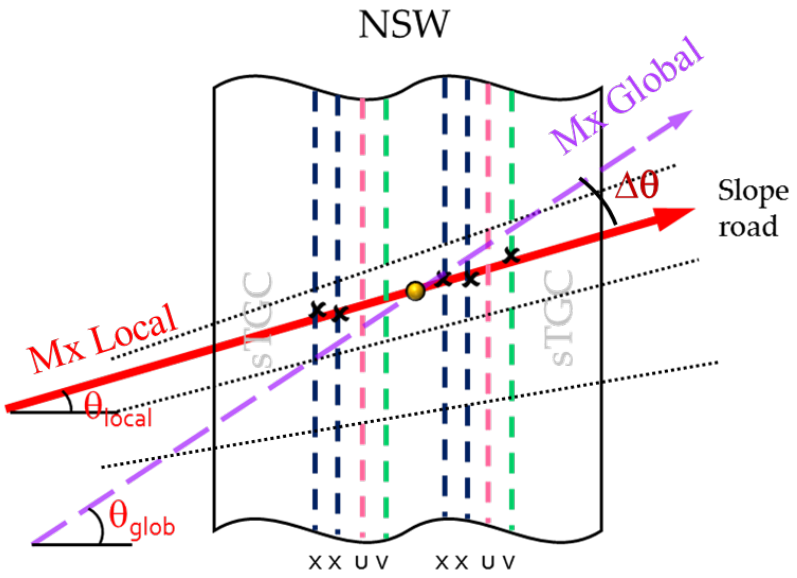
ADDC v1 board



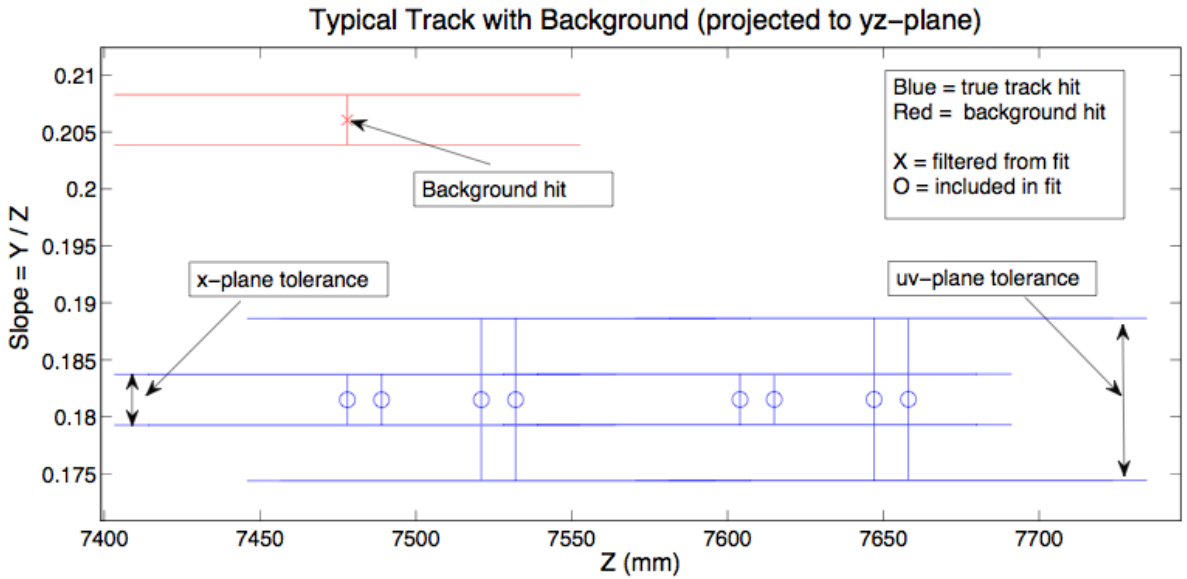
MM trigger: Trigger Processor



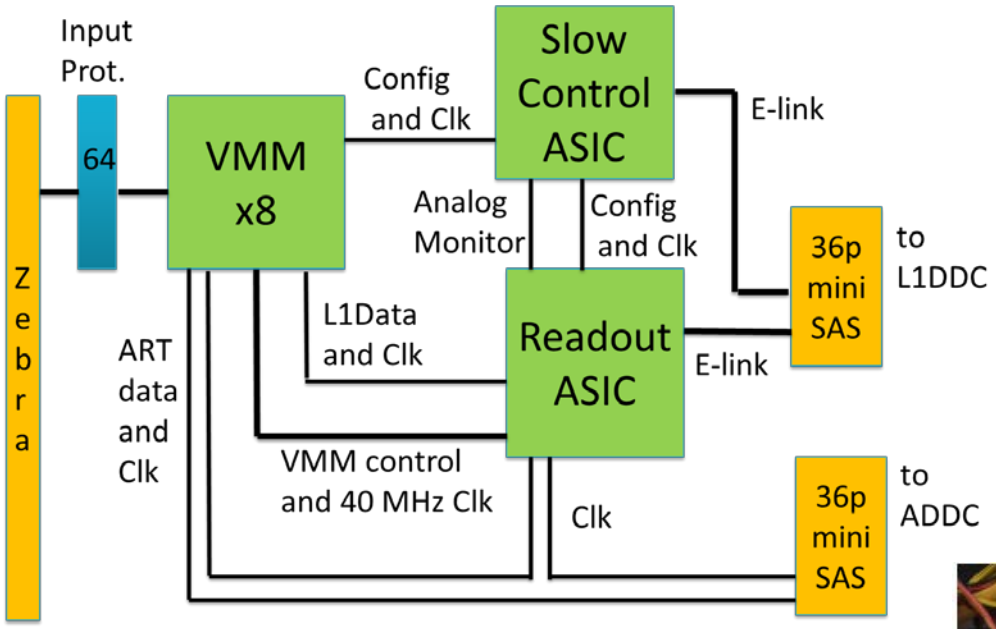
x: horizontal strip (2 plans per quad.)
u,v: stereo strip (1 each per quad.)



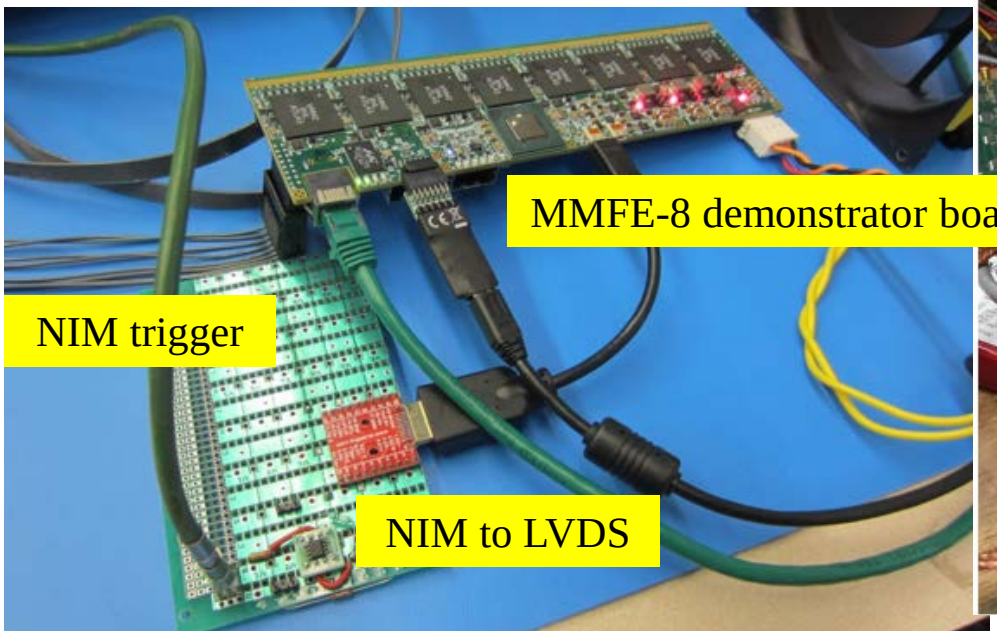
- Projective roads to IP (hit→slope)
- X-roads narrower, u-v (stereo) wider
- A segment is multi-layer coincidence within a slope road

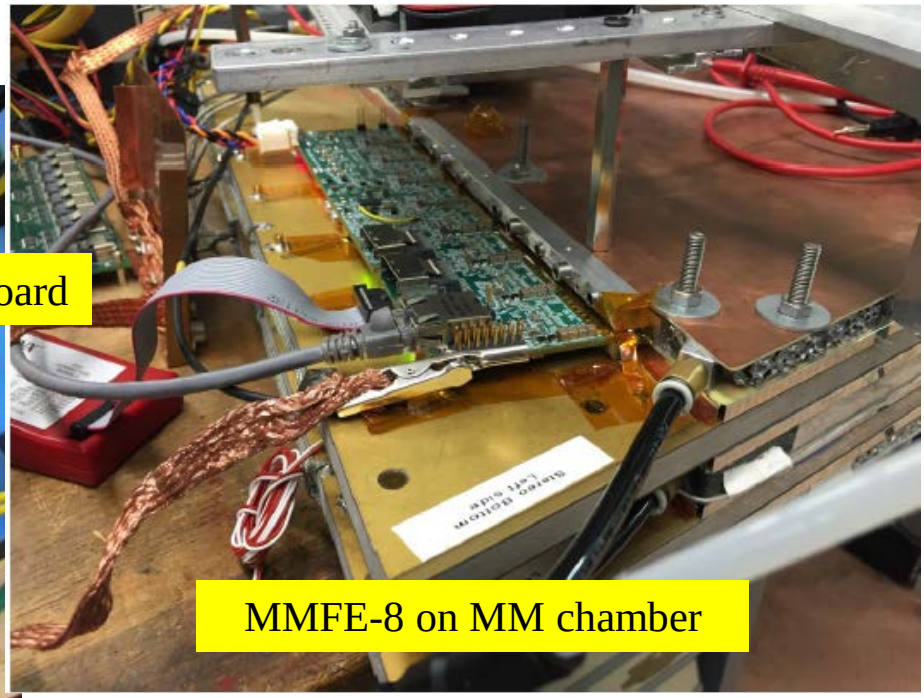


MM FEB

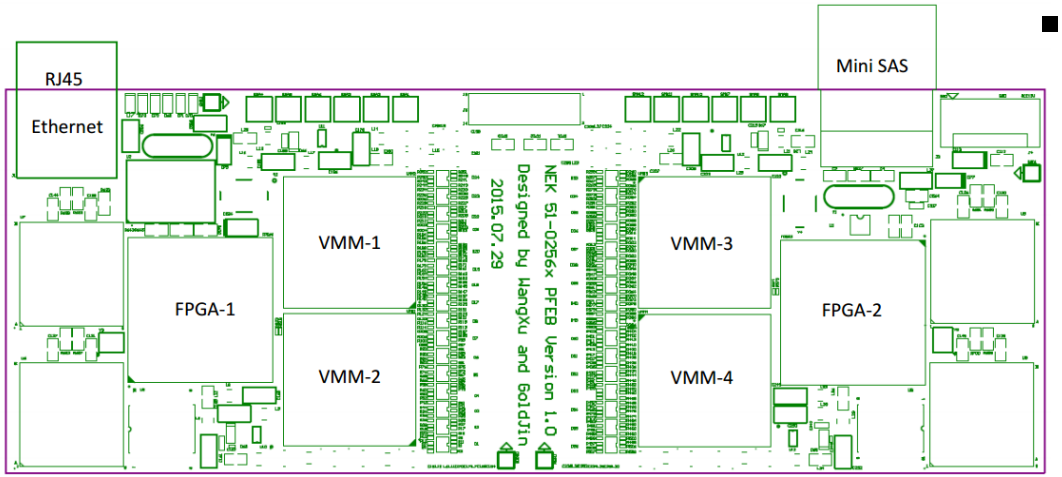


- Per MM FEB:
  - ✓ 8 x 64 VMM channels
  - ✓ 8 x 6 bit address of ART data
  - ✓ L1A readout via two e-links @ (up to) 320 Mb/s
  - ✓ ~8W of power
  - ✓ 5 cm × 18 cm

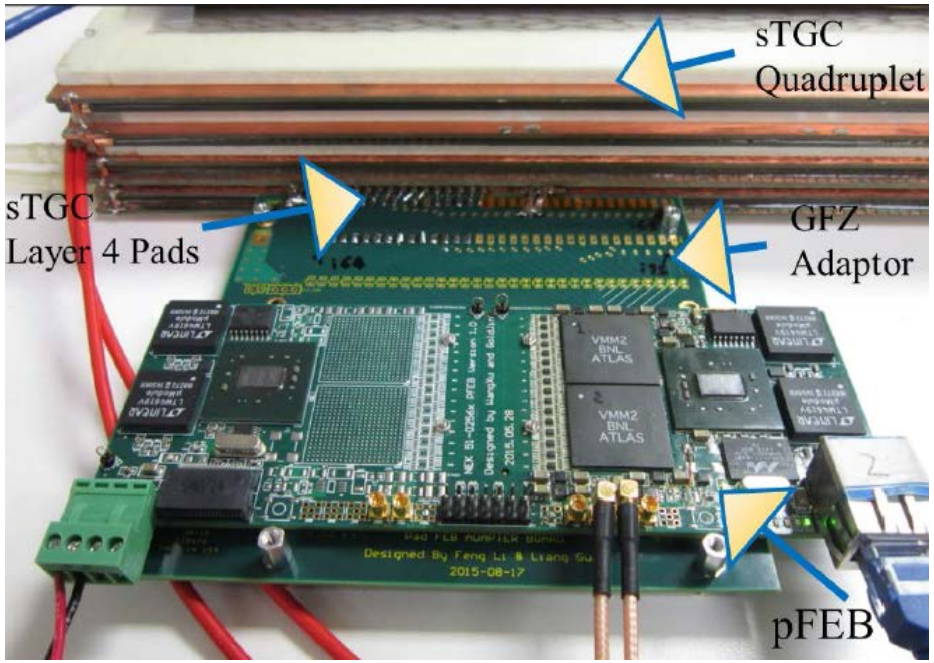


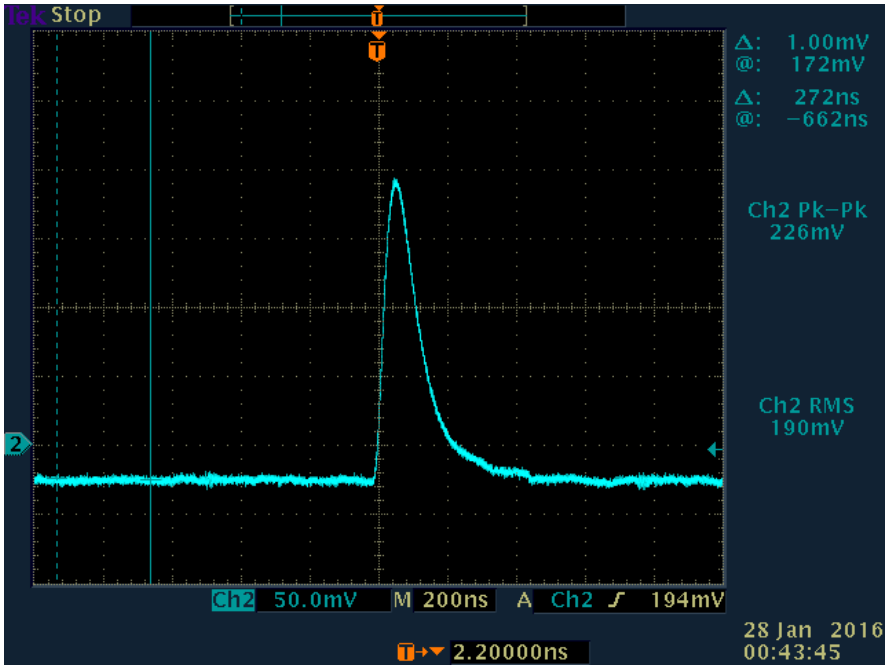


sTGC FEB



- Per sTGC FEB:
  - ✓ 7(3) x 64 VMM channels
  - ✓ 4(1) x 128 TDS channels
  - ✓ L1A readout via two e-links @ (up to) 320 Mb/s
  - ✓ ~10W of power
  - ✓ 5 cm × 18 cm





Conclusions

- The NSW upgrade is necessary for ATLAS to improve the LV1 muon trigger and maintain precision tracking capability at high luminosity
- Separate trigger strategies for two sub-detector systems have been developed, taking into account substantial readout and geometry differences
- Advance development of both detectors and trigger/readout electronics
- Significant effort have been made in the design of various trigger electronics in order to fit within the tight Phase-I latency budget
- A vertical slice of the MM/sTGC detector is under preparation and will be used to test and integrate all NSW electronics