Developments for serial power applications

Laura Gonella

Report on RD53 powering working group

ACES workshop

08/03/2016

Introduction

- R&D on serial powering ongoing for more than 10 years in ATLAS

- Leading institutes
  - Uni Bonn for pixels
  - RAL, UPenn, BNL for strips

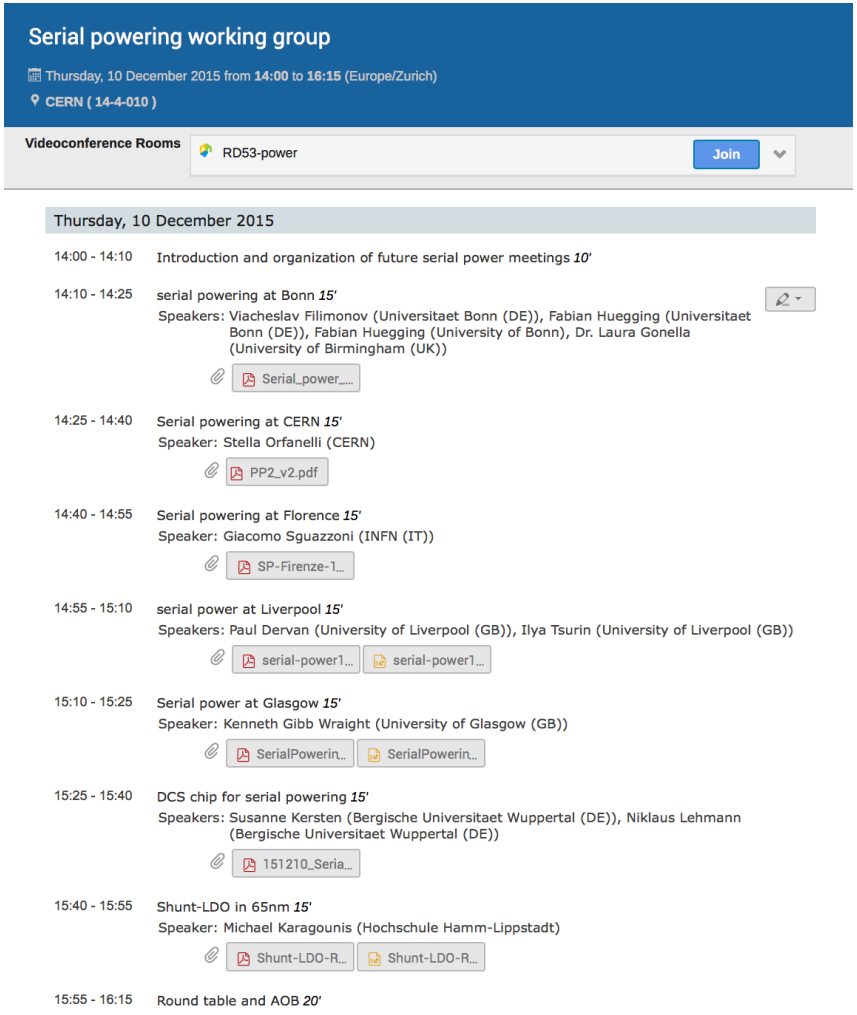
- Serial powering proven to be a feasible and reliable powering scheme for trackers at the HL-LHC

- The current scalability brings significant advantages in terms of material reduction and power efficiency

→ Serial powering is the baseline powering scheme for pixel detectors at the HL-LHC (ATLAS and CMS)

RD53 powering working group

- RD53 established a powering working group in 2015
- Main focus of the group is twofold
  - Input and discussions with chip designers about powering aspects for the future pixel chips in 65nm
  - Exchange of experiences and concepts with powering schemes between the different experiments, esp. serial powering but not exclusively
- Meetings are quarterly
  - 2 meetings in 2015 plus a special meeting on serial powering simulations in 2016



Serial powering working group

Thursday, 10 December 2015 from **14:00** to **16:15** (Europe/Zurich)

CERN (14-4-010)

Videoconference Rooms: RD53-power — Join

Thursday, 10 December 2015

14:00 - 14:10 Introduction and organization of future serial power meetings *10'*

14:10 - 14:25 serial powering at Bonn *15'*
Speakers: Viacheslav Filimonov (Universitaet Bonn (DE)), Fabian Huegging (Universitaet Bonn (DE)), Fabian Huegging (University of Bonn), Dr. Laura Gonella (University of Birmingham (UK))
Serial_power_...

14:25 - 14:40 Serial powering at CERN *15'*
Speaker: Stella Orfanelli (CERN)
PP2_v2.pdf

14:40 - 14:55 Serial powering at Florence *15'*
Speaker: Giacomo Sguazzoni (INFN (IT))
SP-Firenze-1...

14:55 - 15:10 serial power at Liverpool *15'*
Speakers: Paul Dervan (University of Liverpool (GB)), Ilya Tsurin (University of Liverpool (GB))
serial-power1... serial-power1...

15:10 - 15:25 Serial power at Glasgow *15'*
Speaker: Kenneth Gibb Wraight (University of Glasgow (GB))
SerialPowerin... SerialPowerin...

15:25 - 15:40 DCS chip for serial powering *15'*
Speakers: Susanne Kersten (Bergische Universitaet Wuppertal (DE)), Niklaus Lehmann (Bergische Universitaet Wuppertal (DE))
151210_Seria...

15:40 - 15:55 Shunt-LDO in 65nm *15'*
Speaker: Michael Karagounis (Hochschule Hamm-Lippstadt)
Shunt-LDO-R... Shunt-LDO-R...

15:55 - 16:15 Round table and AOB *20'*

Serial powering configurations

- In module SP
  - Each module builds its own SP chain
  - Independent module power as in voltage based powering schemes
  - Number of chips in module defines the reduction factor n
  - Sensor connected to a few volts different ground
- Across module SP
  - SP chain made of n modules defined by design of local support structures (ATLAS pixels: up to n = 8 – 10)
  - Modules/sensors grounds differ inside the SP chain
  - Option investigated so far by ATLAS pixels

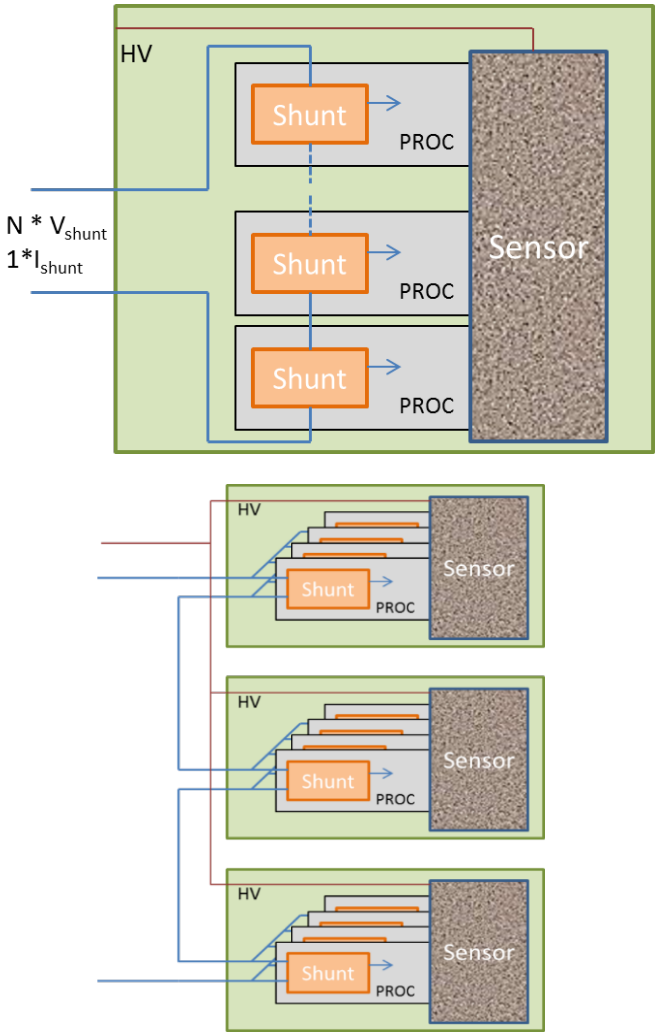
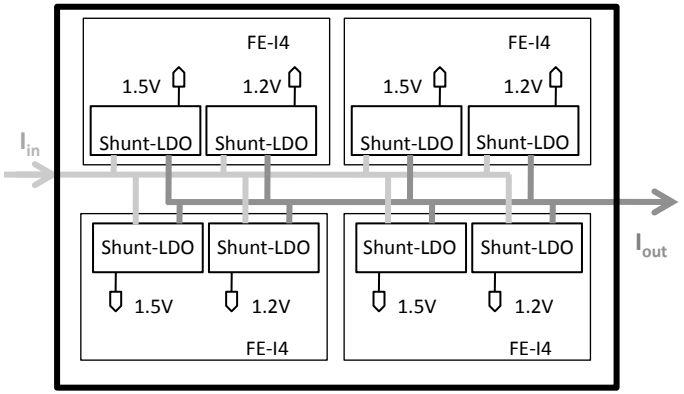


Figure from J. Christiansen

Enabling technologies

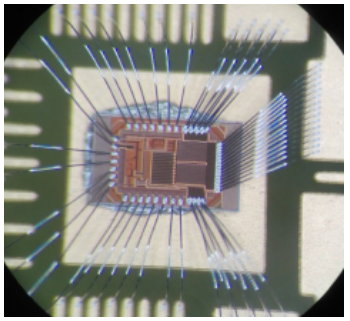
- Shunt-LDO regulator
  - 2 integrated in the FE-I4 chip
- Redundancy and module bypass
  - Parallel connection of all regulators on module
  - PSPP chip as part of DCS system
- AC-coupling
  - FE-I4 cmd and data DC-balanced
  - Self-biased FE-I4 RX inputs
- HV distribution concepts with return referenced to local module ground via high resistive path, or to current return

Current distribution on module

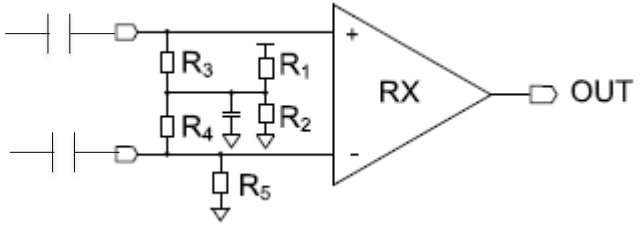


PSPP chip

Picture from N. Lehmann



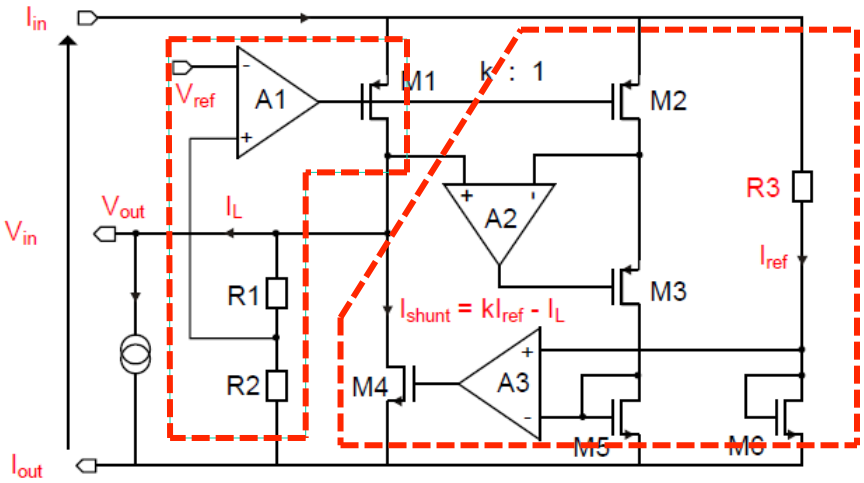
FE-I4 AC-coupled LVDS link



Shunt-LDO regulator

- Idea and design by M. Karagounis (Hochschule Hamm-Lippstadt)

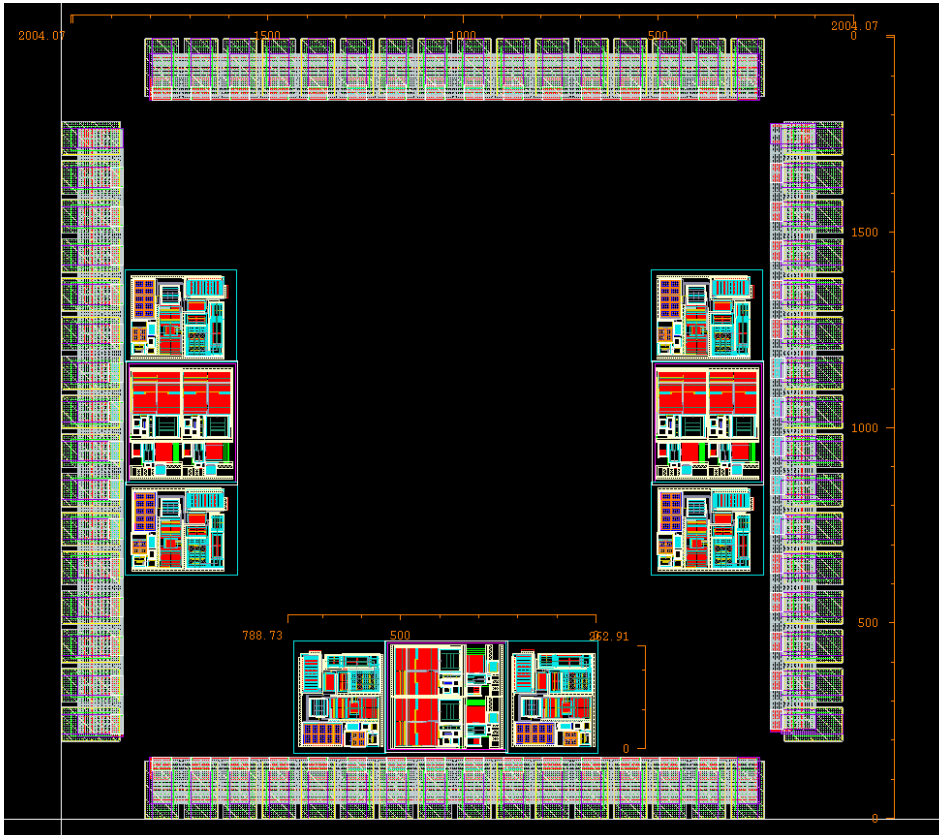
- Voltage regulation loop (LDO) → constant $V_{out} = 2V_{ref}$
- Current regulation loop (shunt) → keeps current through the regulator constant
- Ohmic input characteristics $R_{in} \approx \frac{V_{in}}{I_{in}} \approx \frac{R3}{k}$



- Shunt-LDO features
  - Robust design against process variation and mismatch for safe parallel operation
  - Parallel operation of regulators with different output voltages and shunting capabilities possible
  - Ability to shunt extra current
  - Different working modes for current and voltage based powering

Upcoming: shunt-LDO prototype in 65nm

- 1:1 copy of the design of the Shunt-LDO in FE-I4 (not yet designed for 65nm chip specs)
- Submitted last week



Testchip – Size
2 mm x 2 mm

Testchip - Content
3 regulator incl. biasing

Pad – Count
4 x 16 with 100 µm pitch

Area per Regulator:
800 µm x 400 µm

Pads per Regulator:
5 x input current
5 x shunt current
5 x output voltage
1 x reference voltage
1 x biaising voltage
1 x internal resistor con.
1 x external resistor con.
1 x shunt-circuitry supply

Pixel Serial Powering Protection (PSPP) chip

- Work done at Uni Wuppertal, design by L. Puellen
- Module bypass scheme integrated into DCS system
- PSPP chip loaded on module flex, connected in parallel to the module
- Features:
  - Autonomous fault detection
  - Addressable power control to switch on/off selected modules
  - ADC could be used to measure HV, sensor leakage current, temperature
- PSPP chip services: I2C and power → 3 lines per SP chain
- Two prototypes already existing → working principle demonstrated

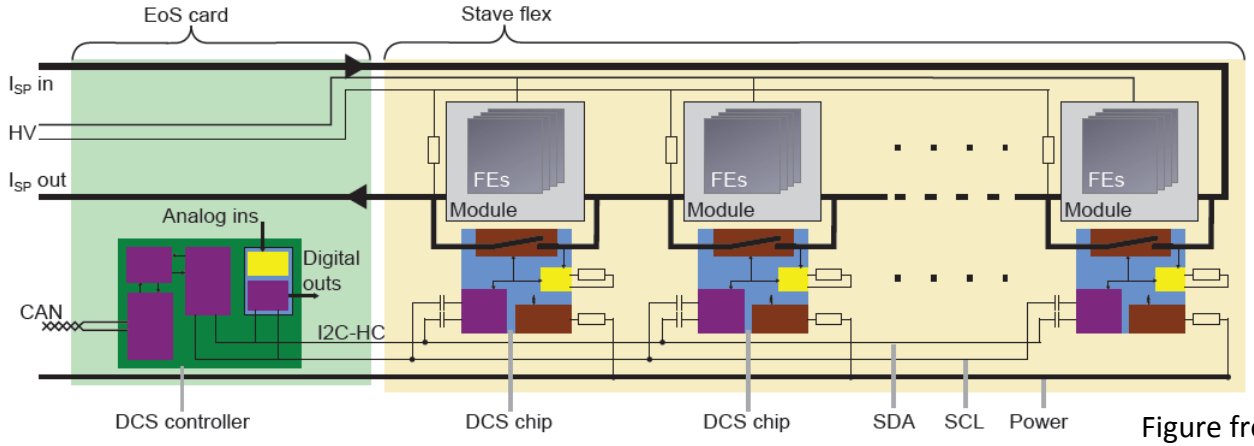


Figure from L. Puellen

Serial powering systems with FE-I4

- Several serial powering systems are in operation/development to study system aspects
  - Uni Bonn: 6 FE-I4 quad modules on a stavelet, partially equipped with PSPP chips
  - LBNL: 3 FE-I4 quad modules on a stavelet
  - Uni Liverpool: 4 FE-I4 quad modules on PCBs in one SP chain
  - Uni Glasgow and INFN Florence: SP chain of FE-I4 single chip modules on PCBs
  - More systems in preparation at CERN and Uni Oklahoma

- Overall performance is good, no significant differences observed with respect to voltage based powering schemes

Serial powering stavelet in Bonn

DCS power

USBPix power

HV

I source

Stavelet

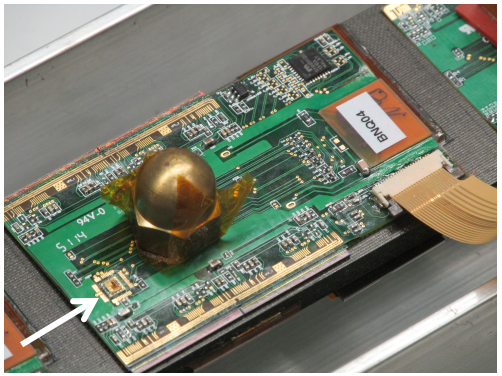
LBNL adapter PCB

DCS master and services

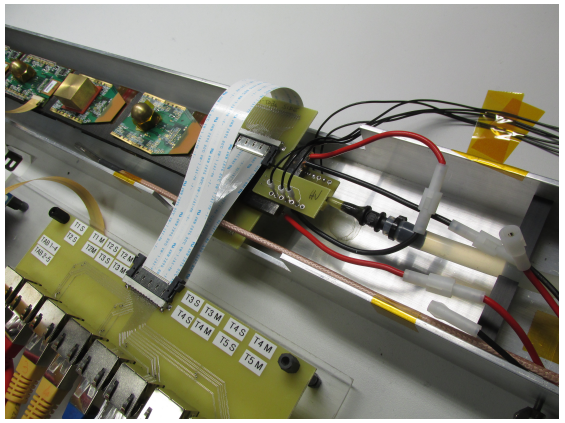
USBPix3.0

Quad module

PSPP chip



End-Of-Stave



All measurements and plots in the following slides done by V. Filimonov

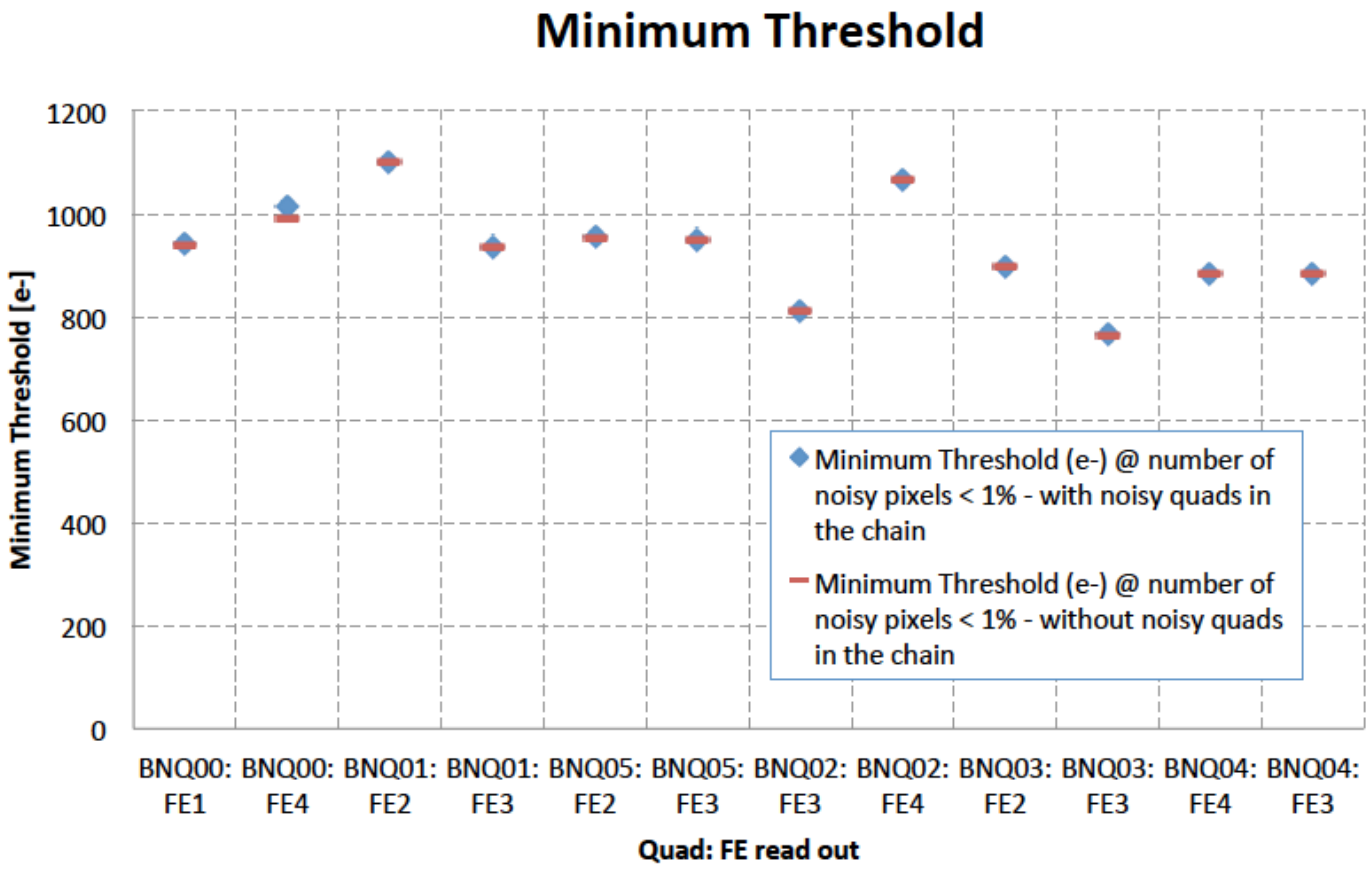
Minimum threshold operation

- Starting point: 6 quad modules tuned to standard threshold values (i.e. 1500e^- threshold, 10TOT @16ke^-)

- Lower the global threshold (GDAC) in steps
- At each step
  - Perform noise occupancy scan (10^7 triggers, 25ns each)
  - Mask pixels with a noise hit probability (NOcc) > 10^{-7}
- When the number of masked pixels reaches 1% stop the scan
  - Leave the FE noisy and continue with the other FEs
  - Increase the global threshold (GDAC +1) and continue with the other FEs

Results of minimum threshold searches

- FEs can be operated at thresholds as low as ~800e-
- Noisy FEs in the chain do not affect the performance of the other FEs



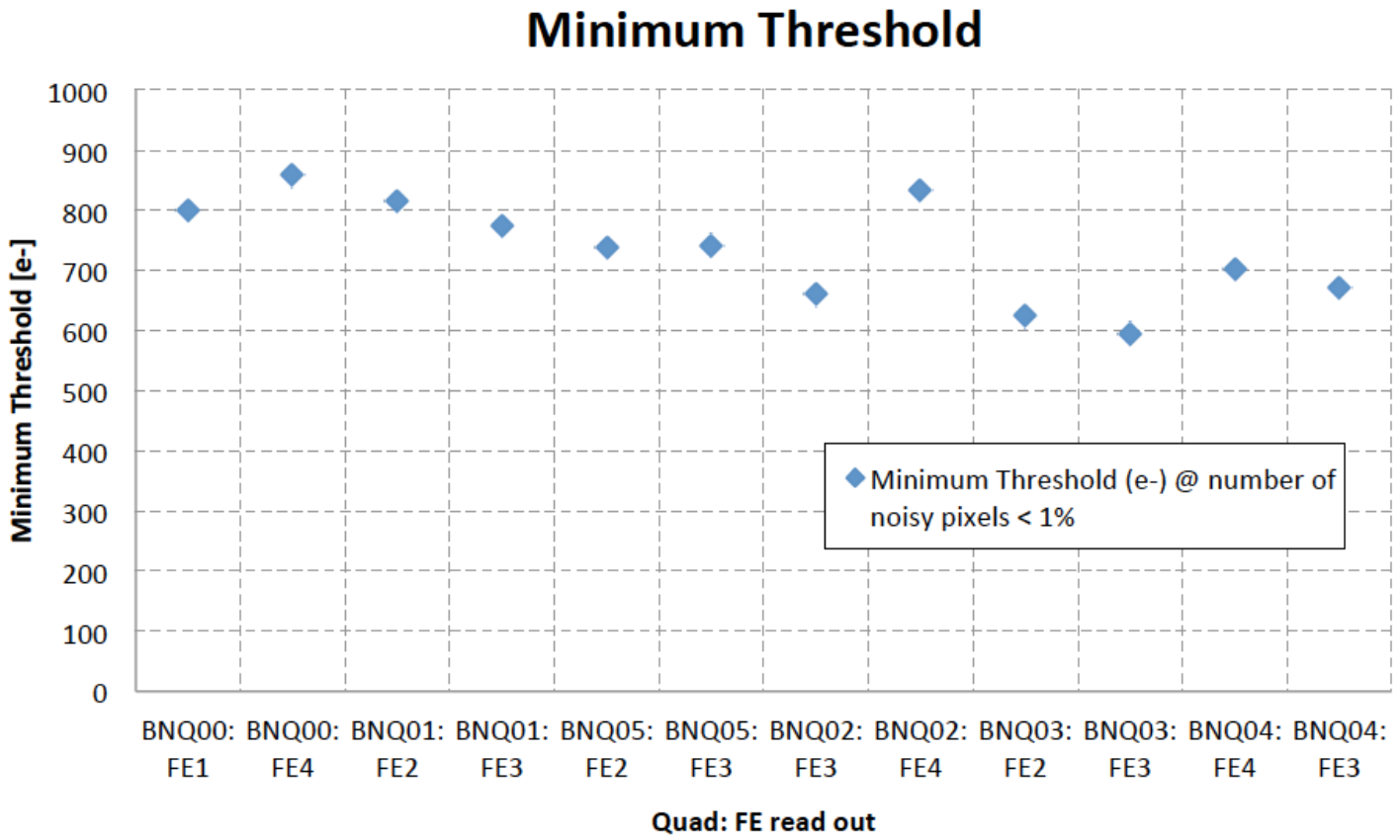
Improved minimum threshold search

- Starting point: 6 quad modules tuned to standard threshold values (i.e. 1500e^- threshold, 10TOT @16ke^-)

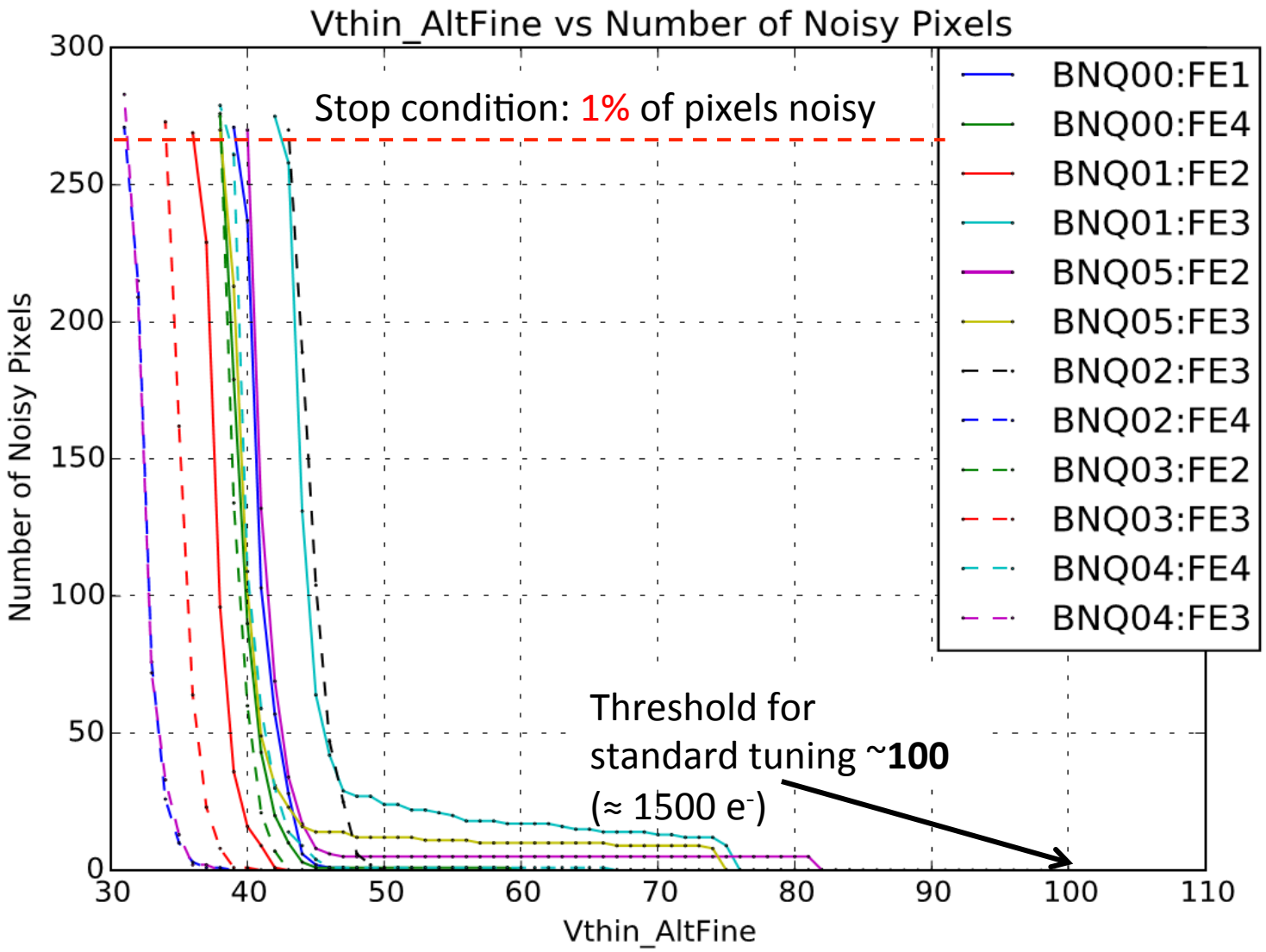
- Lower the global threshold (GDAC) in steps
- At each step, tune the local threshold (TDAC), i.e. increase the threshold of noisy pixels
  - Perform noise occupancy scan (10^7 triggers sent, 25ns each)
  - Mask pixels with NOcc > 10^{-7} or TDAC at maximum
- When the number of masked pixels reaches 1% stop the scan
- Increase the global threshold (GDAC +1) and continue with the other FEs

Results of improved minimum threshold searches

- FEs can be operated at thresholds below ~800e$^-$, down to ~600e$^-$



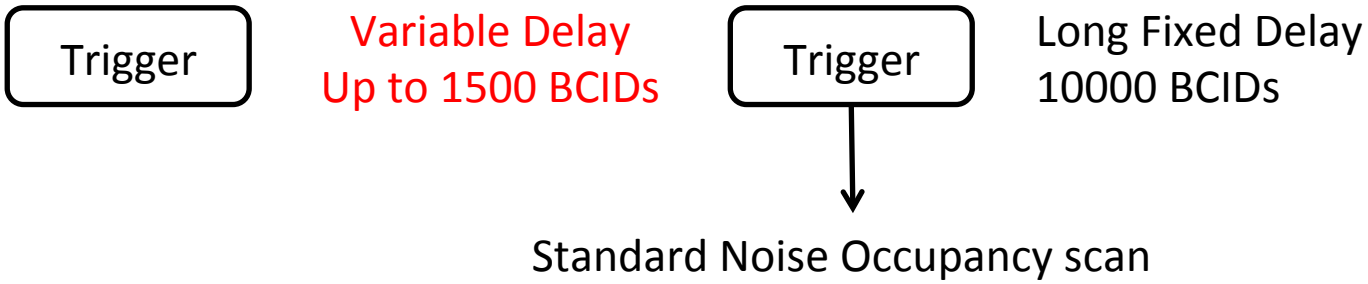
Results of improved minimum threshold searches



2-trigger scan: influence on NOcc

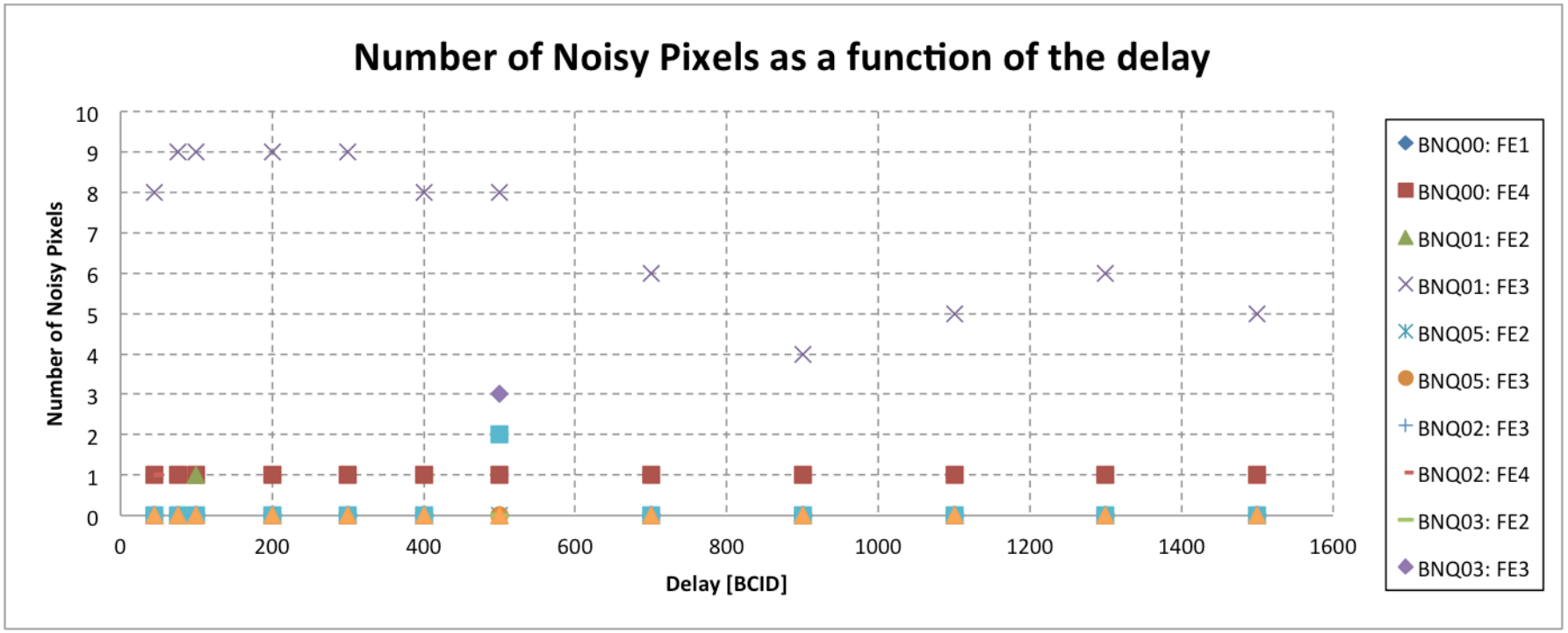
- Starting point: 6 quad modules tuned to minimum threshold

- Command pattern
  - Trigger multiplicity = 1
  - Long fix delay between repetitions



2-trigger scan: influence on NOcc

- No increase in the number of noisy pixels wrt. standard operation
- Lowest delay between triggers ~45BC. For lower values data errors → needs to be investigated (observed also on direct power module)



Conclusion

- Powering for pixel detectors at the HL-LHC is challenging!

- Current ideas are based on long experience with serial powering of ATLAS pixel modules
  - Enabling technologies like shunt-LDO, module bypass scheme, AC-coupling data transmission etc. already developed and integrated in ATLAS pixel modules
  - Successfully built serial powered pixel systems based on FE-I3 and FE-I4 with similar performance as parallel powered systems

- More work needed in many areas (esp. off-stave)
  - Complete definition of the entire pixel powering scheme
  - Modularity, i.e. size of SP chains
  - Power, voltage and current requirements of chips resp. modules
  - Grounding and shielding concepts