Calorimeters Special Needs

Mauro Citterio

On behalf of

INFN and University of Milano

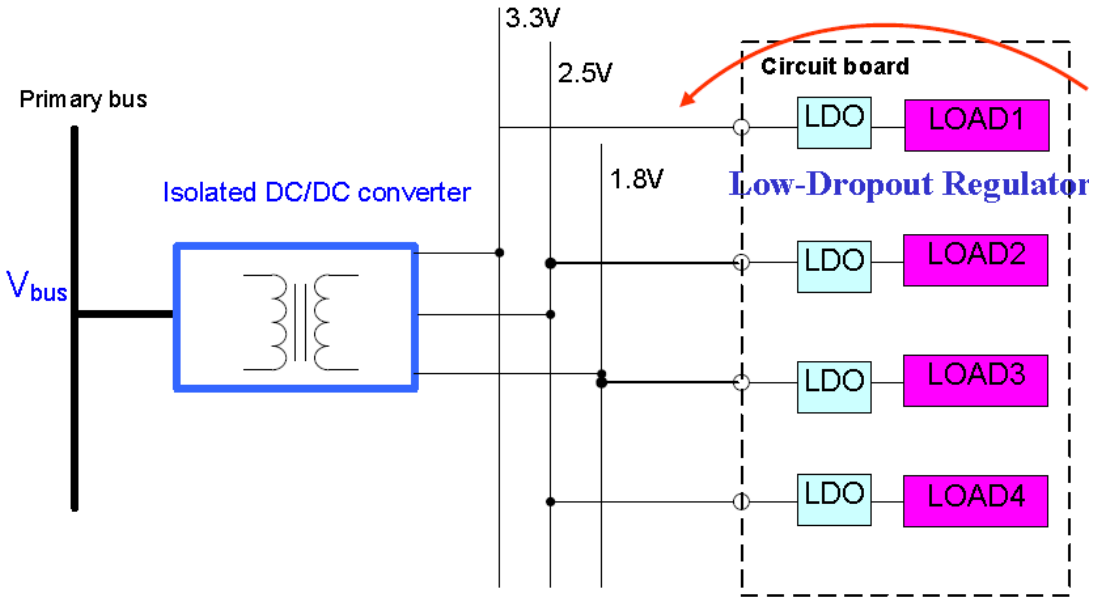
Outline

- Low power distribution architectures
- ATLAS and CMS Calorimeters for Phase II
- Engineering Issues
- Work in Progress (ATLAS LAr case study)
- Conclusions

Centralized power distribution architecture

In large systems with many electronics channels grouped in “read-out boxes”

- Typically, one or many isolated converters/distributors generate the whole set of regulated DC voltages (±12V, ±5V and +3.3V) to be provided to the subsystem circuits.



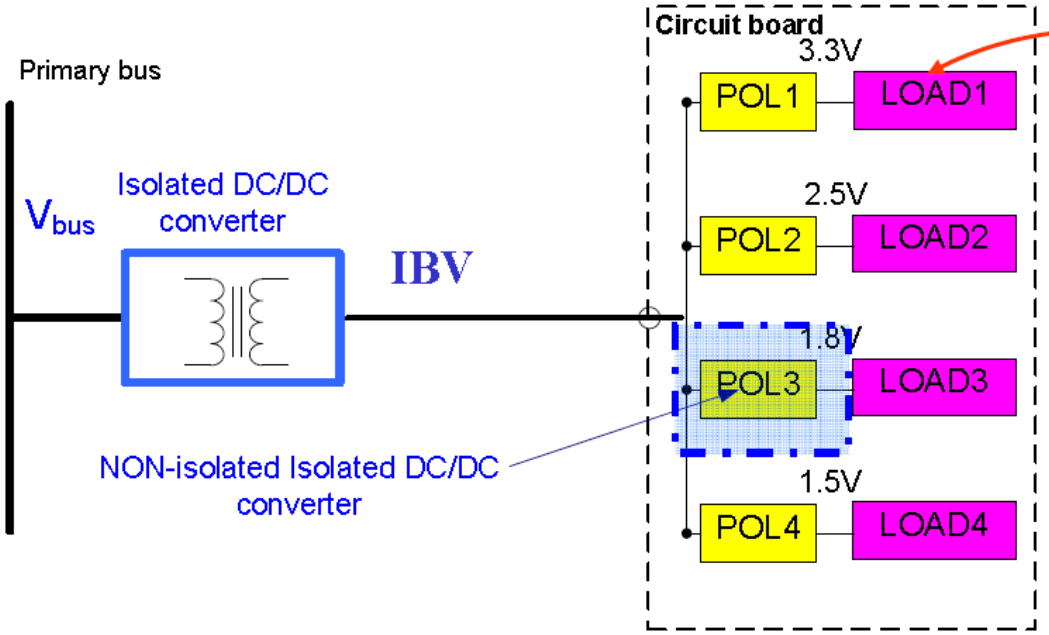
Effects.

- High number of long connection cables (penalty in volume and weight)
  → The converter is “as close as possible” to the load !!!!
- Low flexibility
- High losses mainly in unique hot spot + losses in linear regulator LDO
- Converter power up to several KW/unit

Distributed Power Architectures (DPA)

Phase II upgrades requires new electronics with lower supply voltages
→ LDO regulators replaced more and more by NON-Isolated DC/DC converters

Distributed Power Architecture (DPA) replaces the centralized power distribution
→ A single intermediate DC bus (+48V or +12V) is generated by a main converter



Optimized Voltage Drop

High static regulation and improvement of the dynamic performances
(the impact of the series resistance and inductance is reduced)

The DPA approach benefits from increased efficiency, low size and weight, especially if the “main converter” is really near the front-end electronics

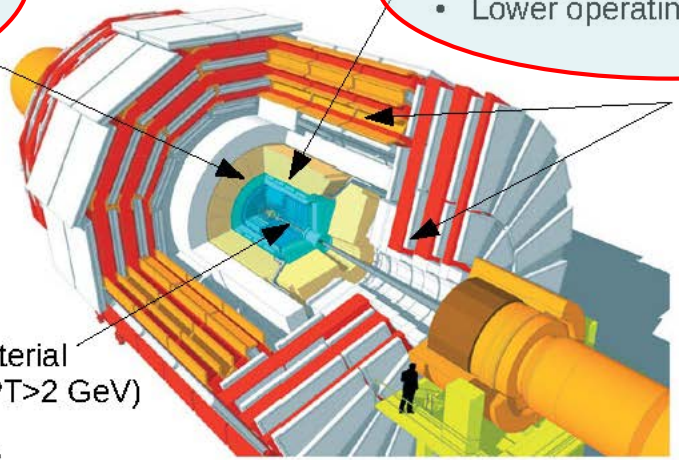
DPA Advantages

- Rationalization of the number and level of the voltages required by the Front End electronics
  - only few intermediate voltages must be supplied (one or two)
  - loads must be served by PoLs regulators
- Based on the availability of PoLs
  - rad tolerant
  - highly efficient
  - magnetic tolerant
  - properly sized in term of max current (several Amps ….) to match the load requirements
- Requires new design of the “main converter”, in some cases
  - improved tolerance to radiation ← → converter near front-end
  - modular approach
  - higher switching frequency
  - optimized design of magnetic devices
  - minor losses and heat
  - reduced voltage across devices
  - high reliability / low maintenance

CMS @ HL-LHC

New Endcap Calorimeter
- Radiation Tolerant
- High Granularity
- 3D capability

Barrel Calorimeter
- Replace FE/BE electronics
- Lower operating temperature(8°)



Muon system
- Replace DT/CSC FE/BE electronics
- Complete RPC coverage In region 1.5<η<2.4
- Muon tagging with GEMs for 2.4<η<3.0

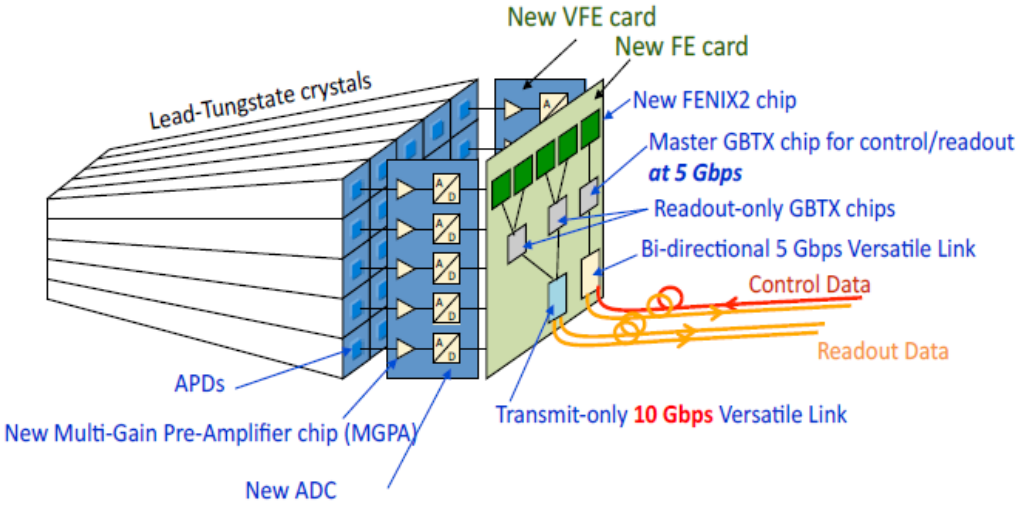
New Tracker
- Radiation tolerant – less material
- 40 MHz selective readout (PT>2 GeV) for track trigger
- Extend to coverage of η~3.8

(Current L1: 4 μs latency, 100 kHz output)

Trigger/HLT/DAQ
- L1 Track Trigger
- L1 Trigger: 12.5 μs latency, 750 kHz output
- HLT output of 7.5 kHz

Technical Proposal Upgrade CMS per HL-LHC
CERN-LHCC-2015-010 LHCC-P-008 CMS-TDR-15-02
June 2015 ***https://cds.cern.ch/record/2020886***

ECAL Barrel on-detector electronics @ HL-LHC



The APDs are connected to a passive motherboard (MB) which
-distributes high voltage and low voltage
- interconnects the APDs to the very-front-end (VFE) cards.

Neither the APDs nor the MBs will be replaced.
The EB upgrade achieved by replacing:

- the VFE and FE cards
- the optical links
- **the low-voltage distribution system**

- **New ASICs → different bias voltages**
- **Radiation-hard DC-DC converter instead of LDO regulators on the new low-voltage regulator card (LVR)**
- **Power supplies STILL into rack ~ 30m away → no substantial improvements necessary**

CMS High Granularity Calorimeter (HGC)

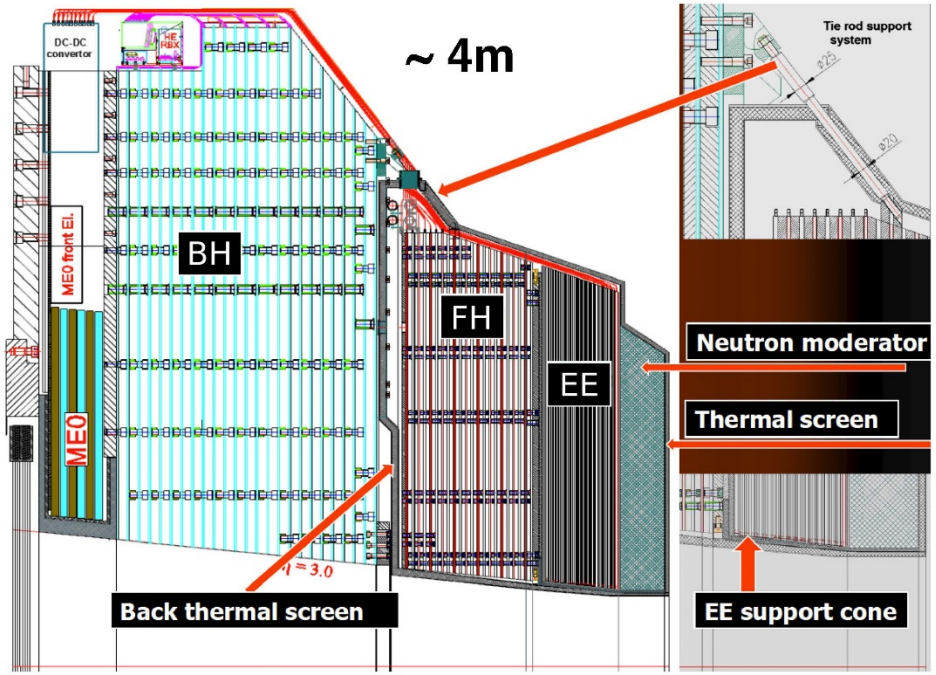


Figure 3.23: Technical drawing of the overall structure. The EE has its front face at the same location as the front face of the current EE. Directly behind it there is the FH, which is a 3.5 λ silicon-brass calorimeter. Behind that is a 5 λ backing hadron calorimeter (BH), which, since the radiation levels are low, uses a similar technology to that of the current HE.

Table 3.2: Parameters of the EE and FH.

	EE	FH	Total
Area of silicon (m^2)	380	209	589
Channels	4.3M	1.8M	6.1M
Detector modules	13.9k	7.6k	21.5k
Weight (one endcap) (tonnes)	16.2	36.5	52.7
Number of Si planes	28	12	40

~ 2 x 50 kW @ 1.2V

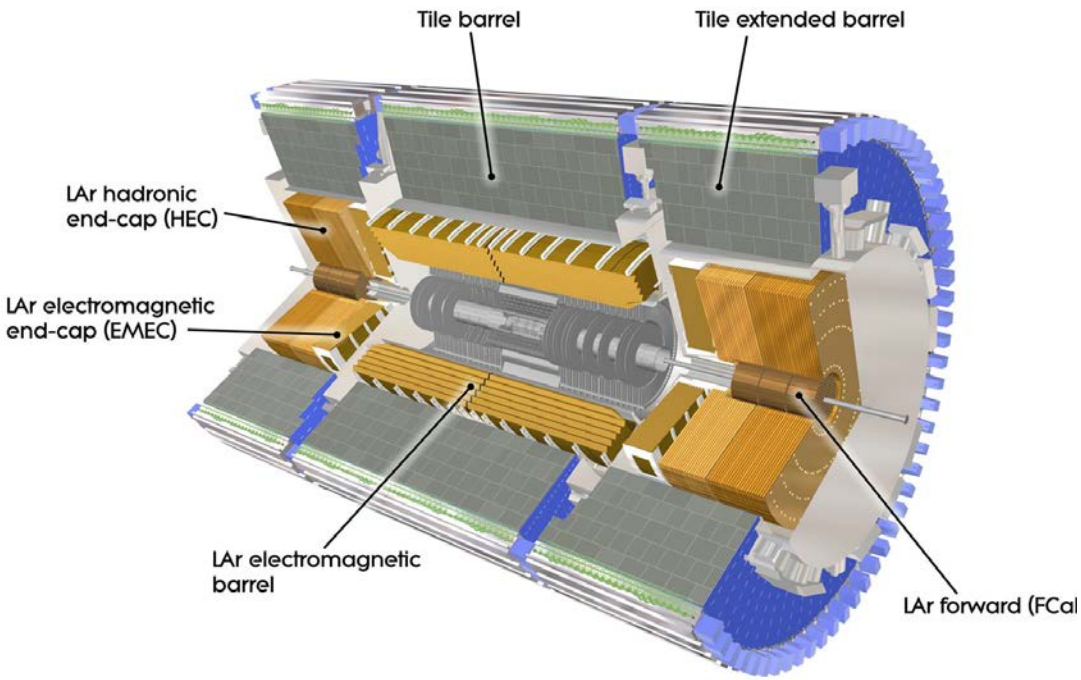
use DC/DC (off detector) + on-detector regulators

DC-DC converters off detectors, used to reduce cross-section of the cables between the converter and the modules (~ 4m)

Power supply located behind the BH (~10m from the DC-DC converter) → No "substantial changes" from present scenario

Compact and "rad-hard" DC-DC converters could be mounted directly on the detector modules, with only a marginal increase in the gap between absorbers

ATLAS @ HL-LHC



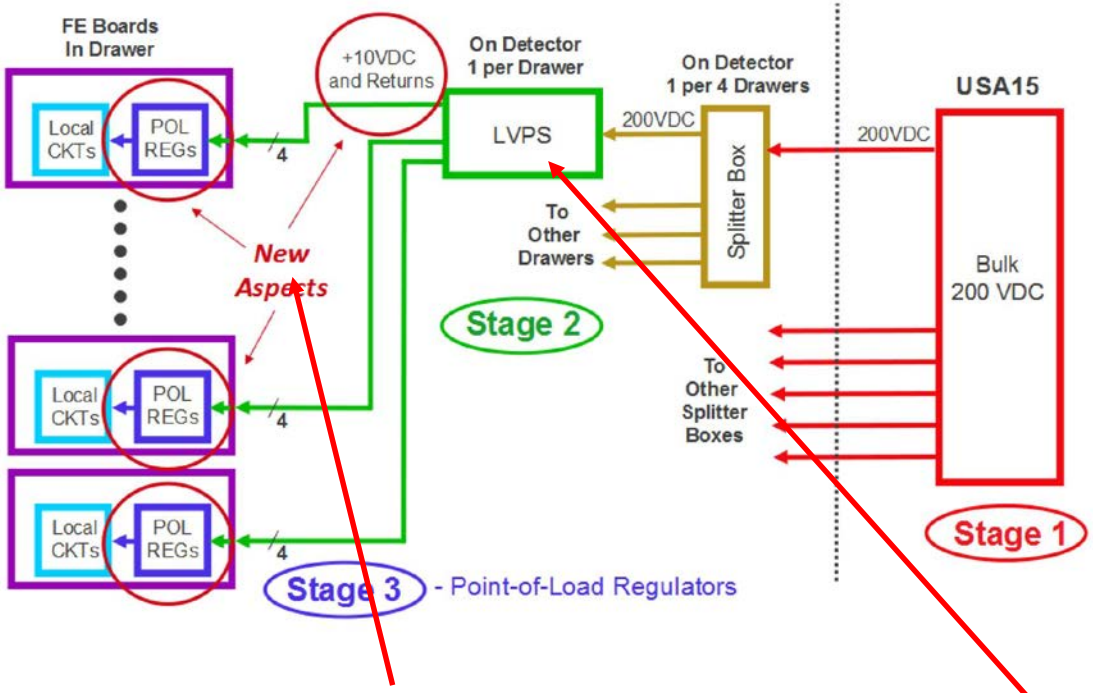
Both the EM and the Hadronic calorimeter will change the FE electronics

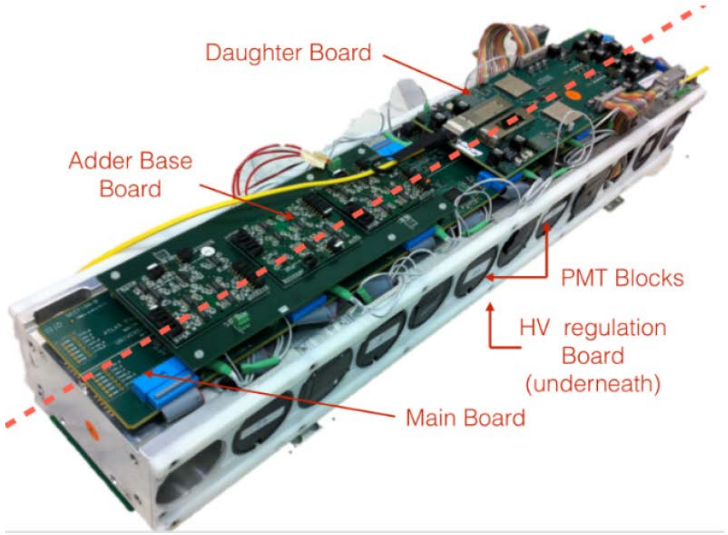
Consequently the power supply system need to be changed

A distributed power architecture will be adopted:

- The “main converter”, being a custom supply, need to be redesigned and must undergo a dedicated R&D
- The converters are in proximity of the FE electronics (<1m) for both Tile and LAr calorimeters
- **PoL converters should be available**

ATLAS Tile @ HL-LHC





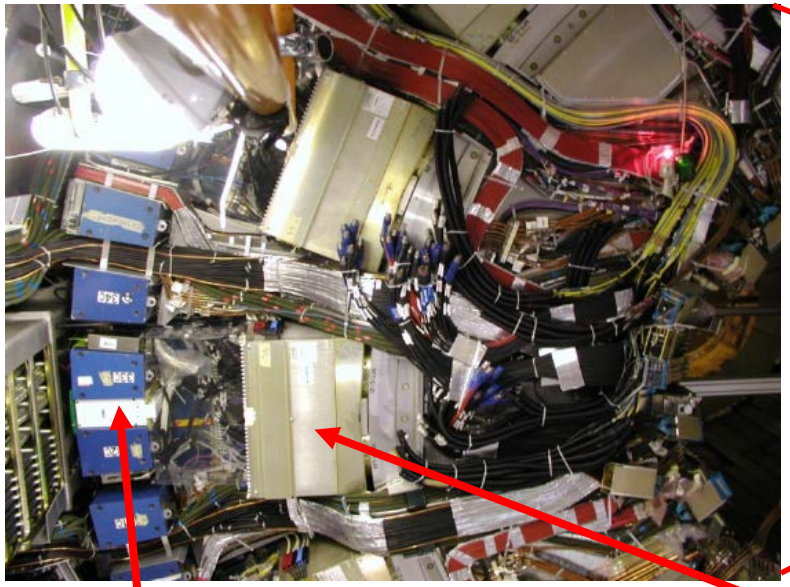
Point of load regulators (POLs) are used on the MB and DB to supply the needed voltages.

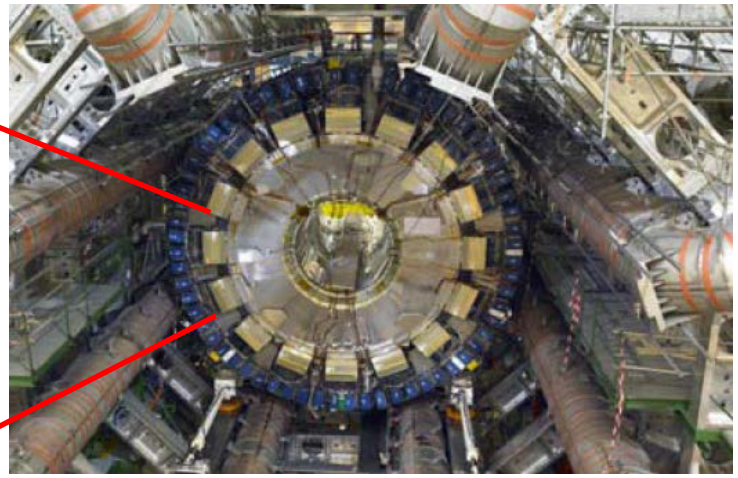
PoL choice is on going …..

The LVPS system consists of +10 V feeder supplies located at the ends of the barrels.

Total power is ~ 300 Watt/unit

ATLAS LAr @ HL-LHC





Front-end Electronics
Equivalent Load: ~ 3kW
Load will not increase in Phase II

DC-DC Main Converter
Constrained between two Tile fingers
Dimensions: ~ 15x30x40 cm^3
Water cooled

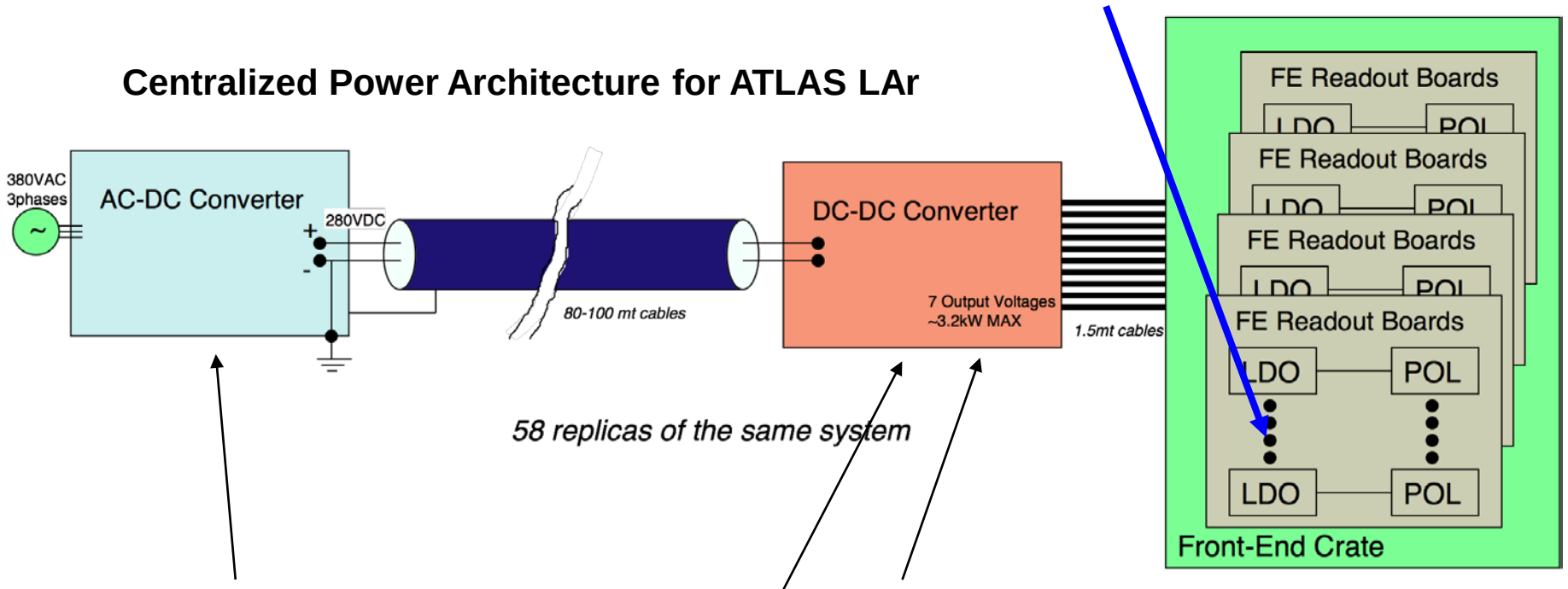
Power Supply exposed to
- radiation
- "moderate" magnetic field (< 1 kG)

NOT accessible → Reliability/Redundancy
Single Point of Failure

ATLAS LAr Power Architecture: Present status

Tens of Low Drop-Out regulators/FEB

Centralized Power Architecture for ATLAS LAr



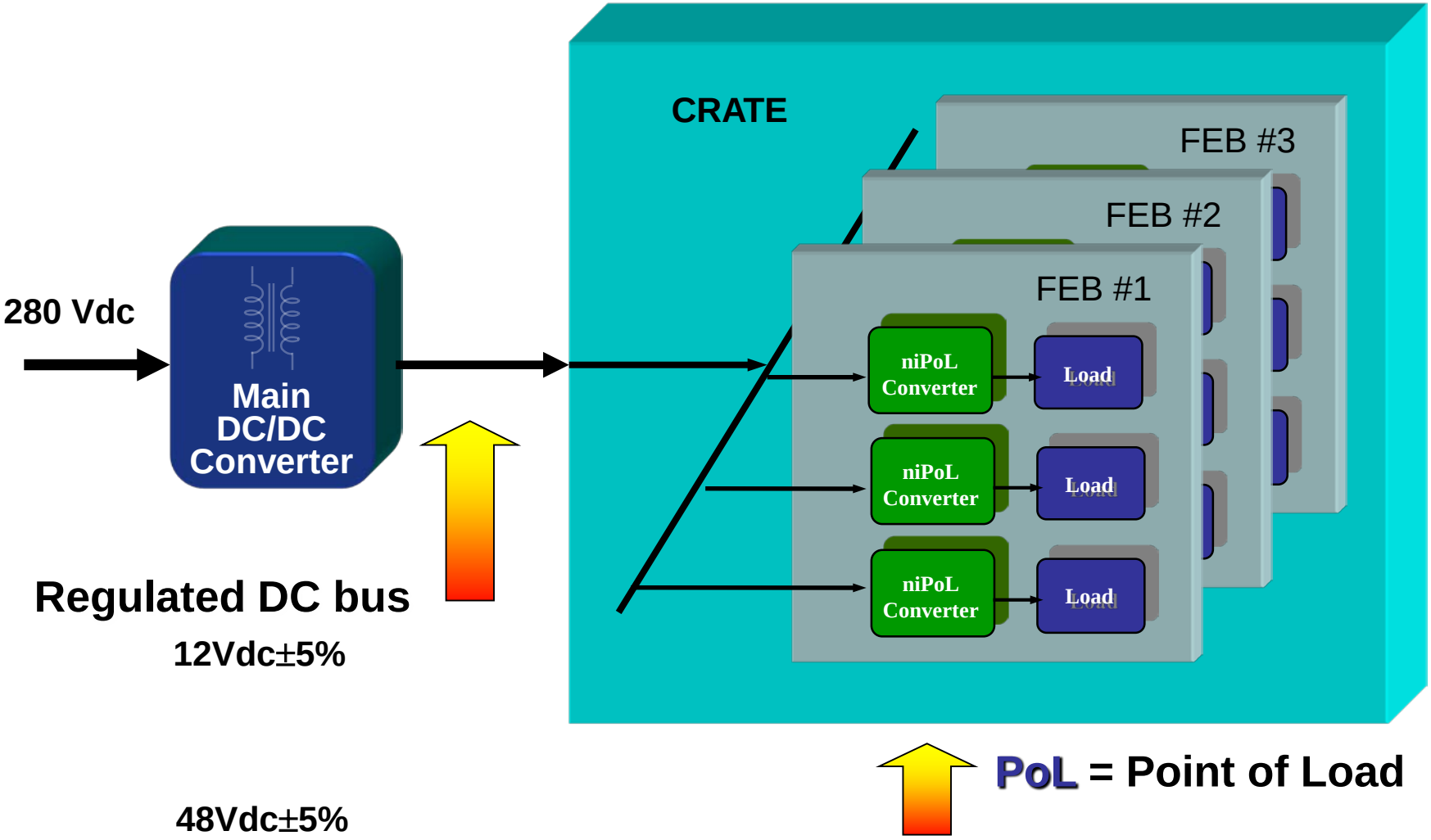
58 replicas of the same system

Outside the cavern

On detector
(~ 1 m from the Front-End Electronics)

~ 5 MCHF including spares

ATLAS LAr DPA for Phase II

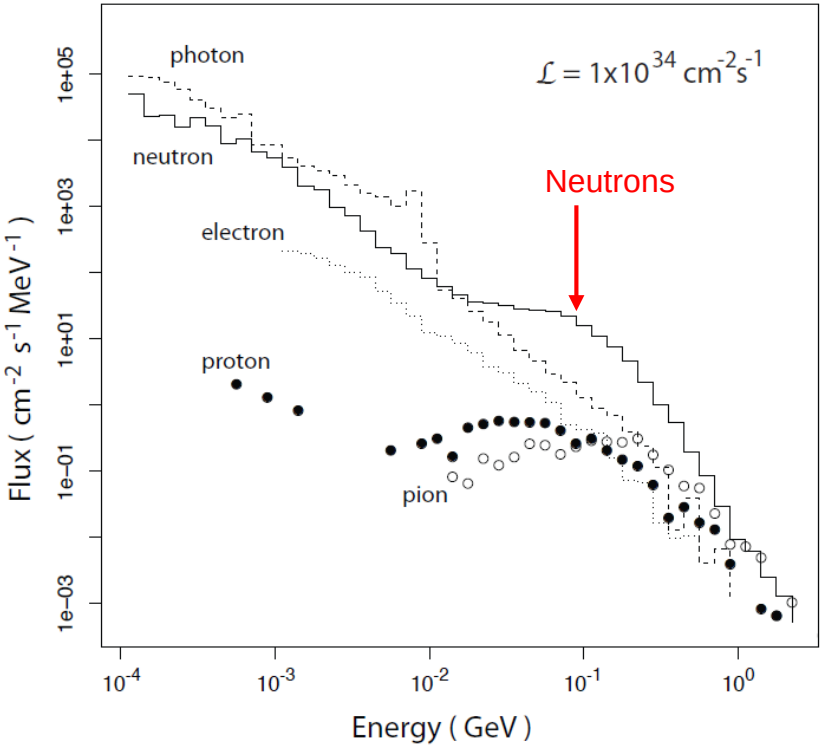


High DC conversion-ratio converters

ATLAS LAr Radiation Environment

	Simulation (one year)	Safety Factor	Test Target* (10 years)
Ionizing Dose	3.0 rad	10	100 krad
1 MeV eq. Neutron	6.0×10^{11} cm^{-2}	2	1.2×10^{13} cm^{-2}
Hadrons (>20 MeV)	8.5×10^{10} cm^{-2}	2	2×10^{12} cm^{-2}

*1 LHC year = 10^7 s, σ_{pp} = 80 mb, Luminosity = 5×10^{34} cm^{-2}s^{-1}



The expected background for the ATLAS Liquid Argon (LAr) calorimeter electronics are shown in the Table for Phase II run.

Phase II background ~ 10 time higher than present

Radiation background is due to a mixed-field of hadrons, electrons and photons.

Electronic devices are effected by: Single event effects, Total ionizing dose, Displacement damage

Engineering Issues (1 of 2)

PoL converter Design

- Electromagnetic immunity of the front-end electronics to the switching converters
- Both CMS and ATLAS are planning to benefit from the CERN designed PoL (FEAST).
- Other rad-tolerant COTs devices are being/have been tested against radiation
  - For space optimization
  - For larger maximum current capabilities
  - For larger input voltage range
  - One very promising candidate is the LTM4619 (tested by BNL, mostly and by Milan)

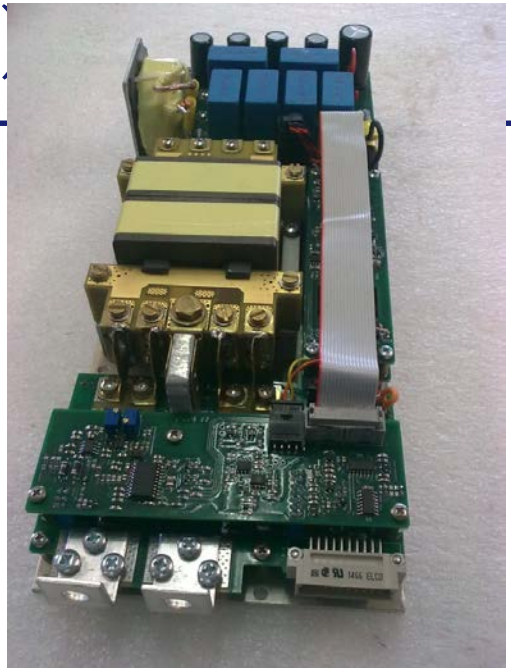
Main Converter design

- Number and levels of intermediate voltages
- How many? Positive and negative?
- Which levels? High for loss reduction or lower for a reasonable POL design (voltage ratio)?
- Redundancy N+1 (single failure tolerance)
- Modular approach: number of modules Vs total power oversizing
- Thermal design
- Power losses distribution

Engineering Issues (2 of 2)

- Analog/Digital/Power Devices selection for the Main Converter
  - Active switches selection
    - Power and voltage level
    - Switching frequency
    - MOSFETs, SiC, GaN
  - Analog/Digital Controllers
    - PWM Controllers
    - Drivers
    - Signal Isolators
    - FPGAs
  - Design of magnetic parts
    - Coreless devices
    - Low permeability cores
    - Thermal analysis

Work in progress - ATLAS Lar (1 of 4)



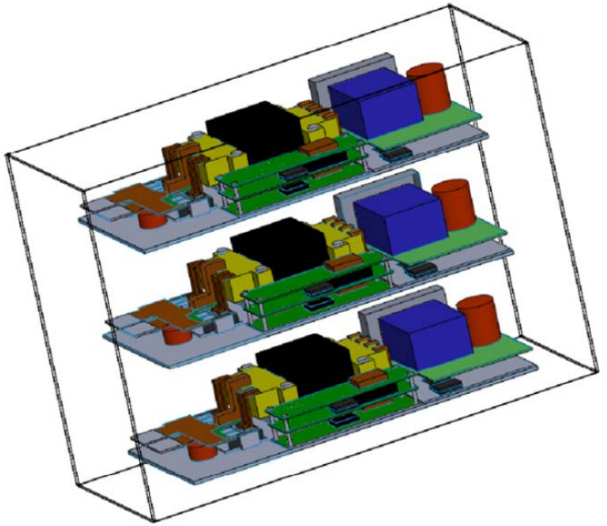
Design of a **M**ain **C**onverter based upon a **DC-DC Phase Shifted Converter** well suited for multi-outputs, or-ed connections and constant load supply (single pole dynamic).

Study Initiated within an INFN Project (named “APOLLO”)

- Project ended in 2014
- Industrial partnership developed with CAEN

A “whole” unit constituted by 3 modules connected in parallel:

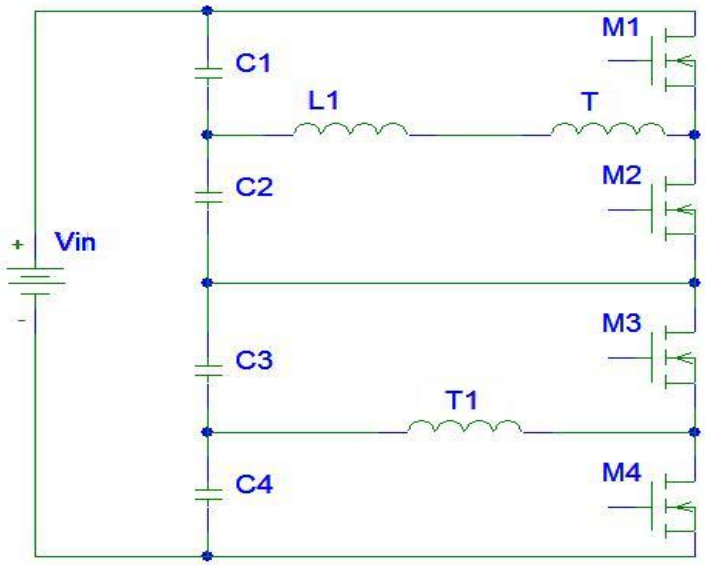
Vin= 280 V
Vout= 12V
Pout= 4.5 kW (including redundancy)
fs= 100kHz

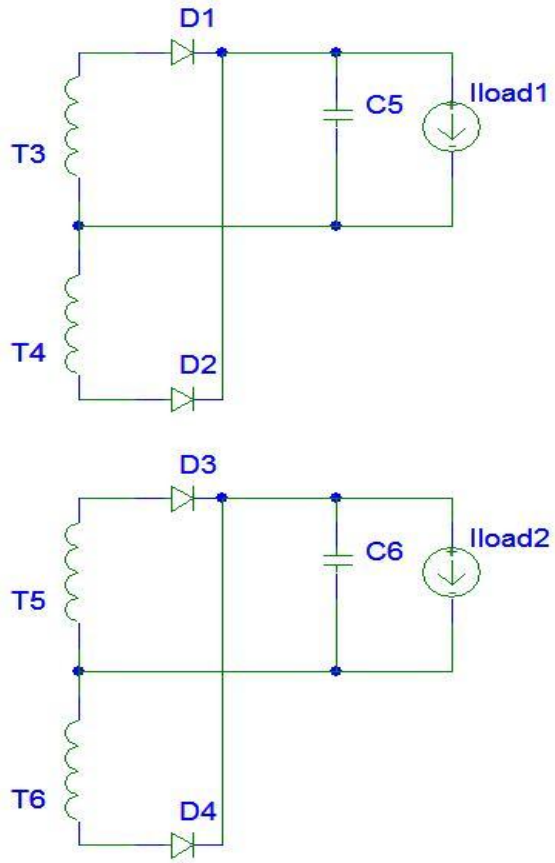


The supervision and protections are demanded to an external interface:

- current sharing
- start-up control/failure
- clock, phase shift between the modules, alarms

Switch In Line Converter





Merits

High switching frequency
Fixed switching frequency
Soft switching commutation
(use of parassitics elements: leakeage inductance)
Single pole dynamics
Well suited for multiple outputs
Suited for or-ed outputs
Reduced MOS drain-source voltage
Non-isolated feedback available

Drawbacks

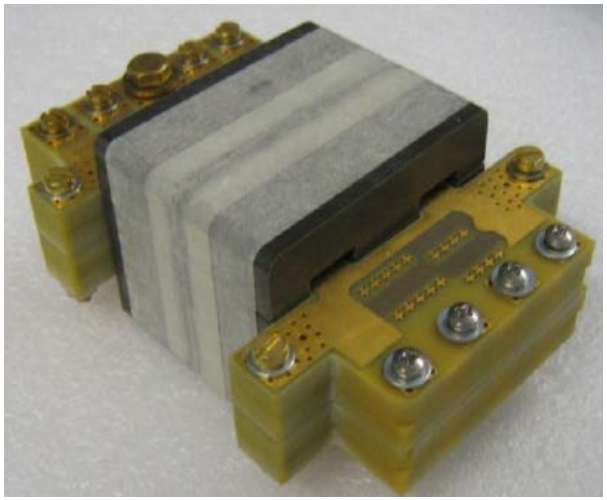
High drain current levels
High number of large capacitors

Work in progress (2 of 4)

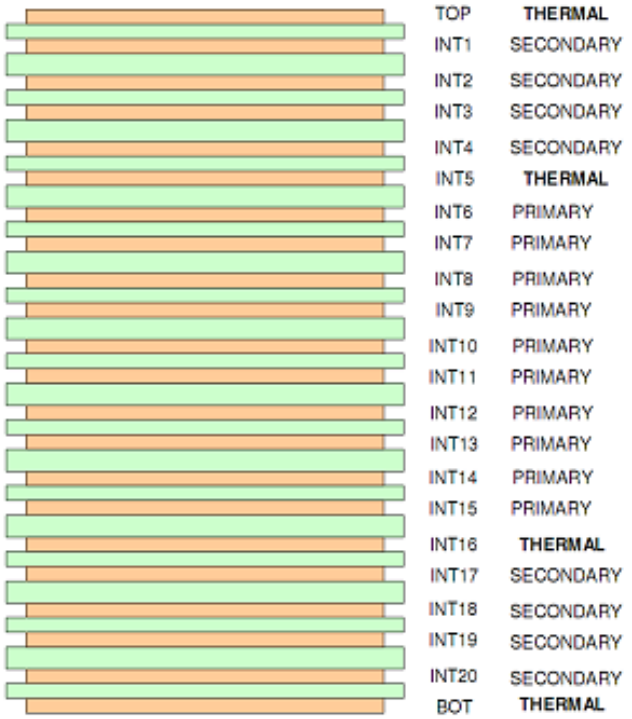
Design and construction of a prototype transformer based on a planar structure → To minimize volume, to achieve high efficiency

The whole transformer has been divided in 4 subsystems

Each subsystem consists by 10 turns for each primary windings and 2 turns for the center tapped secondary.
The secondary has been realized by means of the parallel connections of 2 windings in order to reduce the output leakage inductance.



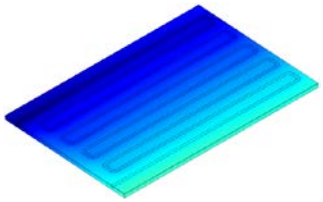
The windings of each subsystems are realized by means of a 22 layers PCB



Work in progress (3 of 4)

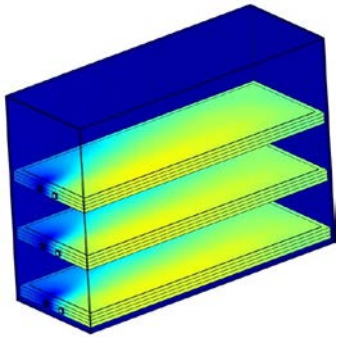
Thermal Modeling → to reduced risk of failures

- **Water cold plate**



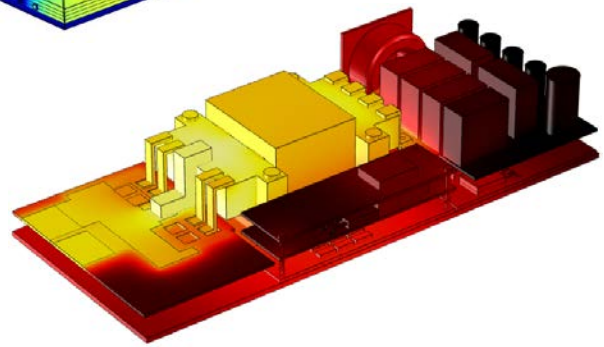
- **System Level**

  boards and cold plate position



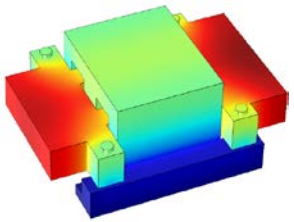
- **Board Level**

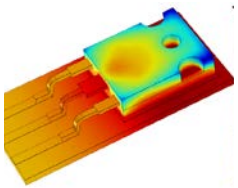
  main heating devices
  modules layout
  heating convection and conduction

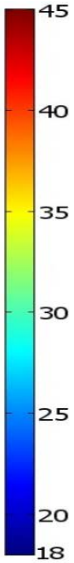


- **Device Level**

  package definition
  heating exchange between single components







Work in progress (4 of 4)

- Selection of radiation tolerant power COTs
  - Si-MOSFETs, SiC, GAN …. new devices …
    - Some components, with V_d ranging from 30V to 200V and polarized in various configurations, were tested
      - at the ^{60}Co γ ray source in the ENEA center of Casaccia, near Roma
      - with a heavy ion beam, ^{75}Br at 155MeV, at INFN Laboratori Nazionali del Sud in Catania
      - with neutrons, at the Casaccia nuclear reactor Tapiro
      - with protons, at INFN LNS and in USA
- Selection of radiation tolerant COTs controllers and FPGA
  - irradiation performed with gamma, neutrons, protons
  - FPGAs seem promising
  - Controllers seem too sensitive to radiation

    → needs for "custom" designed controllers using analog devices or FPGAs?

→ **WORK FAR FROM BEING COMPLETED**

Conclusion

- Distributed Power Architecture is being proposed for Phase II
  - Two essential components necessary

  → Point of Load converter
    - CERN FEASTMP (limited to 4 Amp) or COTs
    - Calorimeters have similar need in respect to other detectors
    - Less demanding in term of radiation

  → Main converter
  - Novel topology should be studied (SILC, for example is under study)
  - Proper Magnetic Devices Design
    - Power Planar Transformer (new magnetic material)
  - Thermal Design
  - Critical selection of components to proper withstand radiation
    - Controller, Driver and Isolator
    - FPGA for overall monitoring
    - MOSFETS
    - Novel devices based on SiC and GaN, are also under investigation
- Some results are encouraging, however more systematic validation is on-going