

Development of DCDC converters

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LHC upgrades, today available:

The FEASTMxx family of DCDC modules is in production and provides a plug-and-play solution for power distribution in LHC detector upgrades

Specifications		
	Min	Max
Vin (V)	5	12
Vout (V)	0.9	5
Iout (A)		4
Pout (W)		10



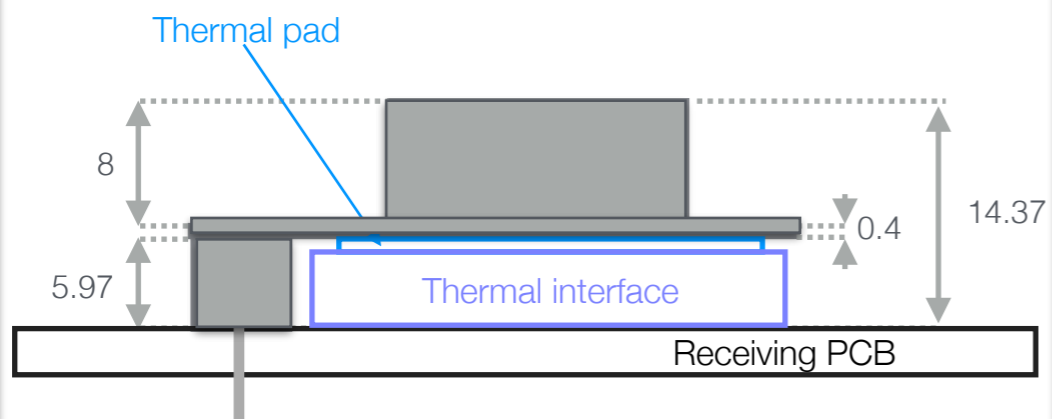
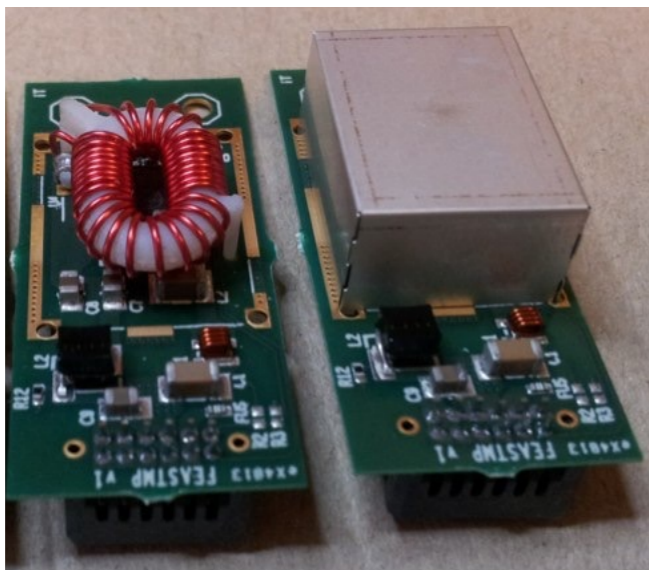
For enquiries and requests of modules:

dcdc.support@cern.ch

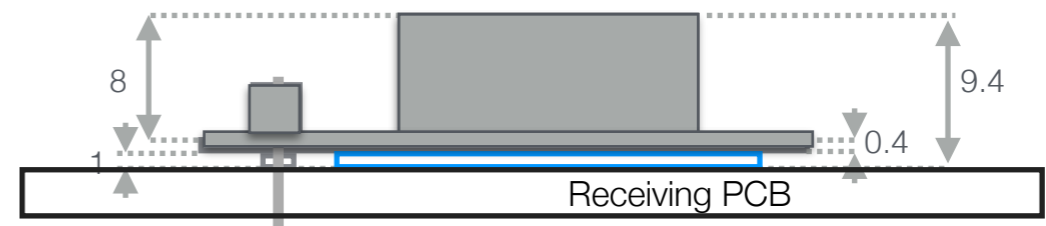
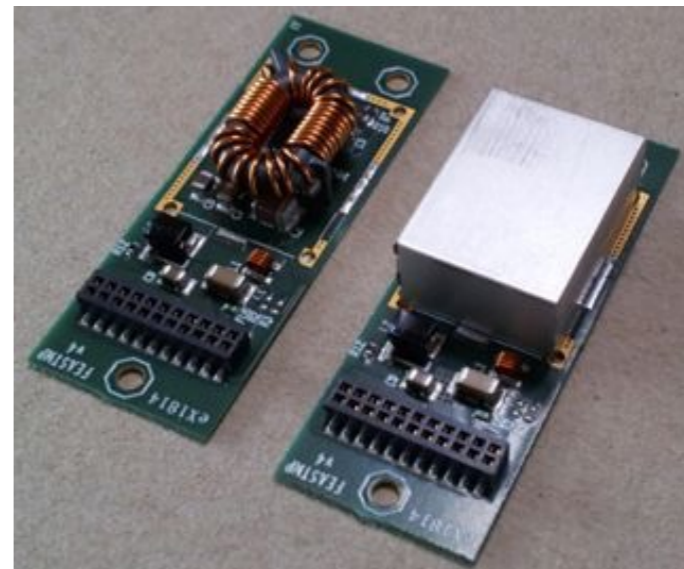


The FEASTMxx module family has been developed to meet the requirements of LHC upgrades

FEASTMP



FEASTMP_CLP

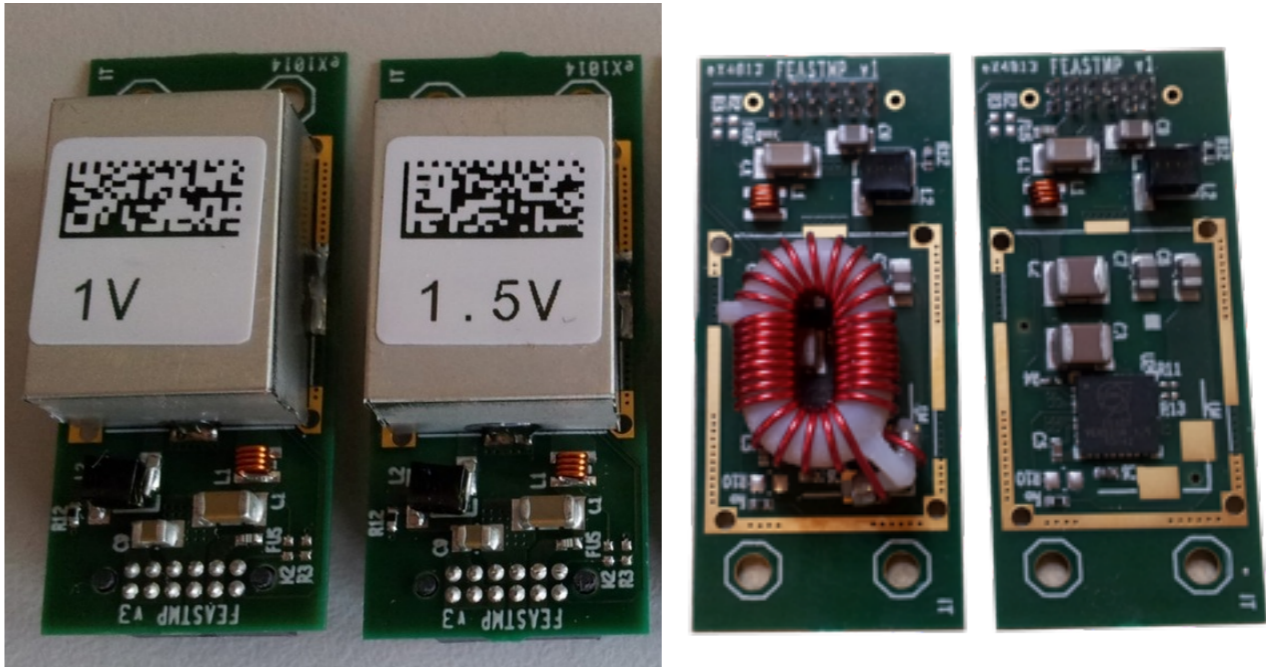


FEASTMN (prototype level)



FEASTMP DCDC modules based on the FEAST2 ASIC

Main electrical parameters	
Input voltage	5 - 12 V
Output voltage	0.6 - 5 V
Output current	0 - 4 A
Max output power	10 W
Programmable switching frequency	1 - 3 MHz
Inductor value	0.15 - 1.5 μ H
Protection features	
Over-current protection peak level	6 A
Over-temperature protection threshold	103°C
Under-voltage lockout threshold	4.5 V
Soft-Start duration	470 μ s
Control features	
Enable (input) threshold	815 mV
Power Good flag (output)	Open Drain
Radiation tolerance	
Total Ionizing Dose	> 700 Mrad
Displacement Damage (1MeV eq. neutron flux)	5x10 ¹⁴ n/cm ²
SEEs: absence of destructive events and of output power interruptions	> 65 MeVcm ² mg ⁻¹

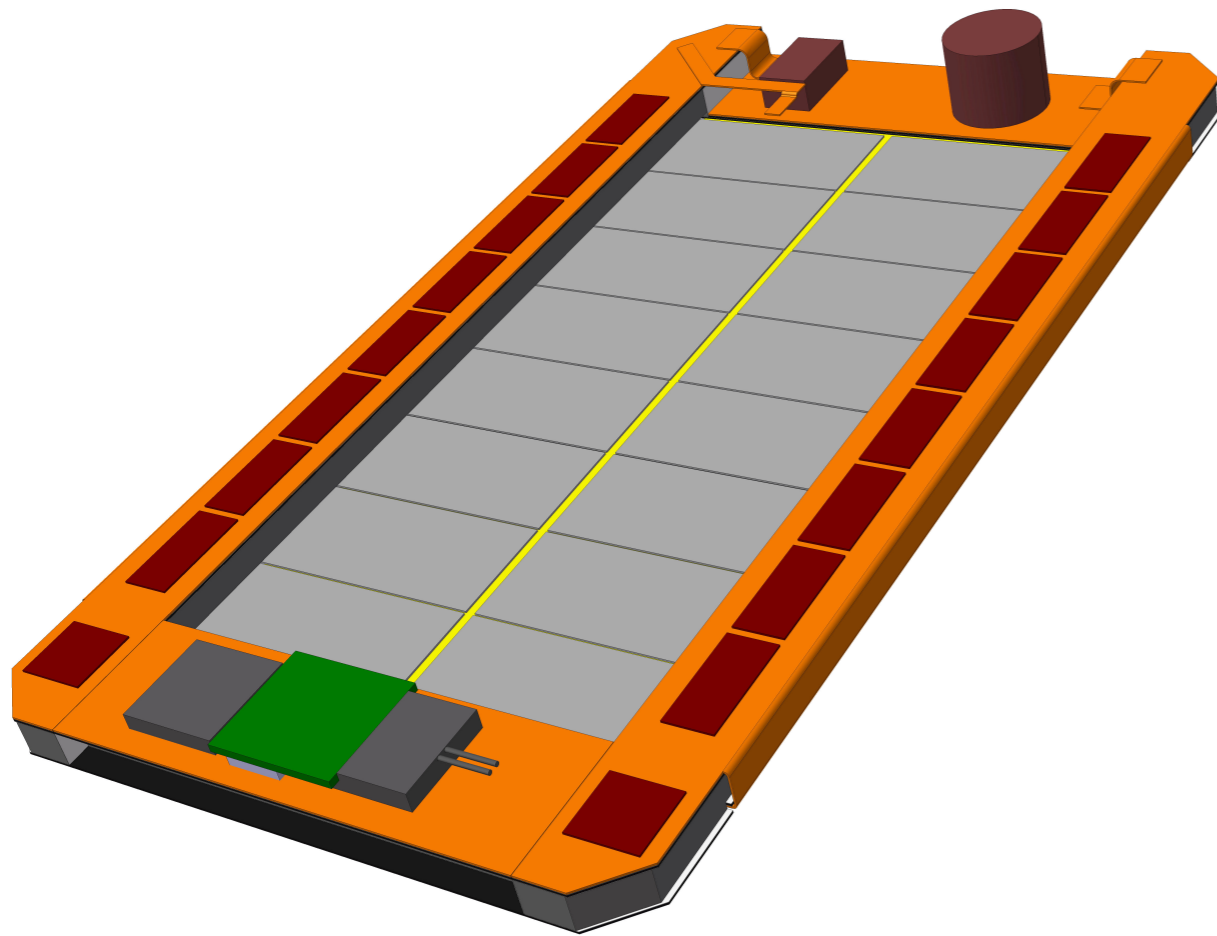


Both the FEAST2 ASIC and modules are in production. 30,000 ASICs and 20,000 modules are being provided to the experiments over a period of 2-3 years.

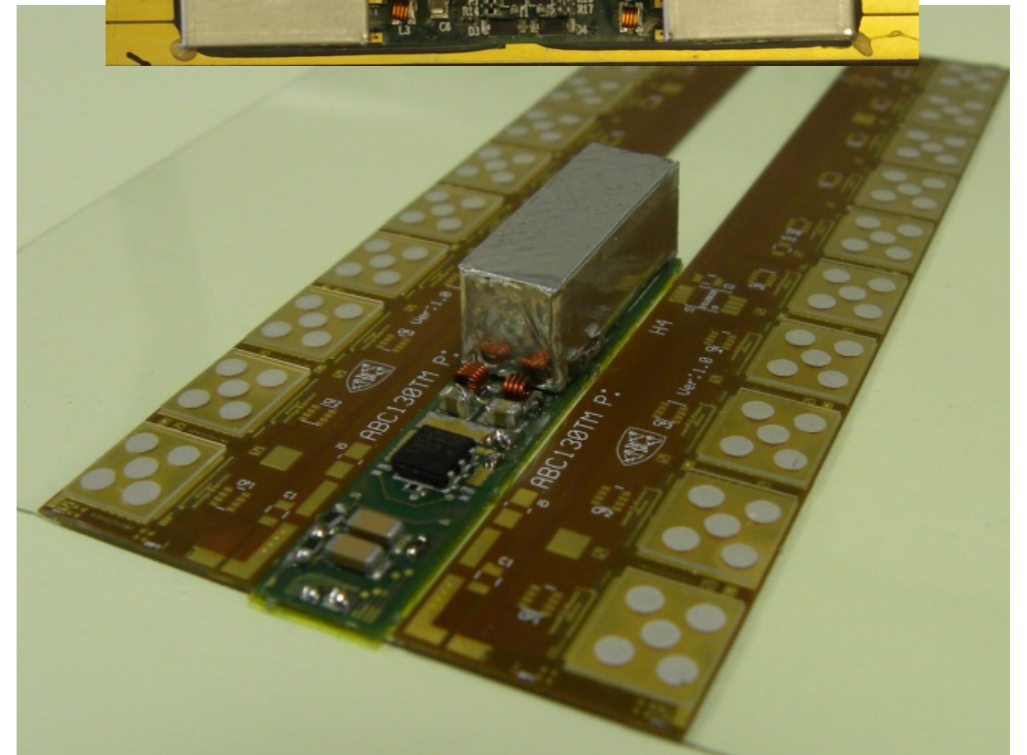
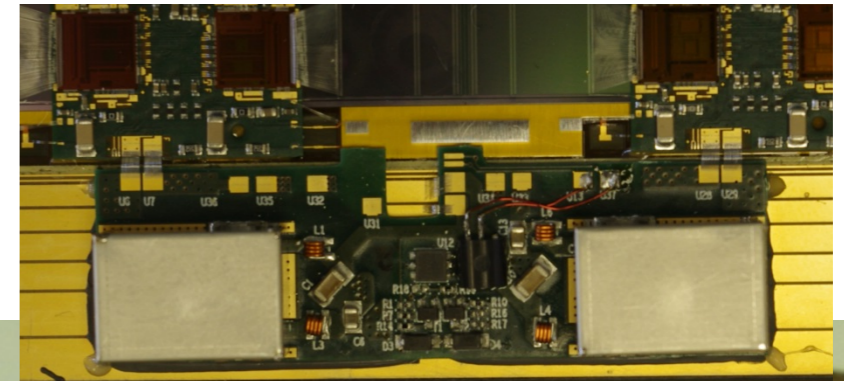
5x10¹⁴ n/cm² → Limit for HL-LHC of tracker’s upgrades.

ATLAS/CMS HL-LHC trackers upgrades

**CMS/ATLAS Trackers will require
higher radiation levels
custom integration
new DCDC blocks**

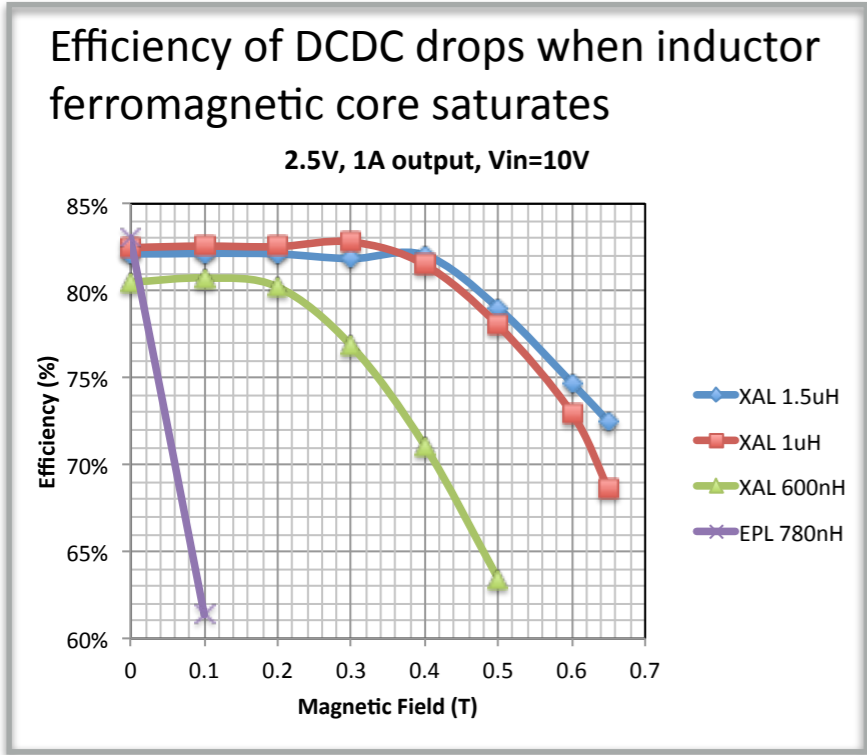


CMS PS module model
(G.Blanchot)

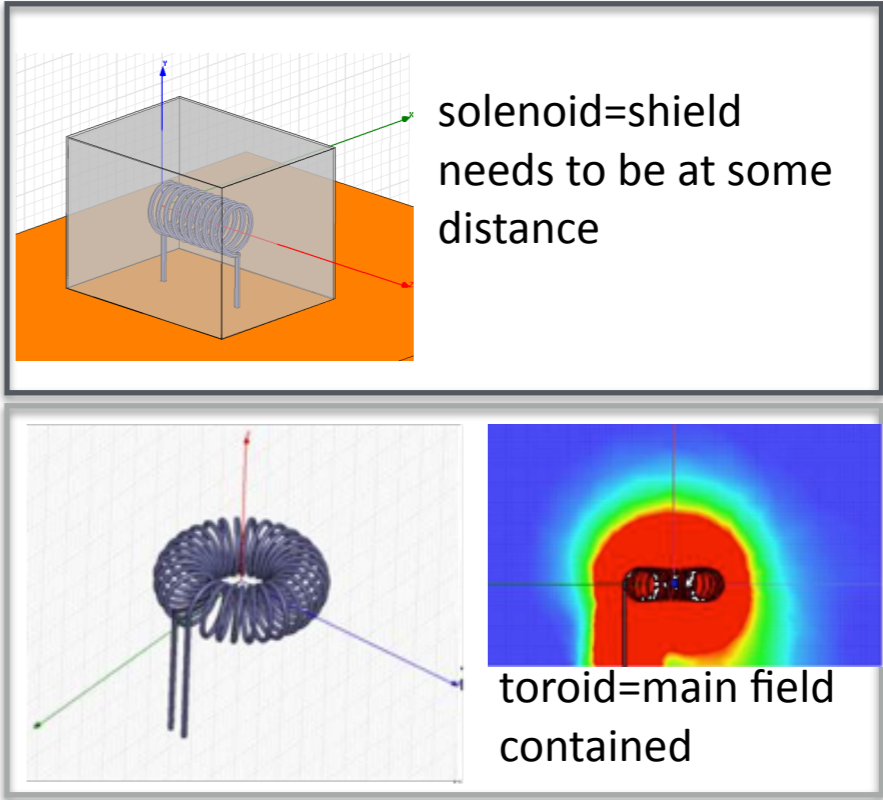


ATLAS ITK customisation
(P.Phillips, ACES14)

A custom development for reducing the inductor mass (and therefore the material budget) for tracker applications can be done



air-core inductor

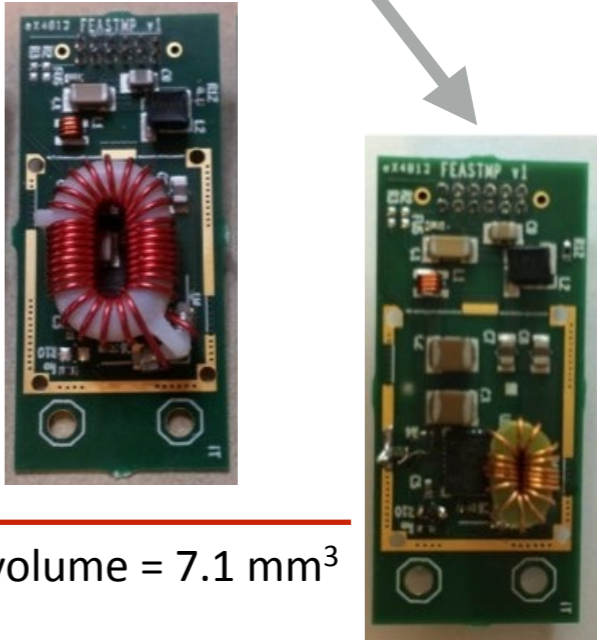


customisable

Inductor	Wire length (mm)	Wire diameter (mm)	Wire volume (mm ³)	Wire Cu volume (mm ³)	Wire Al volume (mm ³)
400 nH Coilcraft, bulk copper	360	0.5	70.65	70.65	0
197 nH prototype, ECCA wire	160	0.38	18.1	5	13.1

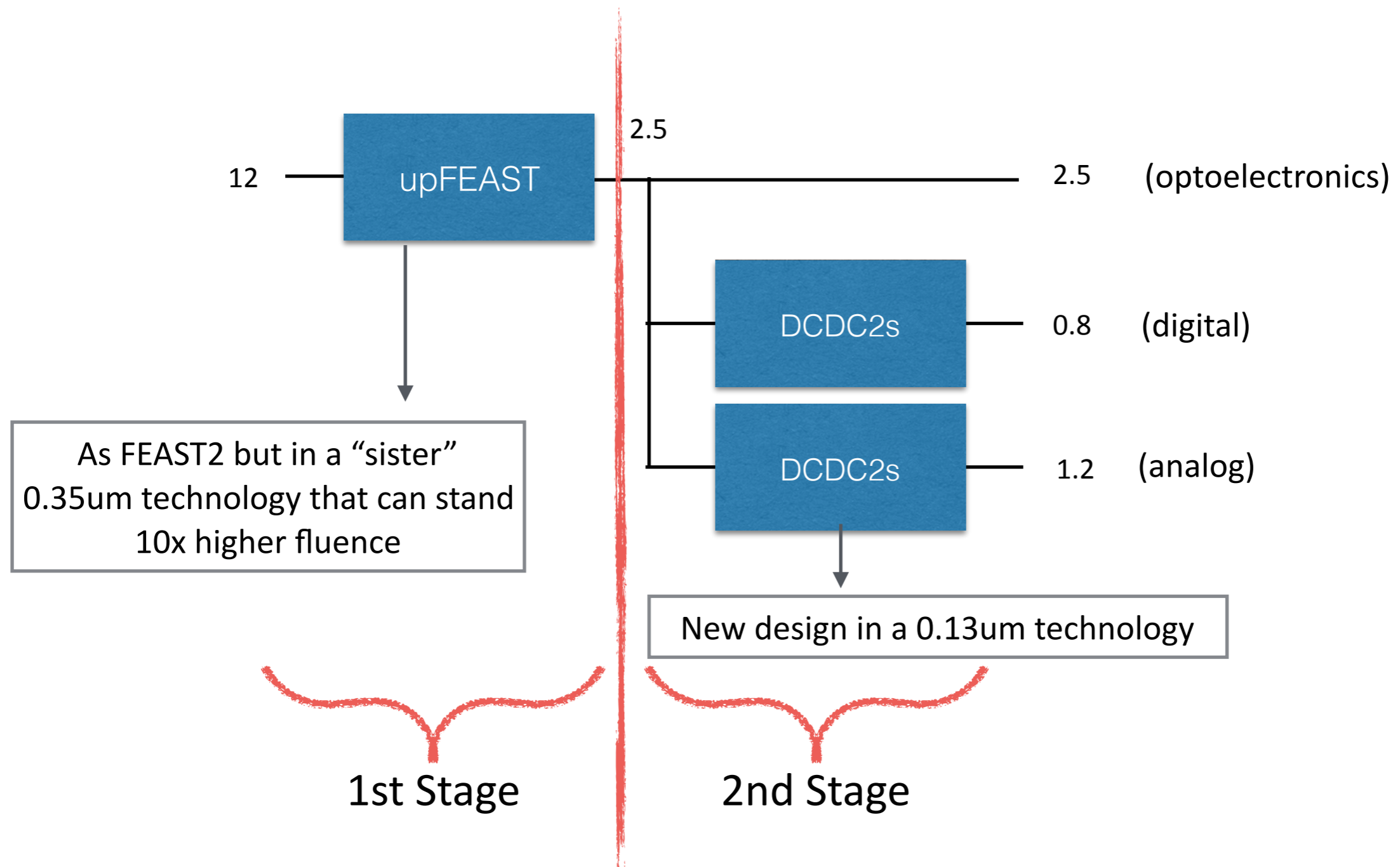
Cu volume = 70.65 mm³

equivalent Cu volume = 7.1 mm³



A more efficient and radiation tolerant on-module power distribution scheme needs new DCDC converters

3 Supply voltage from 1 Power Bus @12V

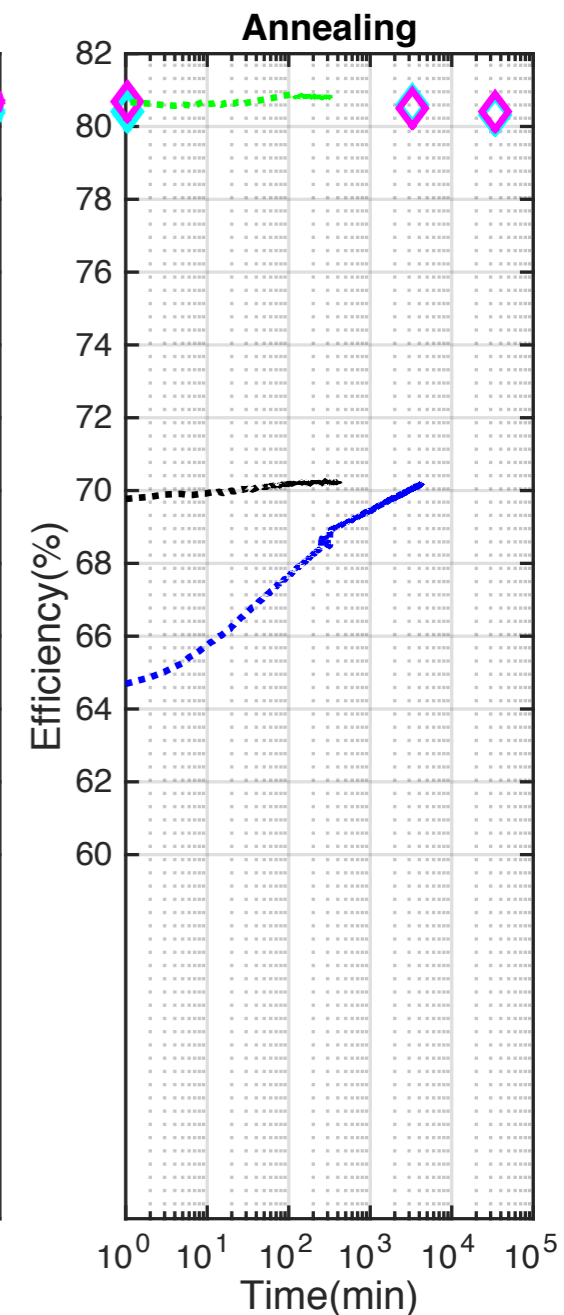
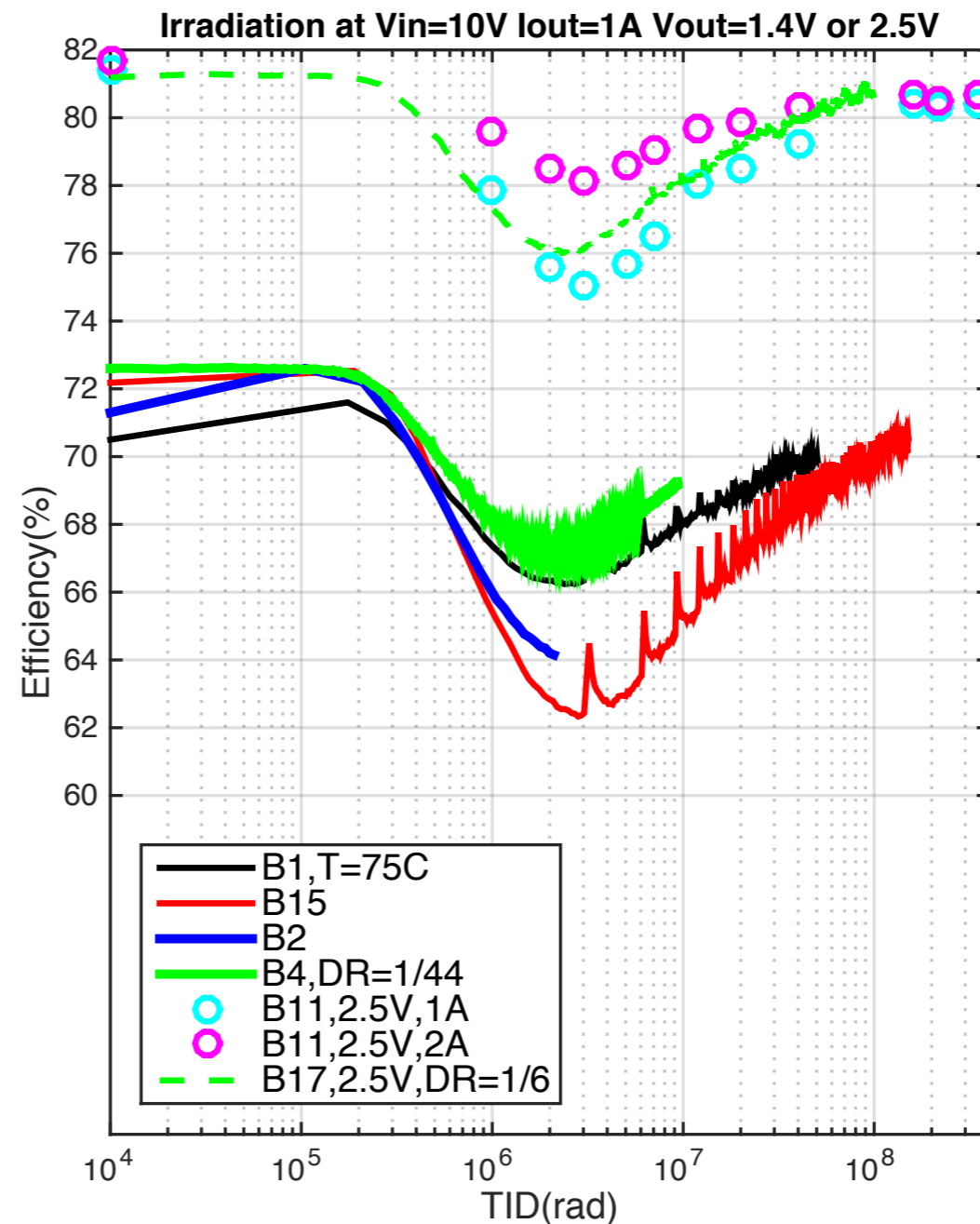
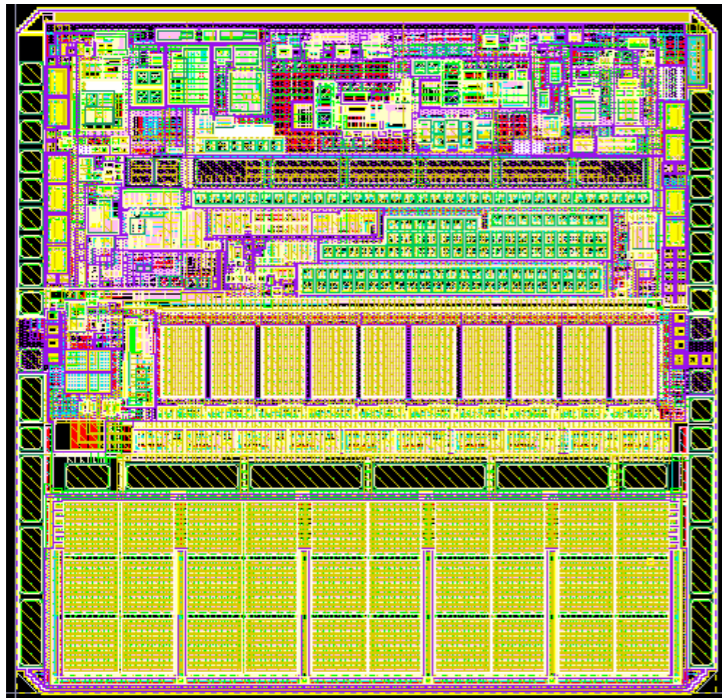


1st Stage: upFEAST

upFEAST tolerance to DD can be increased to meet the requirements of HL-LHC CMS/ATLAS trackers

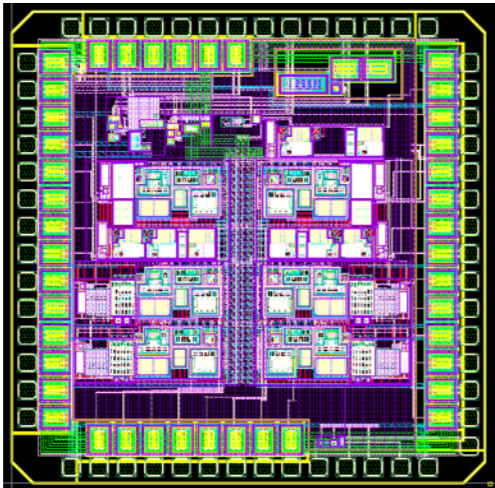
FEAST2 design has been moved in a 'sister' technology that can stand much higher fluence.

The new ASIC is called upFEAST.



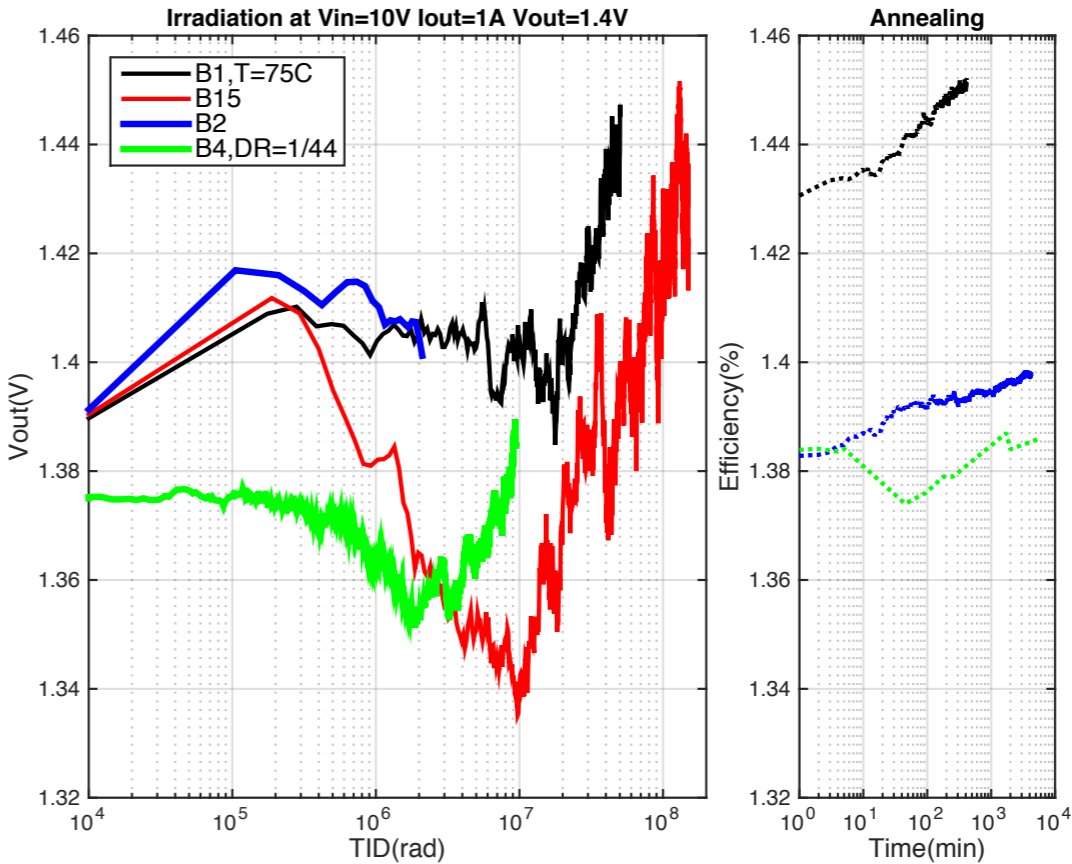
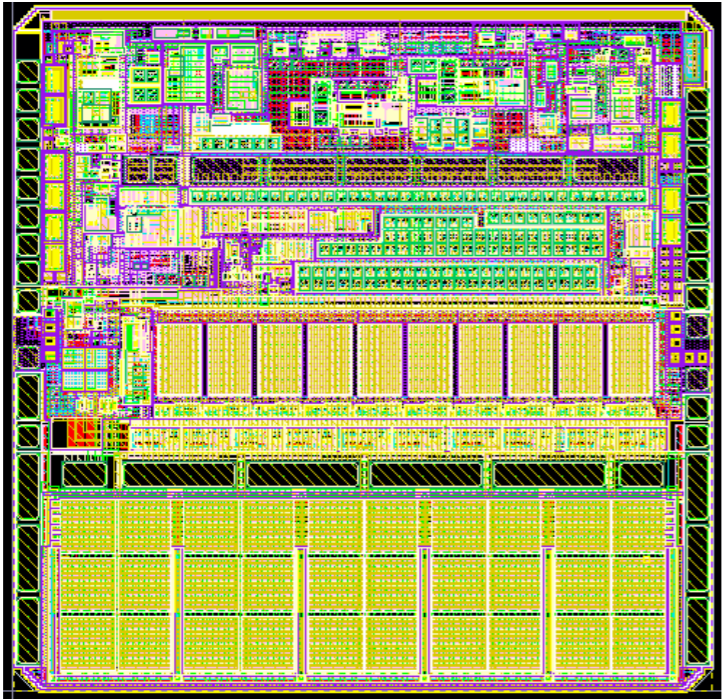
The bandgap is based on DTNMOS for reducing DD shift.
However this structure is more sensitive to TID.
This introduce in upFEAST a small Vout shift during TID irradiation and annealing

Layout of test chip with
4 Voltage generators



Bandgaps					
test		PNP (mV)	NPN (mV)	Vgs (mV)	DTNMOS (mV)
Mean BGP value 34 samples		1192	1238	573	602
TID shift	400Mrad	~10	~10	-30 and failed at 200Mrad	-35
Displacement Damage shift	1e15 n/cm2	62	77	-11	-7
	5e15 n/cm2	219	436	-32	-5
	1e16 n/cm2	403	792	-37	12

upFEAST



This new “sister” technology is more sensitive to substrate noise injection

The implant and resistance of the wells are different:

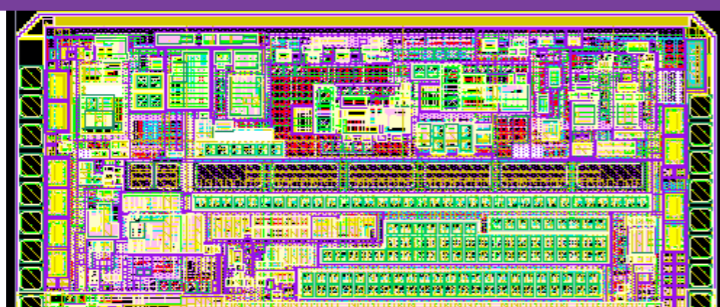
the substrate noise generated by the power transistors couples much more with the control circuitry.

A new ASIC, upFEAST2 has been designed to separate by 800um the control from the power transistors.

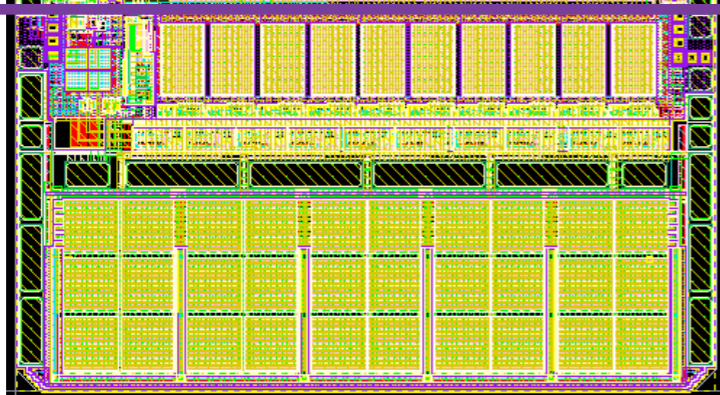
upFEAST2 has been submitted in February 2016, including also some other minor corrections.

upFEAST

**Control
Circuitry**

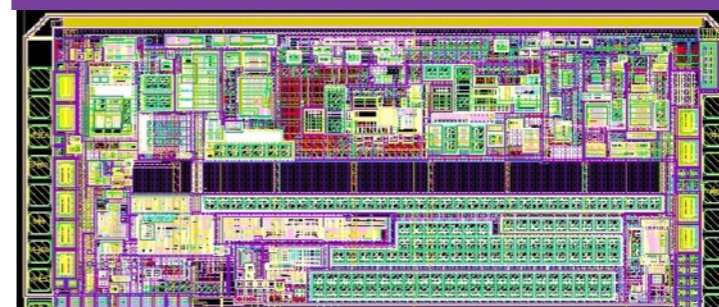


**Power
Transistors**



upFEAST2

**Control
Circuitry**



800um empty



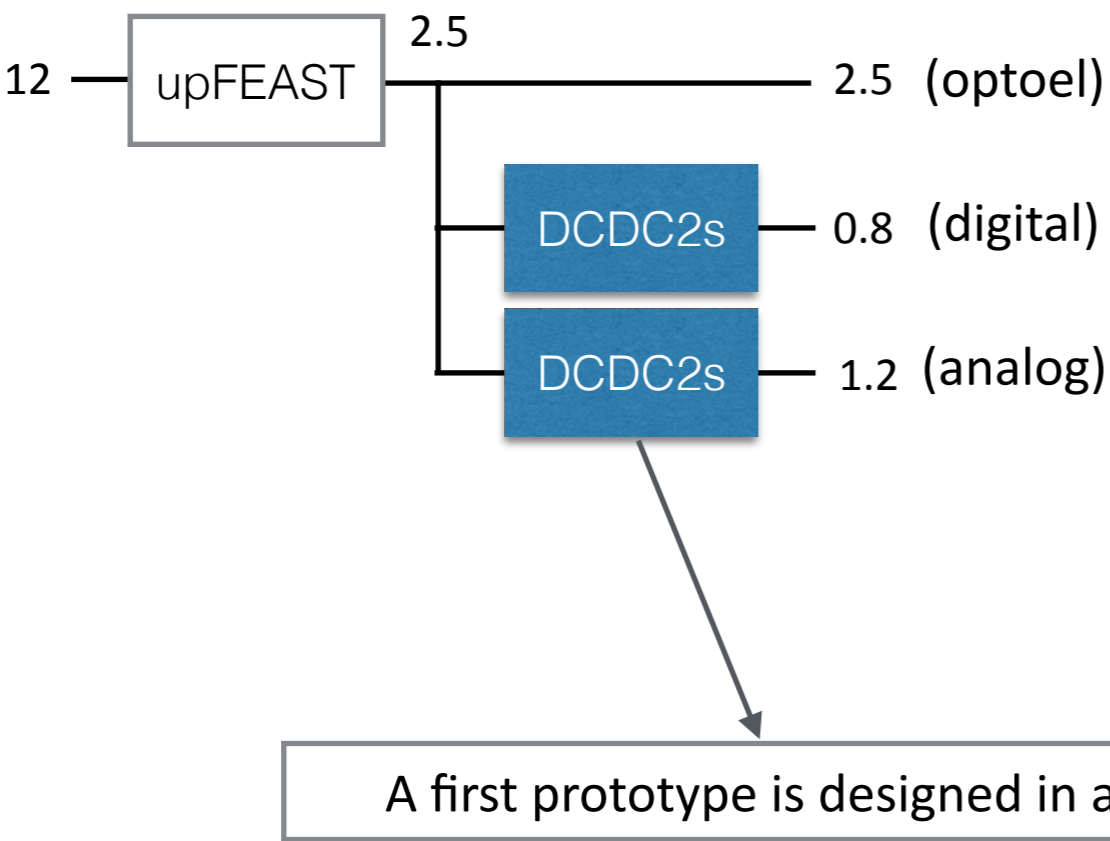
**Power
Transistors**



2nd Stage: DCDC2s

Second-stage DCDC converter to optimize power distribution in complex modules requiring different supply voltages

Useful in particular with FE readout ASICs in 130-65nm requiring 1.5-0.8V



Input voltage	2.0V ÷ 2.7V
Output voltage	0.6V ÷ 1.5V
Output current	≲ 3A (optimize @ 2A)
Switching frequency	> 4MHz
Inductor value	< 150nH
External components	Only C _{in} , C _{out} , L
Assembly	C4 Bump-bonding
Radiation Tolerance	
Total Ionising Dose	> 100 Mrad
Displacement Damage	> 4 10 ¹⁵ n/cm ²
SEEs: absence of destructive events and of output power interruptions	> 40 MeVcm ² mg ⁻¹

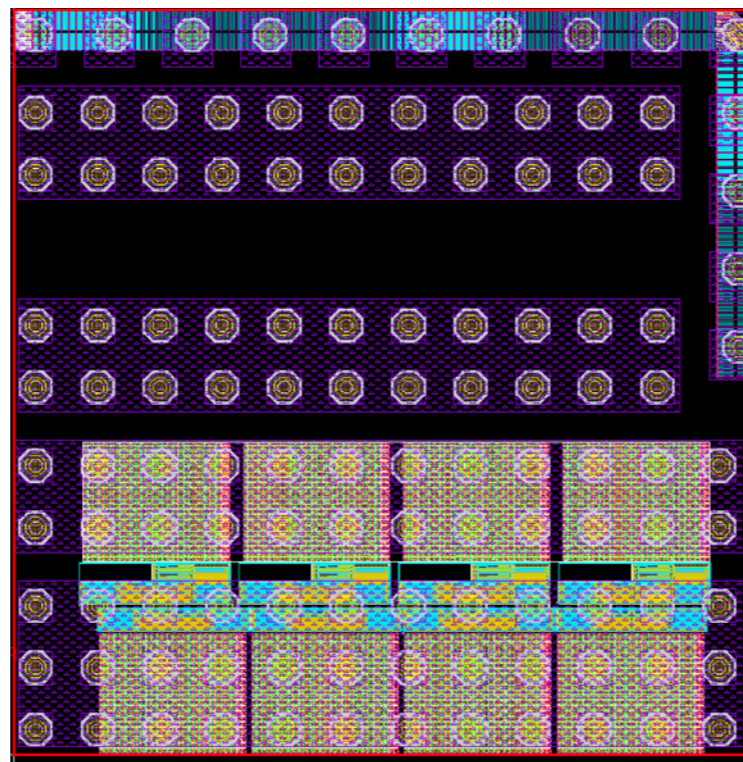
DCDC2S is today in design phase. We should be able to submit a first prototype by May 2016.

Chip size 2.1mm x 2.1mm, designed in a 130nm process with I/O transistors at 2.5V. It contains the most important building blocks (except some protections features).

C4 bumping is required to reduce the parasitic inductance in the current path. We work at the limit of the technology having an input Voltage on 2.5V and transistors that can stand nominally 2.5V.

A prototype with I/O transistors at 3.3V is foreseen to be designed this year.

A collaboration with EPFL is on going for simulating the substrate noise injection



Summary

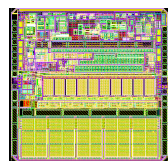
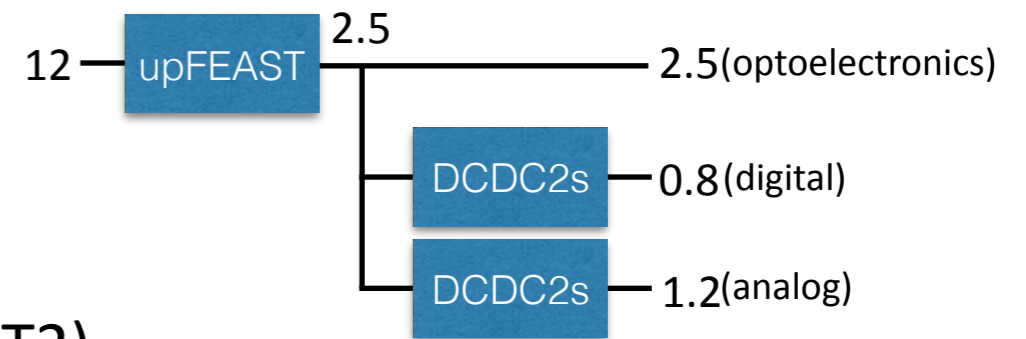
LHC upgrades:



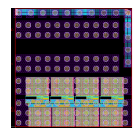
The FEASTMxx family of DCDC modules is in production and provides a plug-and-play solution for power distribution in LHC detector upgrades

ATLAS/CMS HL-LHC trackers upgrades

We are introducing new converters to extend the radiation tolerance and to optimize the on-module power distributions scheme when different voltages are required.



upFEAST: first prototype tested and a new version already in production (upFEAST2)



DCDC2S: first prototype in design phase, integration by May 2016