# The LpGBT Project
# Status and Overview

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On behalf of the GBT collaborations
2016/03/08

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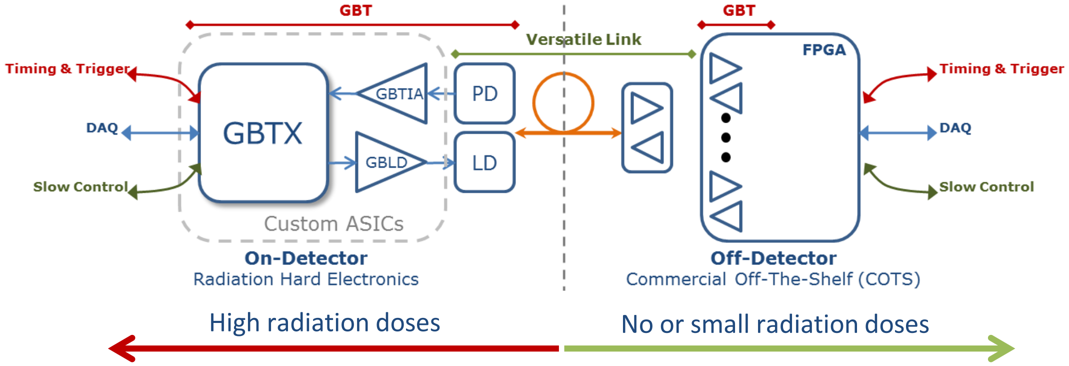
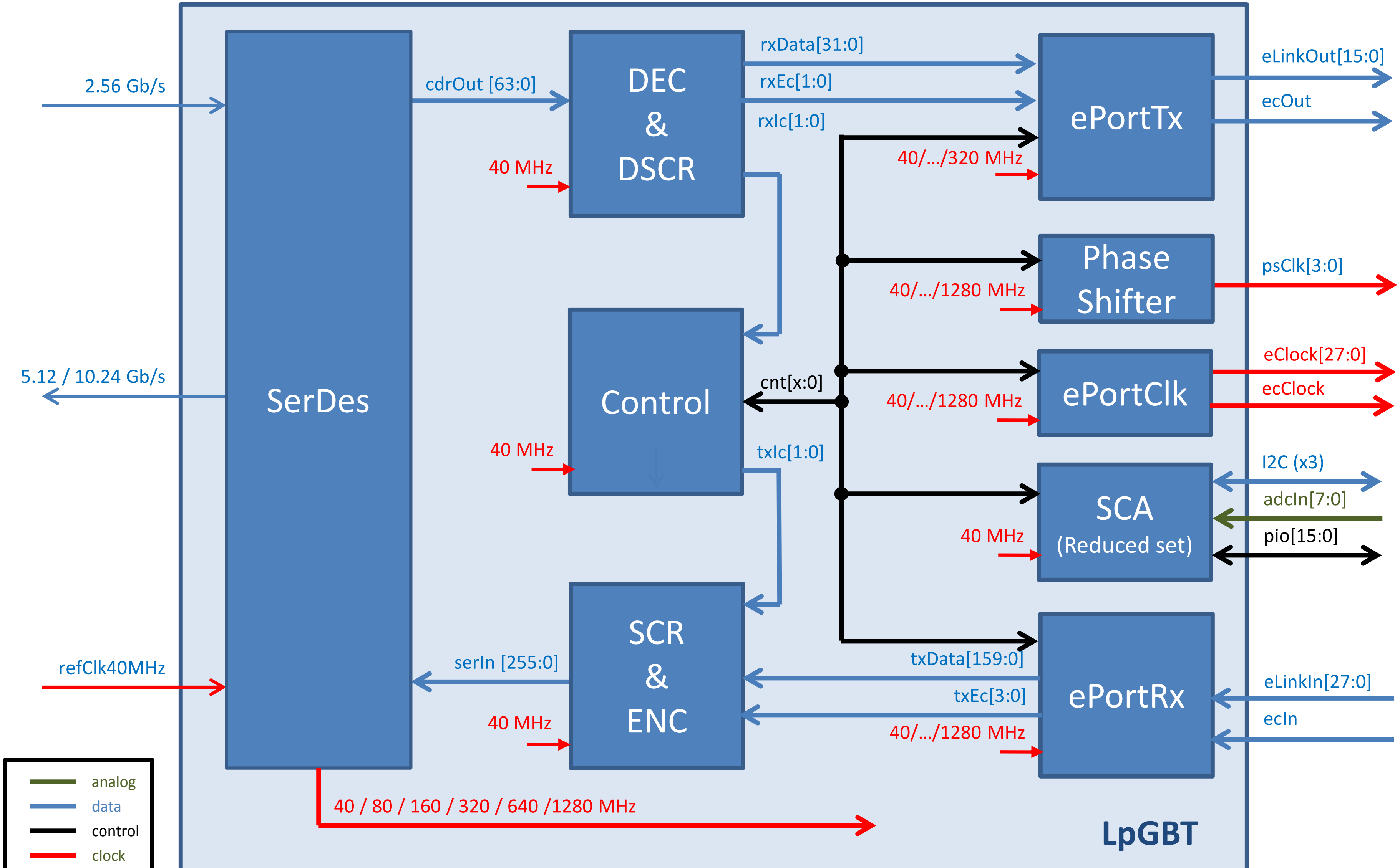
# The LpGBT & VL+ Project Objectives

- Development of Radiation Hard Optical Links
  - For the Phase II Upgrades of the experiments (HL – LHC)
    - Installation during the Long Shutdown 3 (Centred around ~2023)
- Main objectives
  - Data rates:
    - 5 to 10 Gb/s for up links
    - 2.5 Gb/s for down links
  - Environment
    - Temperature: -35 to + 60 °C
    - Total Dose: 100 Mrad qualification (200 Mrad LpGBT chipset)
    - Total Fluence: $2x10^{15}$ n/cm2 and $1x10^{15}$ hadrons/cm2
  - Reduce the power consumption of the data transmission systems
  - Reduce the footprint of the electronic and optoelectronic components
  - Optoelectronic components (VL+):
    - A low-profile package
    - Multiple channel and configurable:
      - Number of channels
      - Unidirectional / bidirectional



# LpGBT Block Diagram



# Main Features (1/…)

**"Optical" link:**

- Down-link:
  - 2.56 Gb/s (64 – bit frame)
  - Encoding: FEC12
  - User bandwidth:
    - IC (Internal Control (ASIC control)): 80 Mb/s
    - EC (External Control (SCA e-Link)): 80 Mb/s
    - D (Data): 1.28 Gb/s
  - Eye Scan
  - BER Monitoring based on the FEC activity
- Up-link:
  - User bandwidth @ 5.12 Gb/s (128 – bit frame):
    - IC: 80 Mb/s
    - EC: 80 Mb/s
    - D:
      - FEC12: 3.84 Gb/s
      - FEC5: 4.48 Gb/s
  - User bandwidth @ 10.24 Gb/s (256 – bit frame)
    - IC: 80 Mb/s
    - EC: 80 Mb/s
    - D:
      - FEC12: 7.68 Gb/s
      - FEC5: 8.96 Gb/s
  - Programable pre-emphasis

> - Down-link bandwidth require by the experiments is typically small (no need for 5 or 10 Gb/s):
>   - Experiment control
>   - Trigger information
> - Easier to achieve receiver SEU robustness at lower speeds!

# Main Features (2/…)

**E-Links**:

- Down-link:
  - Bandwidths: 80/160/320 Mb/s
  - Number of links*: 16/8/4
  - One EC channel @ 80 Mbit/s
- Up-Link:
  - FEC5 @ 5.12 Gb/s:
    - Data rate: 160 / 320 / 640 Mb/s
    - # eLinks*: 28 / 14 / 7
  - FEC5 @ 10.24 Gb/s:
    - Bandwidth: 320 / 640 / 1280 Mb/s
    - # eLinks*: 28 / 14 / 7
  - FEC12 @ 5.12 Gb/s:
    - Bandwidth: 160 / 320 / 640 Mb/s
    - # eLinks*: 24 / 12 / 6
  - FEC12 @ 10.24 Gb/s:
    - Bandwidth: 320 / 640 / 1280 Mb/s
    - # eLinks*: 24 / 12 / 6
  - One EC channel @ 80 Mbit/s
  - Phase alignment on a per channel basis:
    - User programable phase
    - Automatic phase tracking

* Excluding the EC channel

# Main Features (3/…)

**Latency**

- Both the RX and TX will have fixed and “deterministic” latency

**eLink Line Drivers**

- Programable:
  - Driving current: 1, 2 and 4 mA
  - Receiving end termination 100 Ω (external)
  - Pre-emphasis
  - Driver end termination (on/off - internal) (for back reflection cancelation)

**eLink Line Receivers**

- Programable:
  - 100 Ω differential terminations (on/off)
  - Auto bias for AC coupling (on/off)
  - Line equalization

# Main Features (4/...)

**Slow Control:**

- ASIC control:
  - IC channel: 80 Mb/s
  - I2C interface
- LpGBLD control:
  - I2C master
- Experiment control:
  - Two I2C masters
  - Programmable parallel port:
    - 16 x DIO
- Environmental parameters monitoring
  - 10-bit ADC:
    - 8 inputs
  - Temperature:
    - On chip: yes
    - Programable current source to drive an external temperature sensor

# Main Features (5/…)

**Clock distribution:**

- Phase/Frequency – 4 programmable clocks
  - 4 independent
  - Phase resolution: 50 ps
  - Frequencies: 40 / 80 / 160 / 320 / 640 / 1280 MHz
- eLink Clocks:
  - 28 independent
  - Fixed phase
  - Frequency programable:
    - 40 / 80 / 160 / 320 / 640 / 1280 MHz
- Clock jitter < 5 ps rms

**Power dissipation:**

- 500 mW @ 5.12 Gb/s
- 750 mW @ 10.24 Gb/s

**Radiation hardness:**

- Total dose:
  - 200 Mrad
- SEU robust

# Main Features (6/.)

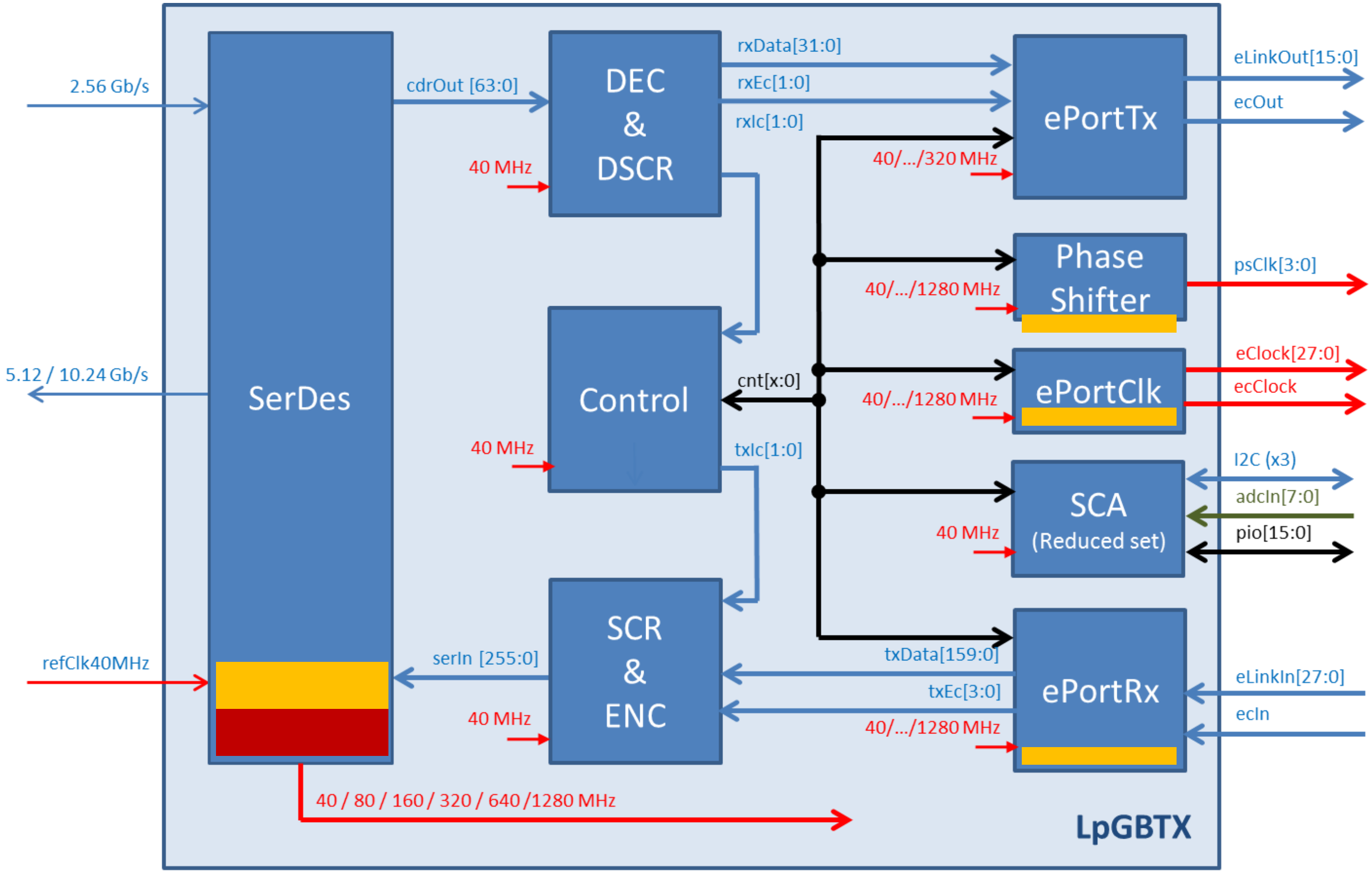
**Package:**

- BGA
- Fine Pitch:
  - 0.5 mm
- Pin count:
  - 289 (17 x 17)
- Size:
  - Our wish would be:
    - 9 mm x 9 mm x 2 mm
- Querying package providers for the availability of smaller packages.

| | # Ports | # Signals |
|---|---|---|
| **Optical Link** | | |
| Serial In | 1 | 2 |
| Serial Out | 1 | 2 |
| Power | 4 | 8 |
| **eLinks** | | |
| eLink Down | 16 | 32 |
| eLink Up | 28 | 56 |
| eLink Clock | 28 | 56 |
| eLink SC Down | 1 | 2 |
| eLink SC up | 1 | 2 |
| eLink SC Clock | 1 | 2 |
| Power | 9 | 18 |
| **ASIC Control** | | |
| SDA - asic | 1 | 1 |
| SCL - asic | 1 | 1 |
| I2C - address | 4 | 4 |
| RST | 1 | 1 |
| Transceiver Mode | 4 | 4 |
| Lock Mode | 2 | 2 |
| Ref CLK | 1 | 2 |
| Ref CLK Select | 1 | 1 |
| Power | 1 | 2 |
| **E-Fuse** | | |
| State overwrite | 1 | 1 |
| Ppulse | 1 | 1 |
| Power (x.xV) | 1 | 2 |
| **Test** | | |
| Test In | 4 | 4 |
| Test Out | 4 | 4 |
| **GBLD interface** | | |
| SDA - GBLD | 1 | 1 |
| SCL - GBLD | 1 | 1 |
| RST - GBLD | 1 | 1 |
| **Phase-Shifter** | | |
| Clock | 4 | 8 |
| Power | 4 | 8 |
| **I2C Master** | | |
| SDA - Master 1 & 2 | 2 | 2 |
| SCL - Master 1 & 2 | 2 | 2 |
| Power | 1 | 2 |
| **SC - Control interface** | | |
| Parallel I/O | 16 | 16 |
| DC/DC disable | 1 | 1 |
| Hard RST out | 2 | 2 |
| DC/DC power good | 3 | 3 |
| Power | 1 | 2 |
| **ADC** | | |
| Voltage Inputs | 8 | 8 |
| Temp Sens Input | 1 | 1 |
| **Digital** | | |
| Power | 4 | 8 |
| **Total # Pins** | | **276** |

Preliminary

# LpGBT Speed Domains




2.56 / 5.12 / 10.24 GHz clock domains

1.28 GHz clock domain

40 / 80 / 160 / 320 / 640 MHz clock domains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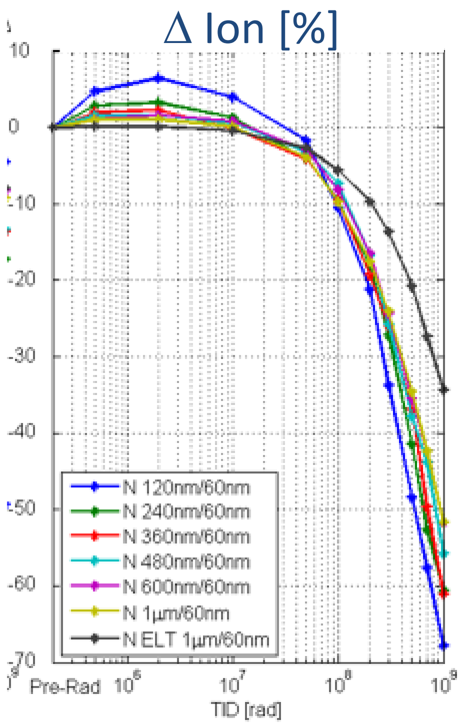
# TID "$I_{on}$" Degradation

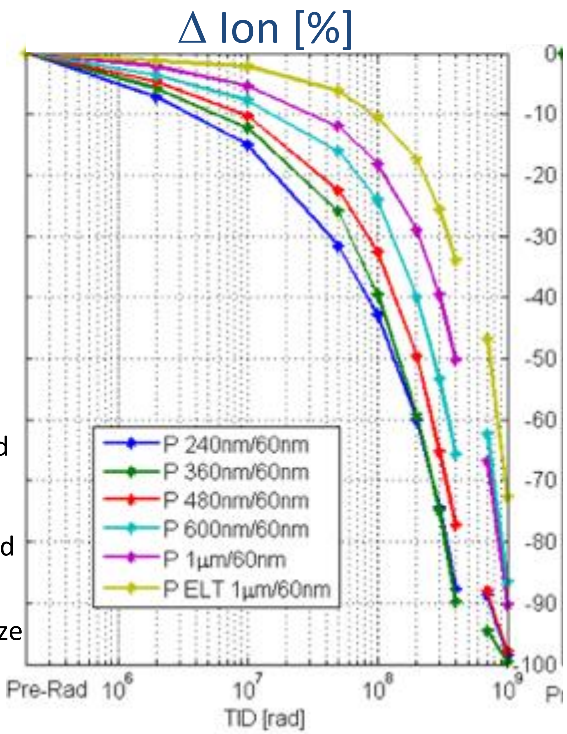
**NMOS**

- Moderately affected
- L dependent:
  - Longer is better
  - $L_{min}$ required for fast digital logic
- W dependent:
  - Wider is better
- Minimum size:
  - 10% @ 100 Mrad
- Enclosed devices:
  - The least affected
  - 5% @ 100 Mrad
  - Non minimum size




**PMOS**

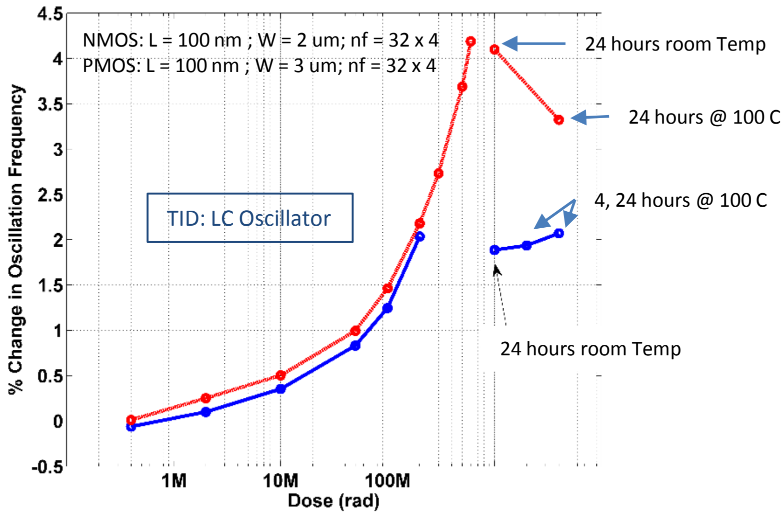
- Strongly affected
- L dependent:
  - Longer is better
  - $L_{min}$ required for fast digital logic
- W dependent:
  - Wider is better
- Minimum size:
  - 43% @ 100 Mrad
- Enclosed devices:
  - The least affected
  - 5% @ 100 Mrad
  - Non minimum size




- 2.56 / 5.12 / 10.24 GHz
  - CML logic will be used
  - Avoids the use of PMOS altogether ☺
  - It has a speed advantage ☺
  - It has a power penalty ☹
  - But, its use is restricted to a small fraction of the circuitry ☺

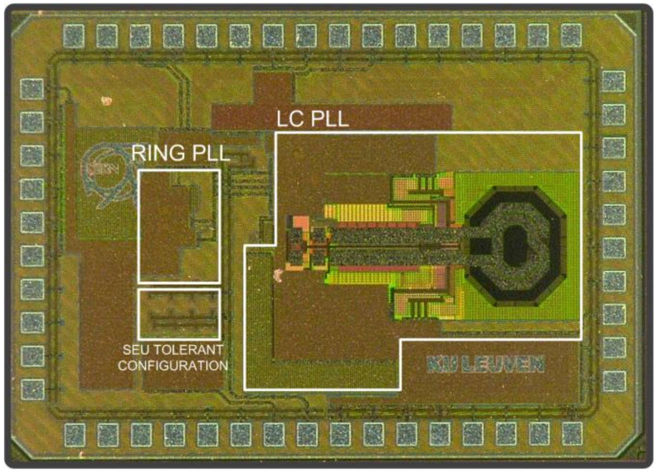
- 1.28 GHz
  - Logic cells will use enclosed devices
  - Devices non-minimum size:
    - Required anyway for fast digital
    - Small power penalty
- 40 / 80 / 160 / 320 / 640 MHz
  - Synergy with RD53
  - Non-minimum size devices
    - On R&D phase

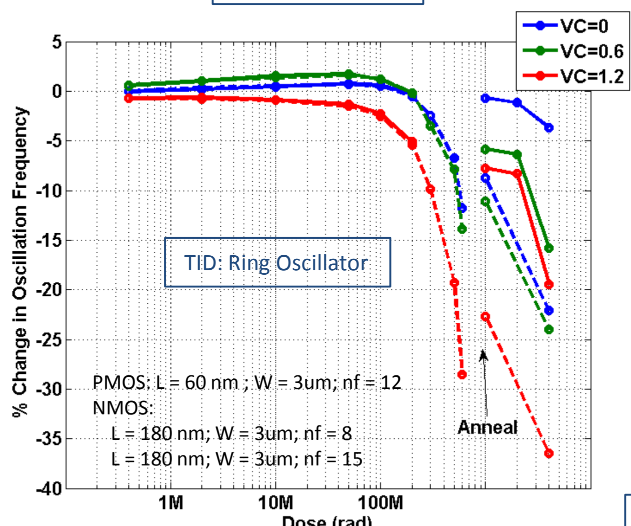
# Ring / LC oscillator test PLL – TID & SEU

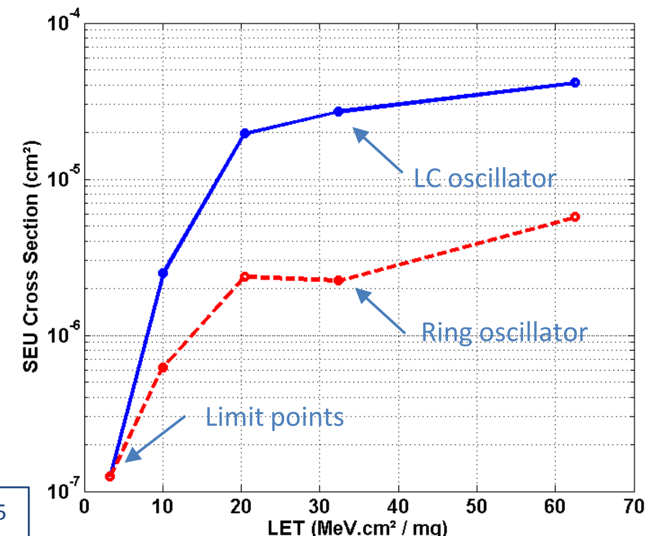



TID: 9 Mrad/hour

## 2.5 GHz PLL (LC & Ring Oscillators)




Paper submitted to NSREC 2015
J. Prinzie et. al.

# GBLD10

### Prototype:

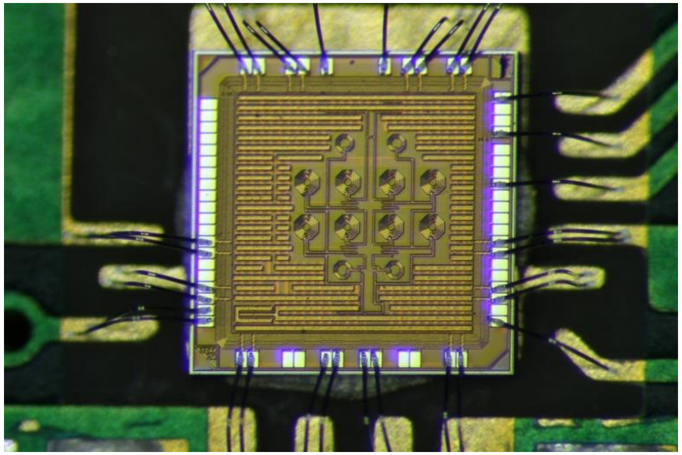
- A low-power 10 Gb/s laser driver was prototyped in 130 nm CMOS

### Main Features:

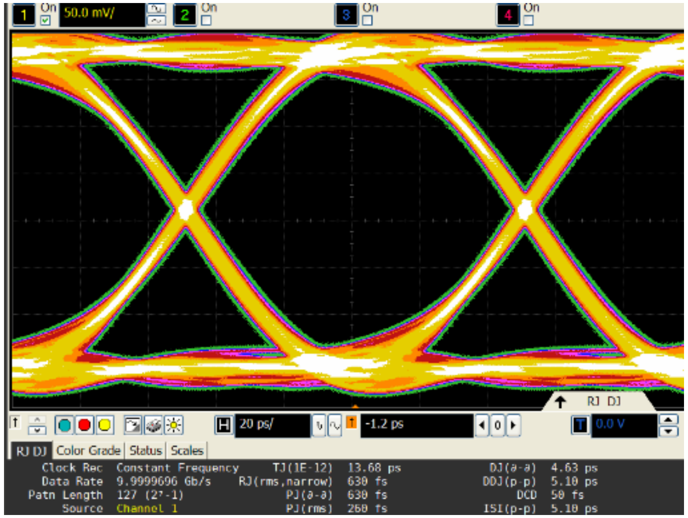
- **VCSEL driver**
- Laser coupling:
  - Differential AC with external components
- Minimum bit rate : **10 Gb/s**
- Programable pre-emphasis
- Modulation current: 0-12 mA
- Distributed amplifier structure
- QFN package, and ESD protection
- Area: 2mm x 2mm (same as GLBD)

### Measurement results:

- Data rate: > **10 Gb/s**
- Power dissipation: **86 mW** (typical settings)
- Jitter: **< 15 ps**
- Input Return Loss:
  - < -14 dB (0 – 5 GHz)
  - < -3 dB (10 GHz – 20GHz)
- Radiation hardness proved up to 500 Mrad
  - No annealing step



**Electrical Eye Diagram @ 10 Gb/s**




See: Zhang et all, TWEPP 2014, JINST 057P 1114

# GBLD10+

### Prototype:

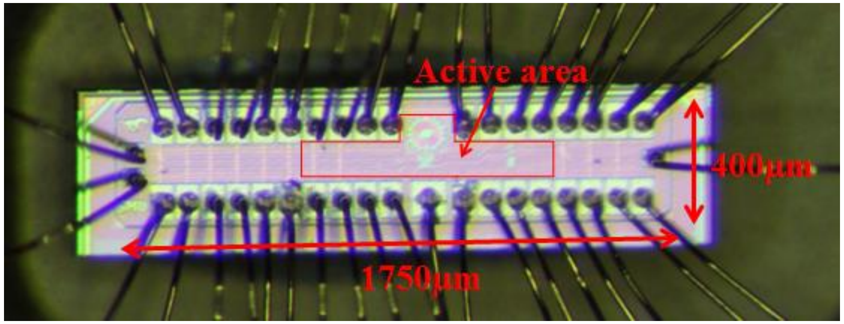
- A low-power / small-size 10 Gb/s laser driver was prototyped in 65 nm CMOS

### Main Features:

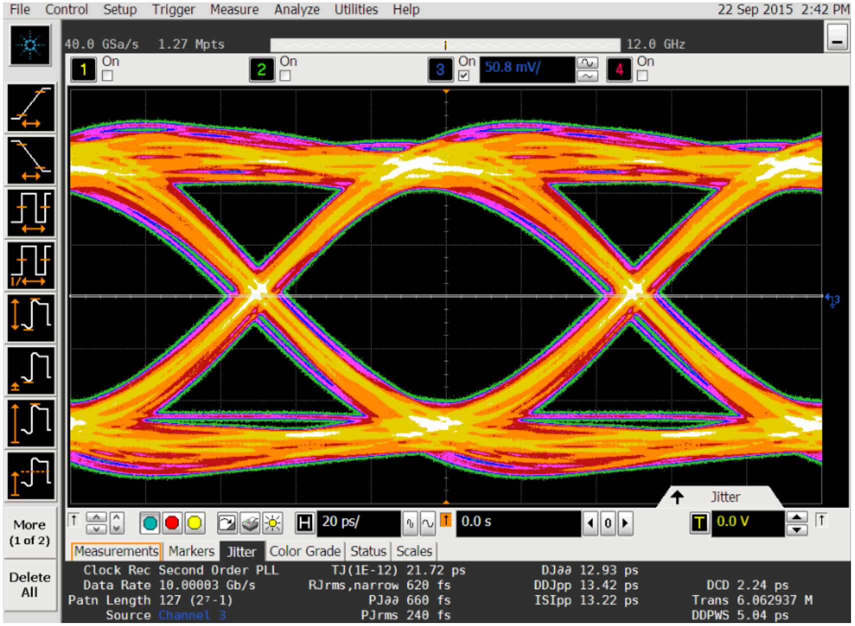
- **VCSEL driver**
- Laser coupling:
  - Single-ended direct bonding
- Minimum bit rate : **10 Gb/s**
- Programable rise/fall pre-emphasis
- Modulation current: 0-10 mA
- Biasing current 0-12 mA
- QFN package, and ESD protection
- Area: 1.75 mm x 0.4mm

### Measurement results (electrical only):

- Data rate: **10 Gb/s**
- Power dissipation: **31 mW** (typical settings)
- Jitter: **< 25 ps**



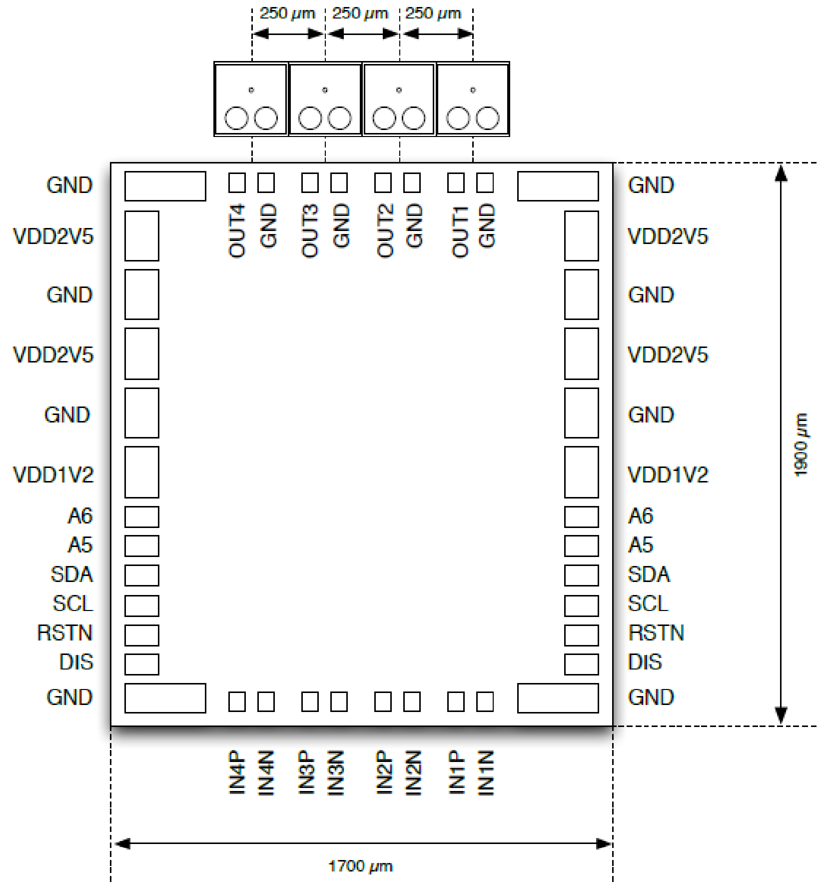

Electrical Eye Diagram @ 10 Gb/s




See: Zhang et all, TWEPP 2015

# VCSEL Driver Arrays

- Laser driver array being developed in Synergy with the VL+ project
  - See talk: "Versatile link+ also in use-cases without GBT" presentation by Csaba Soos in this workshop
- Two ASIC design projects ongoing by the departments of physics and engineering of the SMU university:
  - 4-way VCSEL driver array
  - Single ended driving
  - Internal bias
  - Designed for direct bonding VCSEL arrays
  - Modulation and bias currents programable through I2C
  - Designs submitted for prototyping Feb 2016:
    - Prototype testing foreseen for May 2016



# LpGBT ASIC Development Status

- Hardware
  - Ring and LC oscillator based PLL to test for SEU and TID (previous pages)
  - 10 Gb/s line driver:
    - Programmable pre-emphasis (up to 10 dB)
  - Fast digital library (90%)
    - Enclosed layout for TID robustness
    - Submission of a tests chip on the 23th of March (In collaboration with RD53)
  - Phase-aligner DLL (80%)
  - ePort Driver / Receiver (30%)
- RTL
  - I2C Slave
  - I2C Master
  - IC link
  - Scrambler/Descrambler
  - ePort RX/TX (80% complete)

# LpGBT Project Schedule

**LpGBT**

- **Specification Q2 2015**
- **Full chip prototype out for manufacture Q4 2016**
- **Full chip prototype testing Q3 – Q4 2017**
- **Final Engineering run sent out Q2 2018**
- **First production batch available for users Q4 2019**
- **Completion of production Q4 2020**

# LpGBT Collaboration

- CERN
  - Sophie Barron
  - Rui Francisco
  - Szymon Kulis
  - Pedro Leitão
  - Raul Lesma
  - Alessandro Marchioro
  - Paulo Moreira
  - David Porret
  - Ken Wyllie
- KU Leuven
  - Bram Faes
  - Paul Leroux
  - Jeffrey Prinzie
- SMU
  - Datao Gong
  - Ping Gui
  - Di Guo
  - Dongxu Yang
  - Jingbo Ye
  - Zhiyao Zeng
  - Tao Zhang

# GBT Chipset Status

- GBTIA
  - All wafers produced
  - 26,000 chips diced and tested
  - Quantities required for VTTRx available.
- GBLD
  - All the wafers produced
  - 94,000 chips packaged
  - 22,250 chips tested (remaining devices will be all tested during March)
  - Quantities required for VTTRx and VTTX available March
- GBTX
  - Pre-series production completed (approx. 900 devices)
  - Production testing to be done during April
    - Pre-production chips available for distribution in May
  - First-production lot (14,000 pieces):
    - Launched April 2016
    - Chips available for distribution, June 2016
  - Production complete, September 2016
- GBT – SCA
  - Submitted for prototype fabrication, November 2015
  - Wafers expected end March
  - In house packaging April (general purpose ceramic package)
  - ASIC evaluation testing, April
  - SEU and TID qualification, May
  - Wafer production, June
  - Wafers available, October
  - Packaged parts available in production quantities, Q1 2017