The LpGBT Project
Status and Overview

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On behalf of the GBT collaborations
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• The LpGBT & VL+ Project Objectives
• The LpGBT ASIC
  – LpGBT Block Diagram
  – Main Features:
    • Optical Link
    • E-Links
    • Slow Control
    • Clock Distribution
    • Power Dissipation
    • Radiation Hardness
    • Package
  – The ASIC and Radiation
    • LpGBT Speed Domains
    • TID “I_{on}” Degradation
    • Ring / LC oscillator test PLL
      – TID & SEU
• Project developments
  – GBLD10
  – GBLD10+
  – VCSEL Driver Arrays
• LpGBT ASIC Development Status
• LpGBT Project Schedule
• GBT Chipset Status
The LpGBT & VL+ Project Objectives

• Development of Radiation Hard Optical Links
  – For the Phase II Upgrades of the experiments (HL – LHC)
    • Installation during the Long Shutdown 3 (Centred around ~2023)
• Main objectives
  – Data rates:
    • 5 to 10 Gb/s for up links
    • 2.5 Gb/s for down links
  – Environment
    • Temperature: -35 to + 60 °C
    • Total Dose: 100 Mrad qualification (200 Mrad LpGBT chipset)
    • Total Fluence: $2 \times 10^{15}$ n/cm² and $1 \times 10^{15}$ hadrons/cm²
  – Reduce the power consumption of the data transmission systems
  – Reduce the footprint of the electronic and optoelectronic components
  – Optoelectronic components (VL+):
    • A low-profile package
    • Multiple channel and configurable:
      – Number of channels
      – Unidirectional / bidirectional

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LpGBT Block Diagram

- SerDes
  - refClk40MHz
  - 5.12 / 10.24 Gb/s
  - 2.56 Gb/s
- Control
  - cnt[x:0]
  - txlc[1:0]
  - serIn [255:0]
  - 40 MHz
- SCR & ENC
  - serIn [255:0]
  - 40 MHz
- DEC & DSCR
  - cdrOut [63:0]
  - 40 MHz
- ePortClk
  - cnt[x:0]
  - txlc[1:0]
  - txData[159:0]
  - 40 MHz
- SCA (Reduced set)
  - cnt[x:0]
  - txlc[1:0]
  - txData[159:0]
  - 40 MHz
- ePortRx
  - cnt[x:0]
  - txlc[1:0]
  - txData[159:0]
  - 40 MHz
- ePortTx
  - eLinkOut[15:0]
  - ecOut
  - 40/…/320 MHz
- Phase Shifter
  - 40/…/1280 MHz
  - psClk[3:0]
  - eClock[27:0]
  - ecClock
- ePortClk
  - 40/…/1280 MHz
  - adcIn[7:0]
  - pio[15:0]
- LpGBT
  - ePortClk
  - ePortTx
  - ePortRx
  - eLinkIn[27:0]
  - eClk
  - 40 MHz
  - 40/…/320 MHz
  - 40 / 80 / 160 / 320 / 640 / 1280 MHz

Colors:
- green: analog
- blue: data
- black: control
- red: clock
Main Features (1/…)

“Optical” link:

• **Down-link:**
  - 2.56 Gb/s (64 – bit frame)
  - Encoding: FEC12
  - User bandwidth:
    • IC (Internal Control (ASIC control)): 80 Mb/s
    • EC (External Control (SCA e-Link)): 80 Mb/s
    • D (Data): 1.28 Gb/s
  - Eye Scan
  - BER Monitoring based on the FEC activity

• **Up-link:**
  - User bandwidth @ 5.12 Gb/s (128 – bit frame):
    • IC: 80 Mb/s
    • EC: 80 Mb/s
    • D:
      - FEC12: 3.84 Gb/s
      - FEC5: 4.48 Gb/s
  - User bandwidth @ 10.24 Gb/s (256 – bit frame)
    • IC: 80 Mb/s
    • EC: 80 Mb/s
    • D:
      - FEC12: 7.68 Gb/s
      - FEC5: 8.96 Gb/s
  - Programable pre-emphasis

**Down-link bandwidth require by the experiments is typically small (no need for 5 or 10 Gb/s):**
- Experiment control
- Trigger information
- Easier to achieve receiver SEU robustness at lower speeds!
Main Features (2/...)

E-Links:

- **Down-link:**
  - Bandwidths: 80/160/320 Mb/s
  - Number of links*: 16/8/4
  - One EC channel @ 80 Mbit/s

- **Up-Link:**
  - FEC5 @ 5.12 Gb/s:
    - Data rate: 160 / 320 / 640 Mb/s
    - # eLinks*: 28 / 14 / 7
  - FEC5 @ 10.24 Gb/s:
    - Bandwidth: 320 / 640 / 1280 Mb/s
    - # eLinks*: 28 / 14 / 7
  - FEC12 @ 5.12 Gb/s:
    - Bandwidth: 160 / 320 / 640 Mb/s
    - # eLinks*: 24 / 12 / 6
  - FEC12 @ 10.24 Gb/s:
    - Bandwidth: 320 / 640 / 1280 Mb/s
    - # eLinks*: 24 / 12 / 6
  - One EC channel @ 80 Mbit/s
  - Phase alignment on a per channel basis:
    - User programable phase
    - Automatic phase tracking

* Excluding the EC channel
Main Features (3/…)

Latency
• Both the RX and TX will have fixed and “deterministic” latency

eLink Line Drivers
• Programable:
  – Driving current: 1, 2 and 4 mA
  – Receiving end termination 100 Ω (external)
  – Pre-emphasis
  – Driver end termination (on/off - internal) (for back reflection cancelation)

eLink Line Receivers
• Programable:
  – 100 Ω differential terminations (on/off)
  – Auto bias for AC coupling (on/off)
  – Line equalization
Main Features (4/…)

**Slow Control:**

- **ASIC control:**
  - IC channel: 80 Mb/s
  - I2C interface

- **LpGBLD control:**
  - I2C master

- **Experiment control:**
  - Two I2C masters
  - Programmable parallel port:
    - 16 x DIO

- **Environmental parameters monitoring**
  - 10-bit ADC:
    - 8 inputs
  - Temperature:
    - On chip: yes
    - Programmable current source to drive an external temperature sensor
Main Features (5/...)

Clock distribution:
• Phase/Frequency – 4 programmable clocks
  – 4 independent
  – Phase resolution: 50 ps
  – Frequencies: 40 / 80 / 160 / 320 / 640 / 1280 MHz
• eLink Clocks:
  – 28 independent
  – Fixed phase
  – Frequency programable:
    • 40 / 80 / 160 / 320 / 640 / 1280 MHz
• Clock jitter < 5 ps rms

Power dissipation:
• 500 mW @ 5.12 Gb/s
• 750 mW @ 10.24 Gb/s

Radiation hardness:
• Total dose:
  – 200 Mrad
• SEU robust
Main Features (6/.)

Package:
- **BGA**
- **Fine Pitch:**
  - 0.5 mm
- **Pin count:**
  - 289 (17 x 17)
- **Size:**
  - Our wish would be:
    - 9 mm x 9 mm x 2 mm
- Querying package providers for the availability of smaller packages.

## Ports & Signals

<table>
<thead>
<tr>
<th>Feature</th>
<th># Ports</th>
<th># Signals</th>
</tr>
</thead>
<tbody>
<tr>
<td>Optical Link</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Serial In</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>Serial Out</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>Power</td>
<td>4</td>
<td>8</td>
</tr>
<tr>
<td>eLinks</td>
<td></td>
<td></td>
</tr>
<tr>
<td>eLink Down</td>
<td>16</td>
<td>32</td>
</tr>
<tr>
<td>eLink Up</td>
<td>28</td>
<td>56</td>
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<tr>
<td>eLink Clock</td>
<td>28</td>
<td>56</td>
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<tr>
<td>eLink SC Down</td>
<td>1</td>
<td>2</td>
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<tr>
<td>eLink SC up</td>
<td>1</td>
<td>2</td>
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<tr>
<td>eLink SC Clock</td>
<td>1</td>
<td>2</td>
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<tr>
<td>Power</td>
<td>9</td>
<td>18</td>
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<tr>
<td>ASIC Control</td>
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<td></td>
</tr>
<tr>
<td>SDA -asic</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>SCL -asic</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>I2C -address</td>
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</tr>
<tr>
<td>RST</td>
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</tr>
<tr>
<td>Transceiver Mode</td>
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<tr>
<td>Lock Mode</td>
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<tr>
<td>Ref CLK</td>
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<tr>
<td>Ref CLK Select</td>
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<tr>
<td>Power</td>
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<tr>
<td>E-Fuse</td>
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<tr>
<td>State overwrite</td>
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<td>Ppulse</td>
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<tr>
<td>Power (x.xV)</td>
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<tr>
<td>Test</td>
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<td>Test Clock</td>
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<tr>
<td>GBLD Interface</td>
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<td>SDA - GBLD</td>
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<td>1</td>
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<tr>
<td>SCL - GBLD</td>
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<td>1</td>
</tr>
<tr>
<td>RST - GBLD</td>
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<td>1</td>
</tr>
<tr>
<td>Power - GBLD</td>
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</tr>
<tr>
<td>Clock</td>
<td>4</td>
<td>8</td>
</tr>
<tr>
<td>Test</td>
<td>4</td>
<td>8</td>
</tr>
<tr>
<td>I2C Master</td>
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<td></td>
</tr>
<tr>
<td>SDA - Master 1 &amp; 2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>SCL - Master 1 &amp; 2</td>
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<tr>
<td>Power</td>
<td>1</td>
<td>2</td>
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<tr>
<td>SC - Control interface</td>
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<tr>
<td>Parallel I/O</td>
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<tr>
<td>DC/DC disable</td>
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<tr>
<td>Hard RST out</td>
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<td>DC/DC power good</td>
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<tr>
<td>Power</td>
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<td>2</td>
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<tr>
<td>ADC</td>
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<tr>
<td>Voltage Inputs</td>
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<tr>
<td>Temp Sens Input</td>
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<tr>
<td>Digital</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Power</td>
<td>4</td>
<td>8</td>
</tr>
<tr>
<td><strong>Total # Pins</strong></td>
<td><strong>276</strong></td>
<td></td>
</tr>
</tbody>
</table>
LpGBT Speed Domains

2.56 / 5.12 / 10.24 GHz clock domains

1.28 GHz clock domain

40 / 80 / 160 / 320 / 640 MHz clock domains
**TID “I\text{on}” Degradation**

**NMOS**
- Moderately affected
- **L** dependent:
  - Longer is better
  - \( L_{\text{min}} \) required for fast digital logic
- **W** dependent:
  - Wider is better
- Minimum size:
  - 10% @ 100 Mrad
- Enclosed devices:
  - The least affected
  - 5% @ 100 Mrad
  - Non minimum size

**2.56 / 5.12 / 10.24 GHz**
- CML logic will be used
- Avoids the use of PMOS altogether 😊
- It has a speed advantage 😊
- It has a power penalty 😞
- But, its use is restricted to a small fraction of the circuitry 😊

**PMOS**
- Strongly affected
- **L** dependent:
  - Longer is better
  - \( L_{\text{min}} \) required for fast digital logic
- **W** dependent:
  - Wider is better
- Minimum size:
  - 43% @ 100 Mrad
- Enclosed devices:
  - The least affected
  - 5% @ 100 Mrad
  - Non minimum size

**1.28 GHz**
- Logic cells will use enclosed devices
- Devices non-minimum size:
  - Required anyway for fast digital
  - Small power penalty

**40 / 80 / 160 / 320 / 640 MHz**
- Synergy with RD53
- Non-minimum size devices
  - On R&D phase

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Ring / LC oscillator test PLL – TID & SEU

2.5 GHz PLL (LC & Ring Oscillators)

TID: 9 Mrad/hour

PMOS: L = 60 nm; W = 3um; nf = 12
NMOS: L = 180 nm; W = 3um; nf = 8
L = 180 nm; W = 3um; nf = 15

NMOS: L = 100 nm; W = 2um; nf = 32 x 4
PMOS: L = 100 nm; W = 3 um; nf = 32 x 4

Vc=0
VC=0.6
VC=1.2

Paper submitted to NSREC 2015
J. Prinzie et. al.
Prototype:
• A low-power 10 Gb/s laser driver was prototyped in 130 nm CMOS

Main Features:
• VCSEL driver
• Laser coupling:
  – Differential AC with external components
• Minimum bit rate: **10 Gb/s**
• Programable pre-emphasis
• Modulation current: 0-12 mA
• Distributed amplifier structure
• QFN package, and ESD protection
• Area: 2mm x 2mm (same as GLBD)

Measurement results:
• Data rate: > **10 Gb/s**
• Power dissipation: **86 mW** (typical settings)
• Jitter: < **15 ps**
• Input Return Loss:
  – < -14 dB (0 – 5 GHz)
  – < -3 dB (10 GHz – 20GHz)
• Radiation hardness proved up to 500 Mrad
  – No annealing step

See: Zhang et all, TWEPP 2014, JINST 057P 1114
Prototype:
- A low-power / small-size 10 Gb/s laser driver was prototyped in 65 nm CMOS

Main Features:
- VCSEL driver
- Laser coupling:
  - Single-ended direct bonding
- Minimum bit rate: **10 Gb/s**
- Programmable rise/fall pre-emphasis
- Modulation current: 0-10 mA
- Biasing current 0-12 mA
- QFN package, and ESD protection
- Area: 1.75 mm x 0.4mm

Measurement results (electrical only):
- Data rate: **10 Gb/s**
- Power dissipation: **31 mW** (typical settings)
- Jitter: < **25 ps**

See: Zhang et al, TWEPP 2015

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VCSEL Driver Arrays

- Laser driver array being developed in Synergy with the VL+ project
  - See talk: “Versatile link+ also in use-cases without GBT” presentation by Csaba Soos in this workshop

- Two ASIC design projects ongoing by the departments of physics and engineering of the SMU university:
  - 4-way VCSEL driver array
  - Single ended driving
  - Internal bias
  - Designed for direct bonding VCSEL arrays
  - Modulation and bias currents programable through I2C
  - Designs submitted for prototyping Feb 2016:
    - Prototype testing foreseen for May 2016

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LpGBT ASIC Development Status

**Hardware**
- Ring and LC oscillator based PLL to test for SEU and TID (previous pages)
- 10 Gb/s line driver:
  - Programmable pre-emphasis (up to 10 dB)
- Fast digital library (90%)
  - Enclosed layout for TID robustness
  - Submission of a tests chip on the 23\textsuperscript{th} of March (In collaboration with RD53)
- Phase-aligner DLL (80%)
- ePort Driver / Receiver (30%)

**RTL**
- I2C Slave
- I2C Master
- IC link
- Scrambler/Descrambler
- ePort RX/TX (80% complete)

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LpGBT Project Schedule

LpGBT

• Specification Q2 2015
• Full chip prototype out for manufacture Q4 2016
• Full chip prototype testing Q3 – Q4 2017
• Final Engineering run sent out Q2 2018
• First production batch available for users Q4 2019
• Completion of production Q4 2020
LpGBT Collaboration

• CERN
  – Sophie Barron
  – Rui Francisco
  – Szymon Kulis
  – Pedro Leitão
  – Raul Lesma
  – Alessandro Marchioro
  – Paulo Moreira
  – David Porret
  – Ken Wyllie

• KU Leuven
  – Bram Faes
  – Paul Leroux
  – Jeffrey Prinzie

• SMU
  – Datao Gong
  – Ping Gui
  – Di Guo
  – Dongxu Yang
  – Jingbo Ye
  – Zhiyao Zeng
  – Tao Zhang
GBT Chipset Status

- **GBTIA**
  - All wafers produced
  - 26,000 chips diced and tested
  - Quantities required for VTTRx available.

- **GBLD**
  - All the wafers produced
  - 94,000 chips packaged
  - 22,250 chips tested (remaining devices will be all tested during March)
  - Quantities required for VTTRx and VTX available March

- **GBTX**
  - Pre-series production completed (approx. 900 devices)
  - Production testing to be done during April
    - Pre-production chips available for distribution in May
  - First-production lot (14,000 pieces):
    - Launched April 2016
    - Chips available for distribution, June 2016
  - Production complete, September 2016

- **GBT – SCA**
  - Submitted for prototype fabrication, November 2015
  - Wafers expected end March
  - In house packaging April (general purpose ceramic package)
  - ASIC evaluation testing, April
  - SEU and TID qualification, May
  - Wafer production, June
  - Wafers available, October
  - Packaged parts available in production quantities, Q1 2017

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