RD53: status and main activities for 2016

Elia Conti on behalf of the RD53 Collaboration

ACES 2016 – Fifth Common ATLAS CMS Workshop for LHC Upgrades – 09/03/2016

- Introduction
- Status of working groups
- Small scale prototypes (2015-2016)
- Main activities for 2016
  - Digital radiation test chip (DRAD)
  - RD53A Demonstrator
- Conclusion

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Next generation of silicon pixel detectors for phase-2 upgrade of ATLAS and CMS at HL-LHC sets unprecedented design requirements

- Small pixels (50x50 μm^2 / 25x100 μm^2)
- Large chips (~2x2 cm^2, ~10^9 transistors)
- Hit rate up to more than 3 GHz/cm^2 (high pileup ~200)
- Radiation tolerance: 1 Grad TID, 2x10^{16} n_{eq}/cm^2
- Trigger rate up to 1 MHz, ~12.5 μs trigger latency

Goals of RD53 (65 nm technology)

- Radiation qualification and characterization in 65 nm → guidelines for radiation hardness
- Development of tools and methodology to efficiently design large complex mixed signal chips
- Design and characterization of circuits and building blocks needed for pixel chips
  → design of shared rad-hard IP library
- Design and characterization of full scale demonstrator pixel chip

RD53 Working Groups (WGs)

Radiation WG | Analog WG | IP WG | Simulation WG | Top level and chip integration WG | I/O WG

~20 participating institutes: Bari, Bonn, CERN, CPPM, FNAL, LBNL, LPNHE Paris, NIKHEF, New Mexico, Milano, Padova, Pavia-Bergamo, Pisa, Perugia, Prague IP-FNSPE-CTU, PSI, RAL, Torino, UC Santa Cruz, Sevilla

RD53 collaboration website: http://rd53.web.cern.ch/RD53/

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Radiation WG

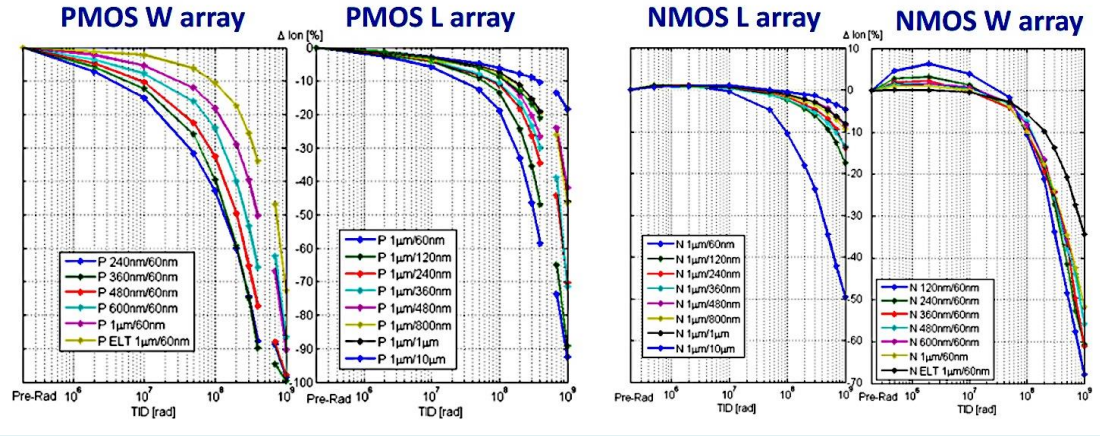
– Extensive investigations at *single transistor level* (CERN, CPPM, FNAL, Padova) on sensitivity to various parameters (NMOS vs PMOS, geometry W/L, influence of temperature, bias, during irradiation / during annealing phase…)

– It was eventually realized that 1 Grad is impossible to guarantee at current times
  - moved our goal to **500 Mrad**
  - **replacement strategy** must be applied for innermost pixel layers

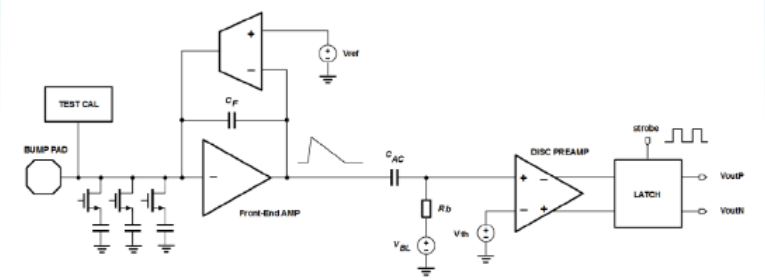
– *Analog* front end prototypes do not feature major degradation up to 500 Mrad thanks to the use of large transistors

– It has to be ensured that *digital* circuitry can be made to operate up to 500 Mrad by still using very small transistors (to obtain density required for hit buffering due to high hit rates and long latency)

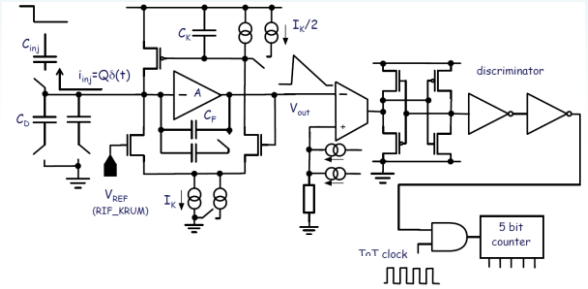
TID Effects in 65nm Transistors: Summary of a Long Irradiation Study at the CERN X-rays Facility [F. Faccio, TWEPP 2015]



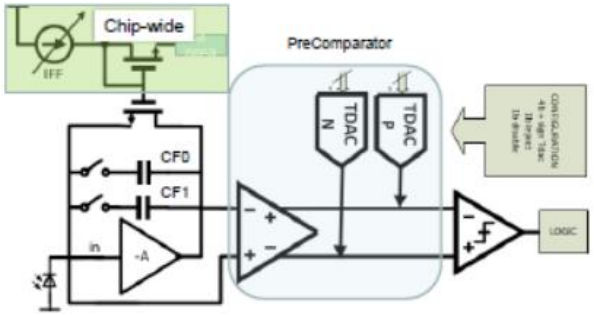
Analog WG



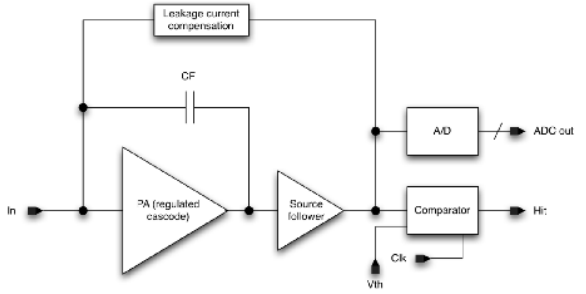
INFN Torino – single stage with SAR-like ToT counter using synchronous comparator



INFN Bergamo/Pavia – single stage with current comparator and ToT counter



LBNL – continuous reset integrator first stage + DC-coupled pre-comparator stage



FNAL – zero dead time and flash ADC (submission planned Q1 2016)

3 different analog front ends have been **prototyped and tested**

IP WG

~25 IPs have been prototyped and (most of them) tested

- Biasing and testing of front end (e.g. bandgap, DAC, test pulse)
- Monitoring (e.g. temperature sensor)
- IO (e.g. serializer, cable driver)
- Power (e.g. shunt-LDO, power-on reset)
- Digital (rad-hard standard cell and memories)

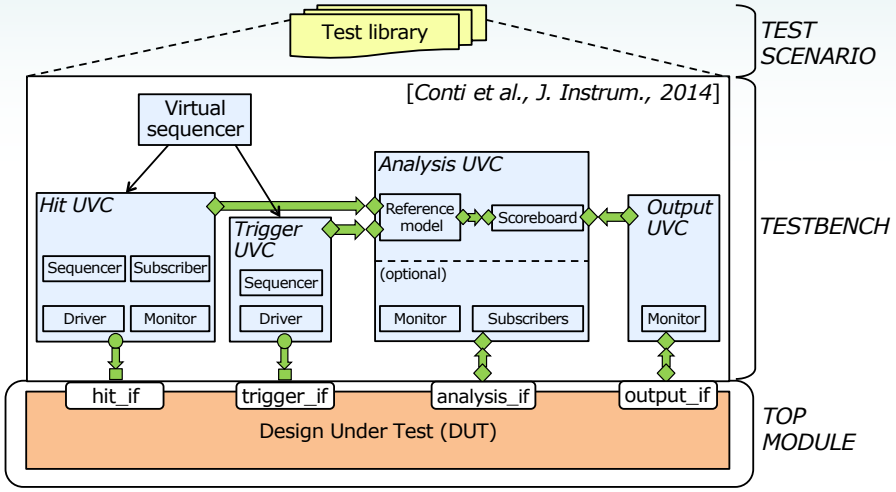
I/O WG

Input and output protocols have been proposed

- Input (command/control incl. trigger)
  - single input line
  - 160 Mbit/s DC balanced constant stream using custom 8-bit symbol pairs
  - single bit error correction through symbol duplication
- Output (data/configuration)
  - 5 Gbit/s total output bandwidth obtained with single or double (4?) link
  - DC balanced
  - simplified version of Xilinx Aurora protocol

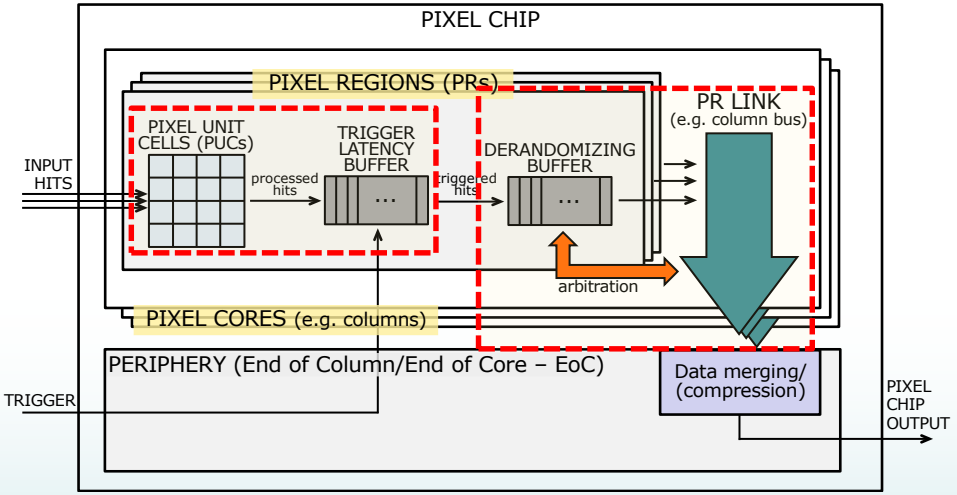
Simulation WG

VEPIX53 framework developed
(SystemVerilog/UVM)



– Performed architecture exploration with *behavioral* (non-synthesizable) parameterized pixel chip model
  - Study of trigger latency buffering (hit loss, buffer occupancy)
  - Study of arbitration scheme (compliance with available bandwidth)

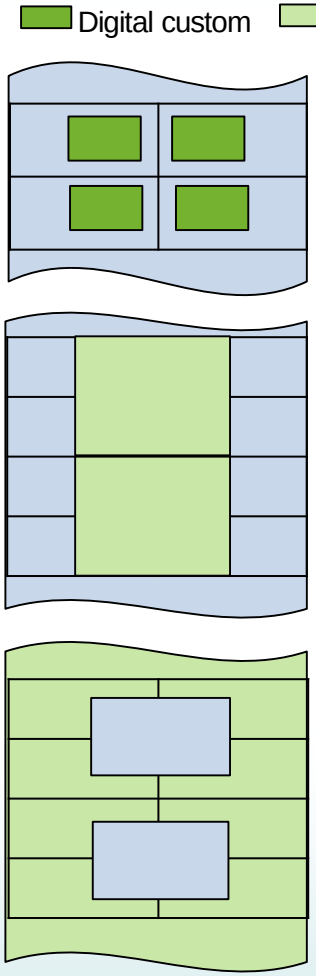
– Different kinds of input hit stimuli
  - Internally generated hits (various classes and parameters)
  - External Monte Carlo simulation data (ATLAS and CMS)



Top Level and Chip Integration WG

New modular approach proposed for design flow

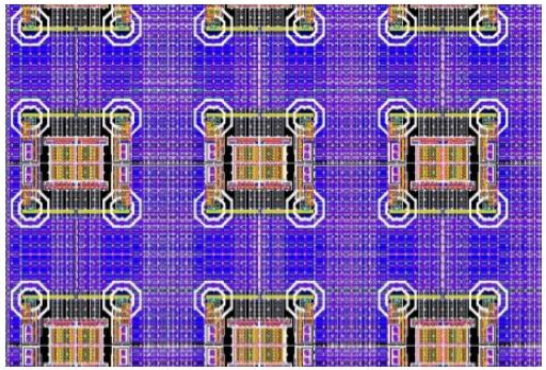
Floorplanning concept: "analog island" in "digital sea"



Traditional full custom design
- Make one pixel
- Step and reapeat identical copies
- Custom made digital
- Example: ATLAS FEI-3

More recently:
- Make few pixel regions
- Step and reapeat identical copies
- Synthesized digital
- Example: ATLAS FEI-4

New approach (RD53):
- Synthesized digital sea containing islands of analog pixels
- Example: FE65_P2



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FE65_P2 prototype chip *(Bonn-LBNL)*

[*T. Hemperek et al., TWEPP 2015*]

– 64x64 matrix, 50x50 μm^2 pixel

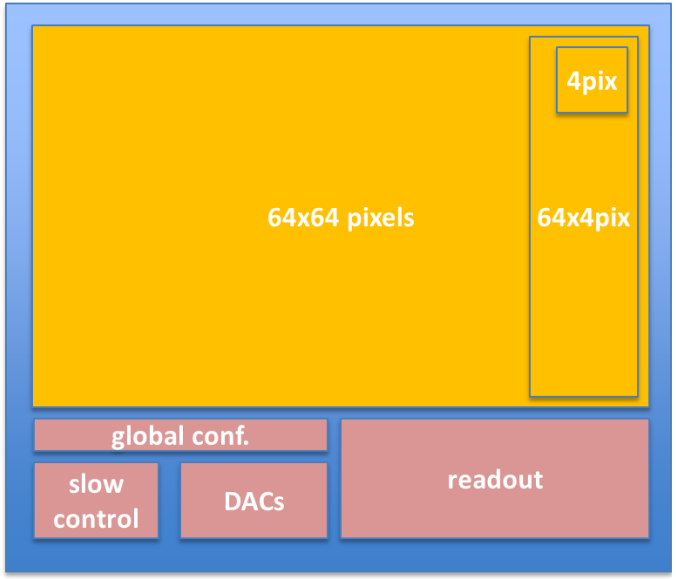
– Put into effect the following RD53 WG proposals:

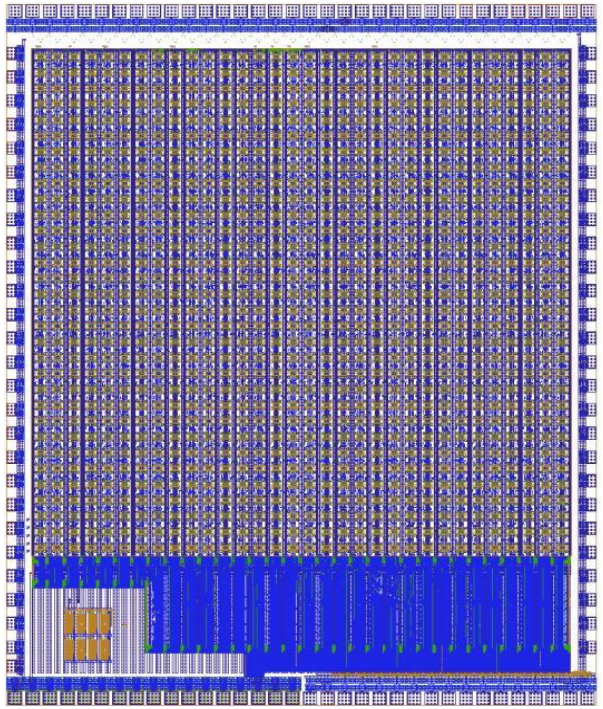
- *Top level* → digital on top hierarchical flow, modular approach (4x64 pixel cores), analog islands
- *Architecture* → distributed latency buffering architecture (2x2 pixel region optimized for higher hit rates)
- *Analog* → LBNL front end
- *Verification* → no VEPIX53; testing oriented verification with custom Python-based framework

Submitted: 12/2015

Started testing phase

- chip is functional and characterization is on-going
- in the process of being bump bonded to pixel sensors





CHIPIX65 Demonstrator *(CHIPIX65 Italian INFN collaboration)*

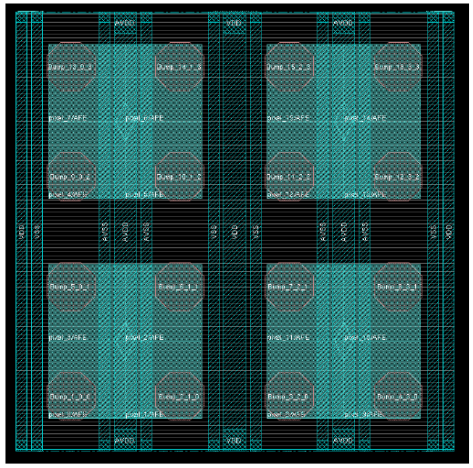
[*CHIPIX Collaboration, RD53 General Meeting (14/10/2015)*]

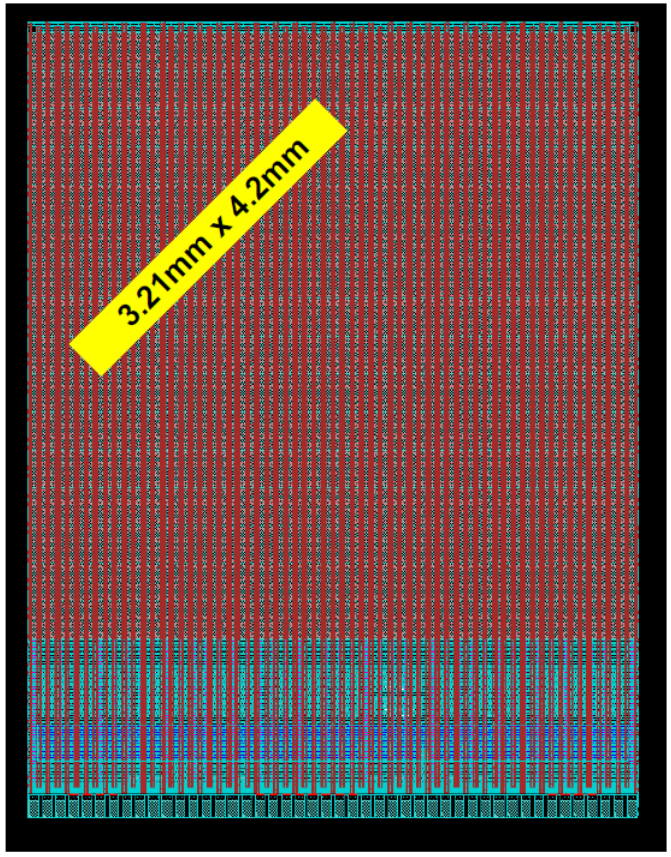
– 64x64 matrix, 50x50 μm^2 pixel

– Put into effect the following RD53 WG proposals:

- *Top level* → digital on top hierarchical flow, analog islands
- *Analog* → integration of 2 different flavours (Torino and Bergamo/Pavia front ends)
- *Architecture* → centralized latency buffering architecture (optimized) (4x4 pixel region)
- *Simulation and verification* using VEPIX53 framework
- *IP* → implementation of a set of tested RD53 IP blocks (bandgap, DAC, serializer…)

To be submitted:
03/2016 (Europractice MPW)





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Motivation

Radiation damage is severe in short and narrow channel. Most of the standard cells in digital libraries use minimum length transistor (L = 60 nm) and small width (W ~200 nm)

- What will effective performance degradation be of *digital circuits* at +100 Mrad?
- Will special/modified libraries be needed for high rad and/or high speed?
- High density digital is critical for high hit rates and long trigger latency

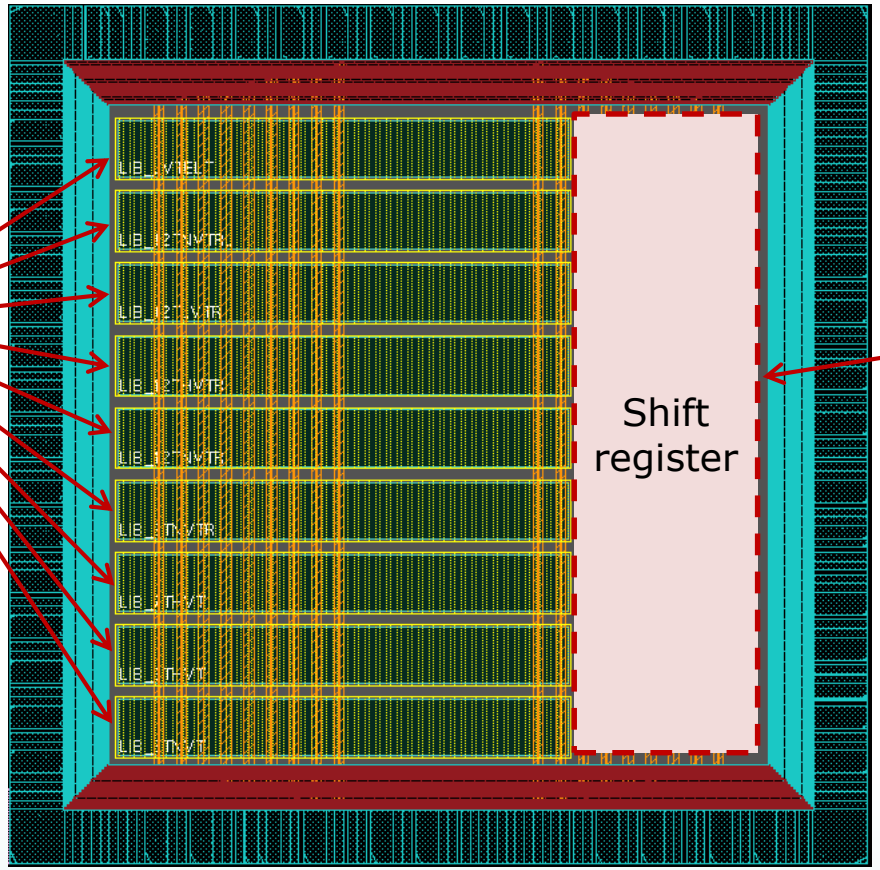
DRAD: joint effort between RD53, MPA and LP-GBT

What to test: speed degradation and power consumption of a subset of the digital library from the foundry and of modified libraries with larger transistor (which should reduce performance degradation)

To be submitted: 03/2016 (Europractice mini@sic)

DRAD layout

9 libraries: Different V_T flavours, transistor size and shape



For SEU testing

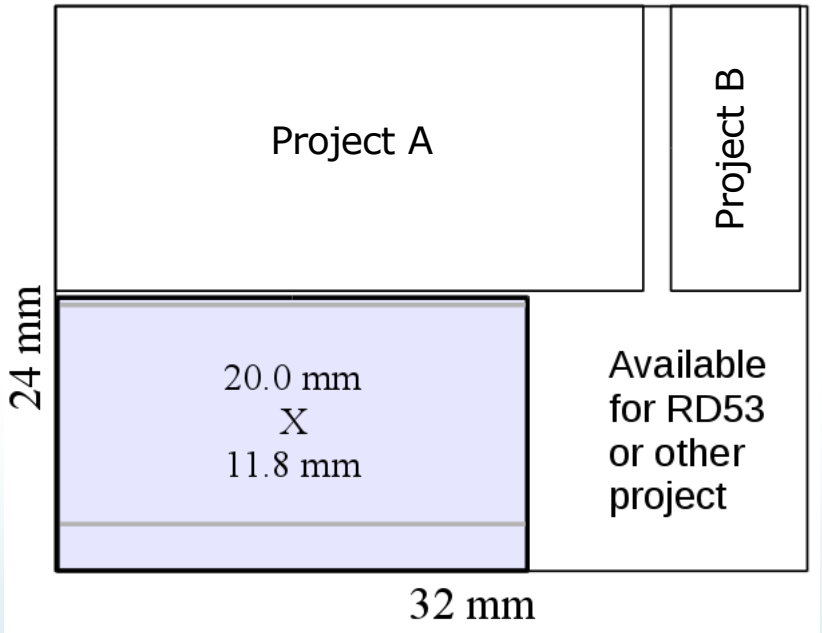
RD53A: full scale demonstrator chip

– Proposed 20x11.8 mm^2 chip (→ 400x192 pixels), 2500 μm^2 pixel

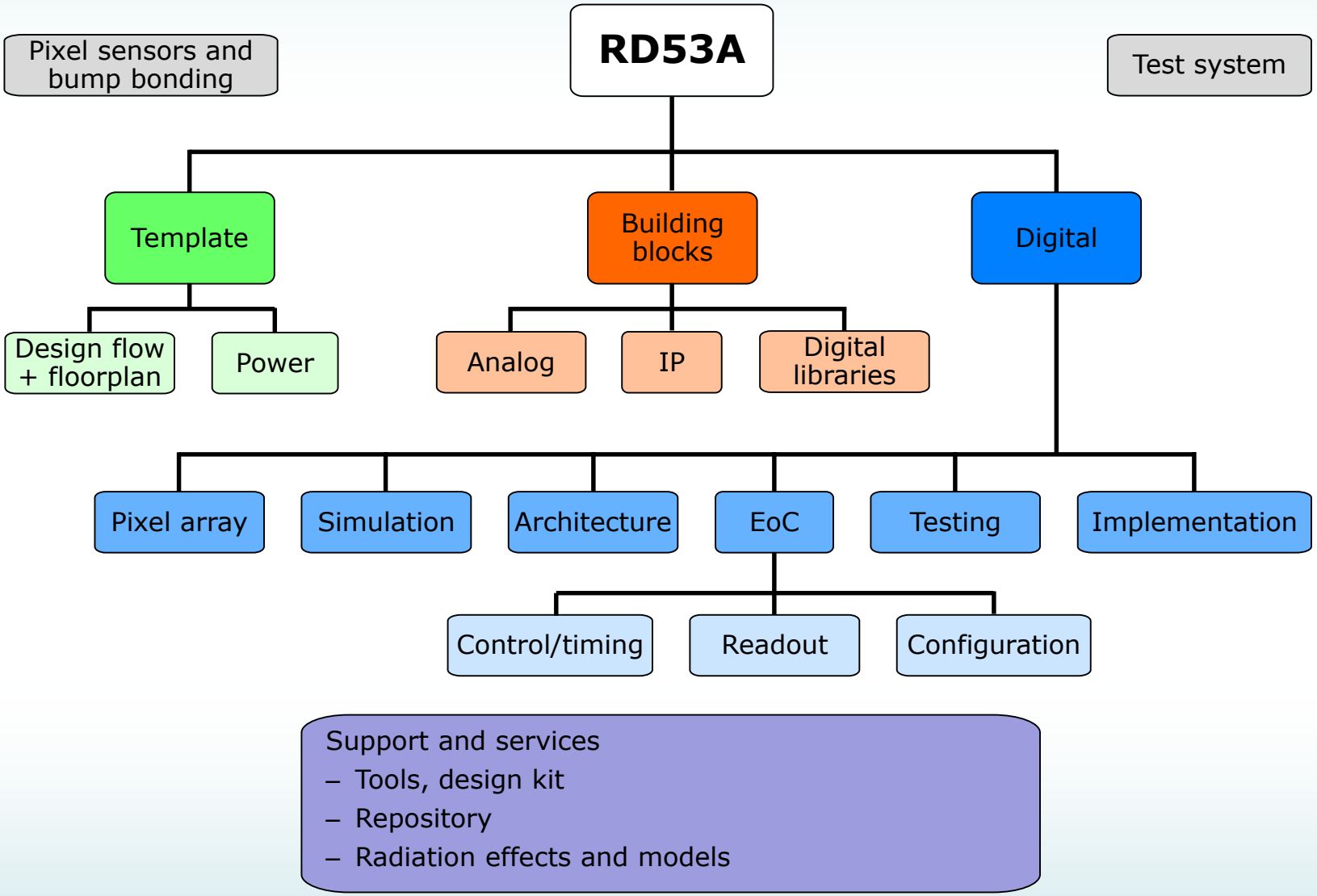
– *Goal*: demonstrate in a large format IC
- suitability of 65nm technology (including radiation tolerance)
- high data/trigger rate, low threshold operation, high speed readout
- power management, serial powering
- put into effect RD53 WG proposals

– Not intended to be a production chip
- will contain design variations for testing purposes
- wafer scale production will enable prototyping of bump bonding assembly with realistic sensors in new technology
  → performance measurement

To be submitted: end 2016
(prospected shared engineering run with other projects)



Project organization



Planning

3 main general project deliverables

- ***V0 (Q1 2016)***: upscaled FE65_P2
  - improved design flow, normal standard cell libs, no IPs, single front end
  - shared repository
- ***V1 (Q2-Q3 2016)***: near final architecture
  - script-based design, multiple front ends, IPs for biasing and monitoring, near final RTL, TMR, radiation hard digital library
  - functional verification, analog verification, timing verification, metal filling with verification
- ***V1.5 (Q4 2016)***: final architecture
  - final RTL
  - final implementation
  - extensive functional and design verification

Each project work package having its specific sub-deliverables

Design flow and floorplan

Compromise: digital in analog template

– Pixel array
- front end quad islands with bump pads
- power-bias distribution with shielding
- triple well isolation

– EoC, power, wire bond pads

Digital must fit in defined digital regions, with some specific constraints (e.g. quiet logic on boundary to analog quads)
- different choices that can be made for modular approach (flattening to pixel/region/(multi)column level)

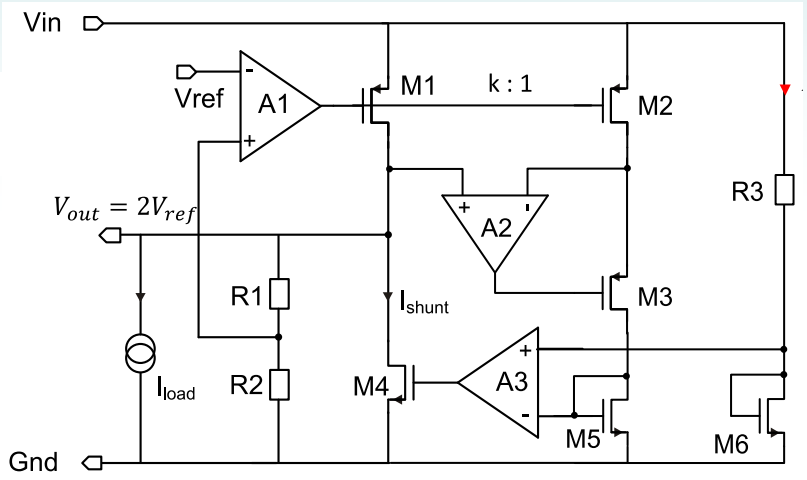
Analog and IPs

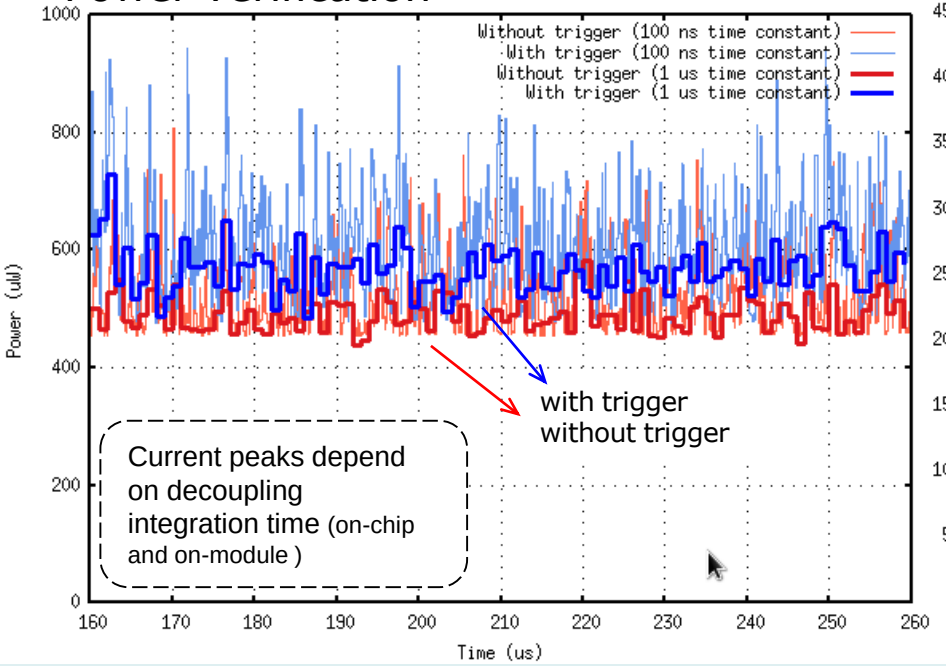
– Organize blocks on common RD53A repository
– Define standard set of design files and information to be provided with each block

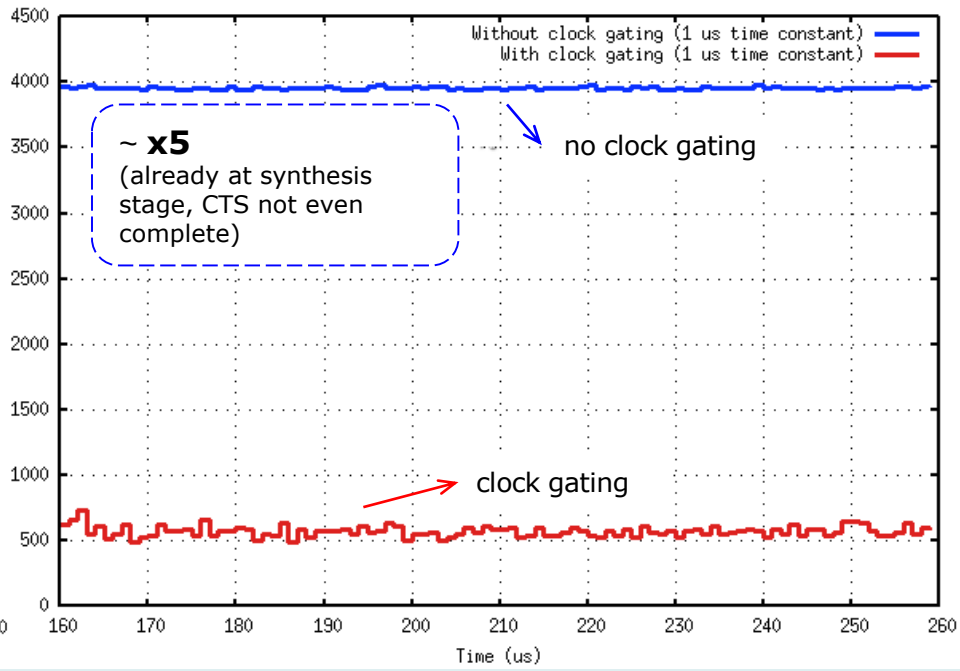
Q1 2016: first version, check functionality and radiation tolerance
Q2 2016: final versions, ready for integration

Power

- Shunt-LDO integration
- On-chip power distribution
- Optimization for serial powering
  - implications of different low power techniques are being studied
- System level power aspects
  - Minimize power consumption
  - Minimize power/current peaks that are particular problematic for serial powering
- Power verification





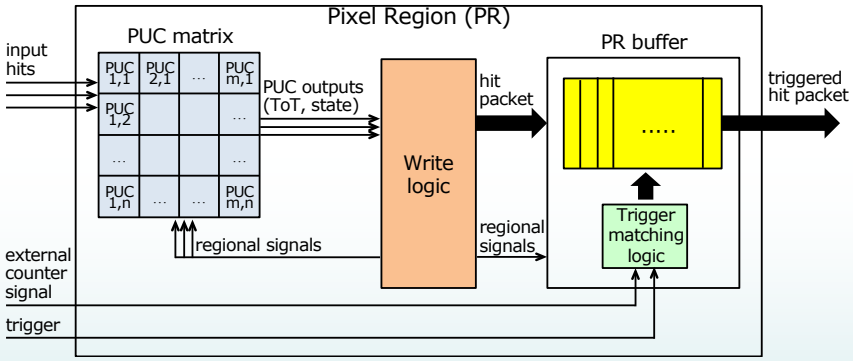


Simulation and architecture

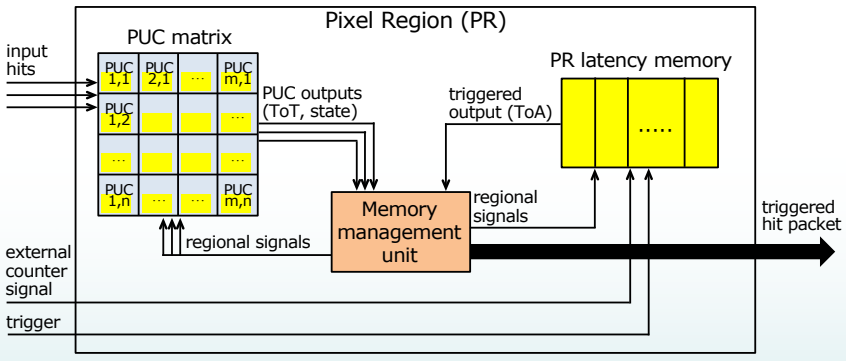
Q1 2016: decision on digital architecture

- highlight pros and cons of different existing architectures quickly (centralized vs distributed as implemented on small scale prototypes)
  - simulation of non-synthesized RTL on VEPIX framework → inefficiency (same simulation parameters, Monte Carlo physics data)
  - comparison of synthesized architectures → area, power, sensitivity to SEU
- converge to a single architecture (choose one, merge the two… based on comparison results)
- use this architecture as starting point for further optimization

Q2-4 2016: focus on extensive verification (adding SEU injection)



centralized architecture

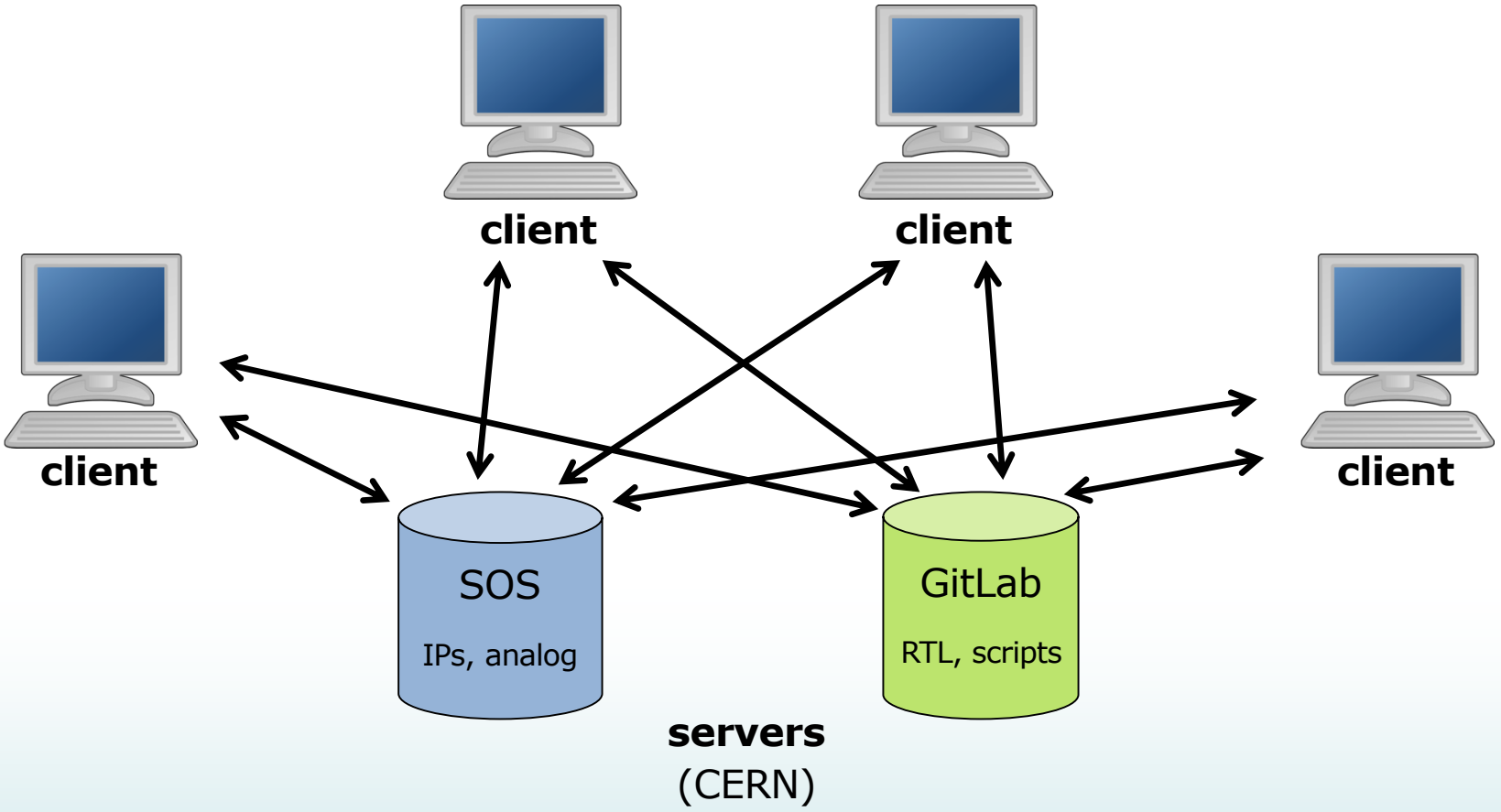


distributed architecture

Common RD53A repository

– ClioSoft SOS repository for analog and IP blocks

– GitLab repository for digital design data



RD53 is addressing the phase 2 upgrade design challenges

Working group progress

- Radiation goal moved to 500 Mrad; recommendations to improve radiation tolerance
- Analog blocks and IPs prototyped and characterized
- Input and output protocols proposed
- Simulation and verification framework developed
- New approach on chip design proposed based on digital on top

➔ Further investigation on radiation being prepared with collaboration on design of DRAD test chip

➔ Small scale prototypes to be tested, putting into effect part of working group results

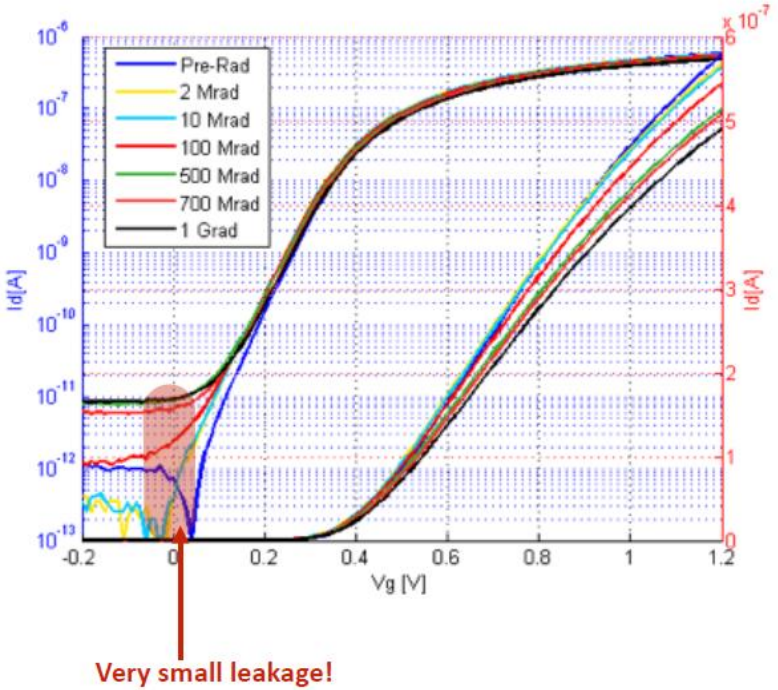
➔ Design of full scale demonstrator has started

BACKUP

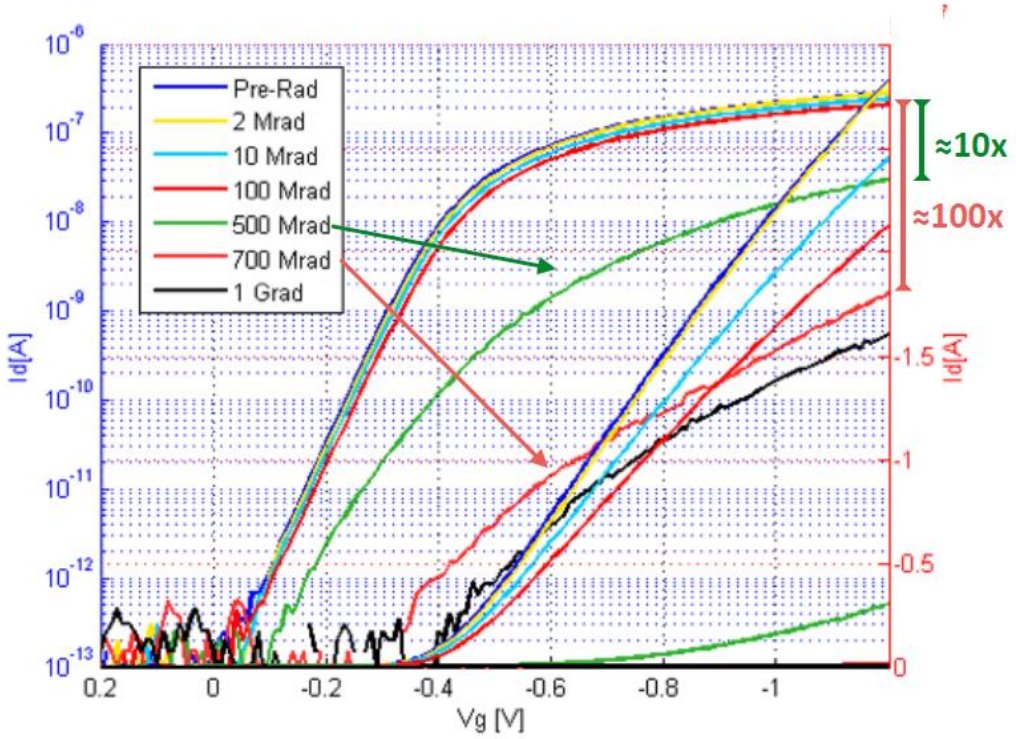
Radiation WG (I)

– Narrow channel PMOS transistors do not work above 500Mrad, while NMOS are working without large damage up to 1Grad

NMOS



PMOS

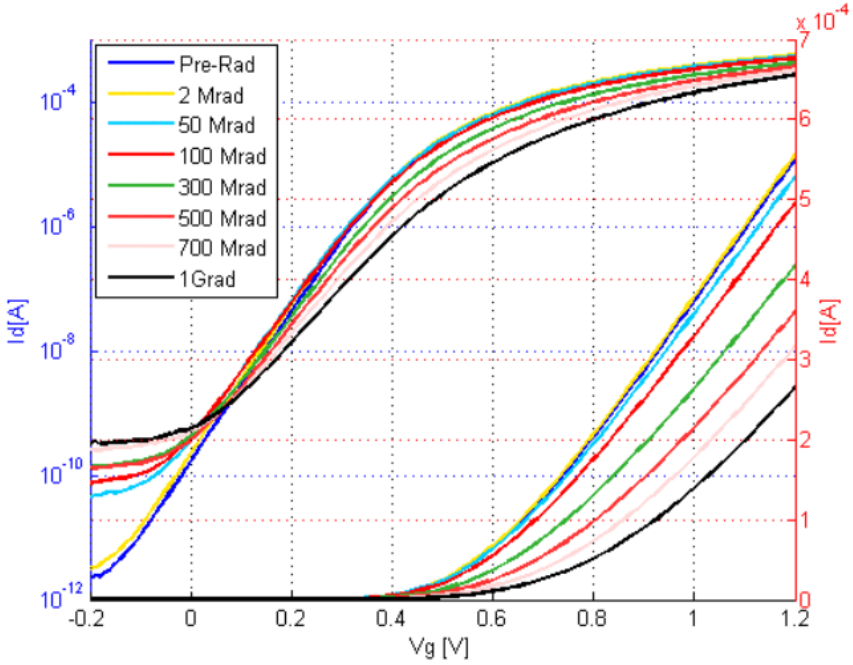


Transistors' size: W=120nm, L=1um
Irradiation conditions:
T = 25C
Bias: |Vgs|=|Vds|=1.2V

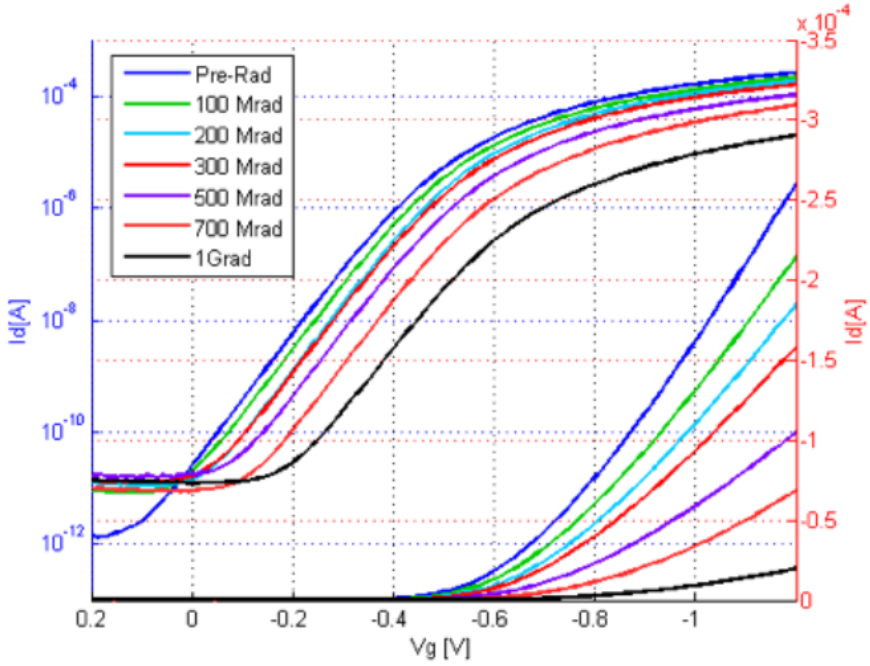
Radiation WG (II)

– Short channel PMOS are more damaged than NMOS

NMOS



PMOS

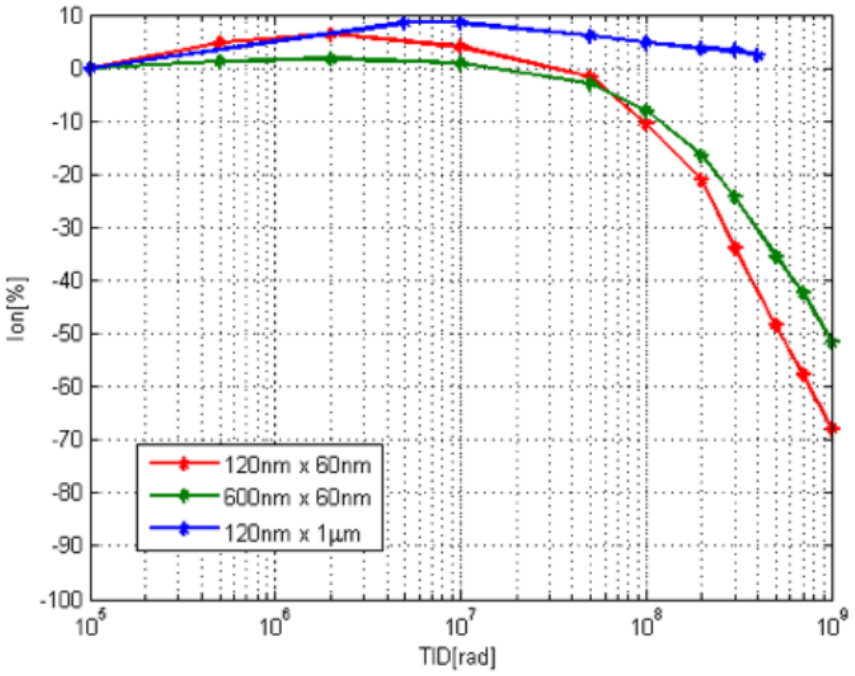


Transistors' size: W=1um, L=60nm
Irradiation conditions:
T = 25C
Bias: |Vgs|=|Vds|=1.2V

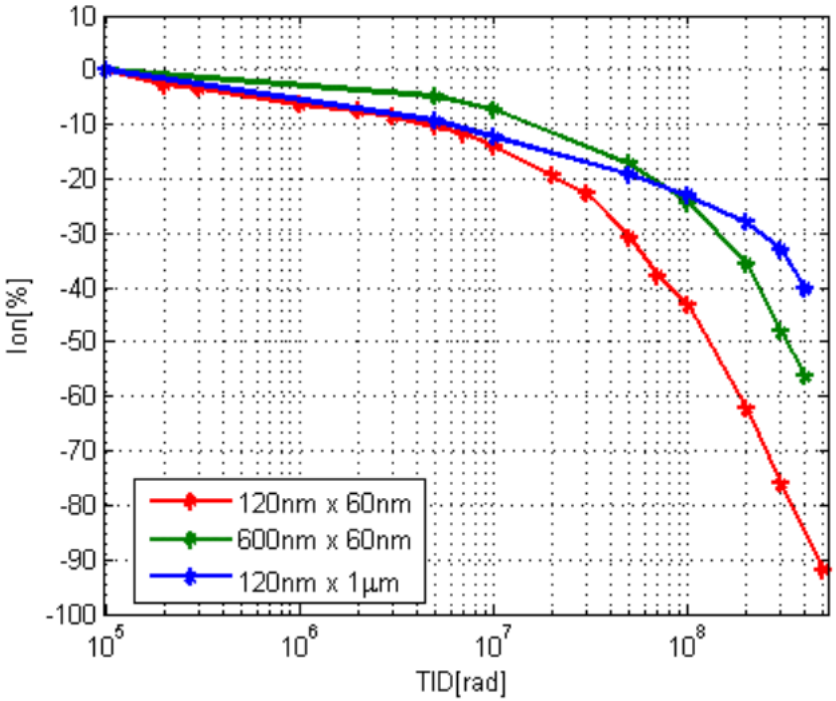
Radiation WG (III)

– Short AND Narrow transistors are simultaneously affected by Radiation-Induced Short Channel Effect (*RISCE*) and Radiation-Induced Narrow Channel Effect (*RINCE*), hence their degradation is the worst measured

NMOS



PMOS



Irradiation conditions:
* T = 25C

* Bias NMOS:
"Diode" => |Vgs|=|Vds|=1.2V

* Bias PMOS:
"Gnd" =>|Vgs|=Vds=0V