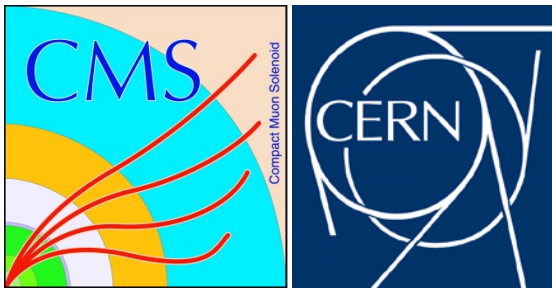
The Electronics for the Upgrade of the CMS Outer Tracker

ACES Workshop

9 March 2016

Francois Vasey

Many thanks to CMS Tracker collaborators,
too numerous to be acknowledged individually

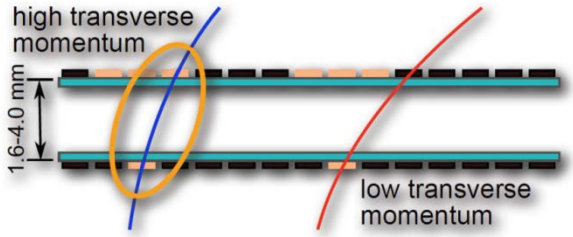


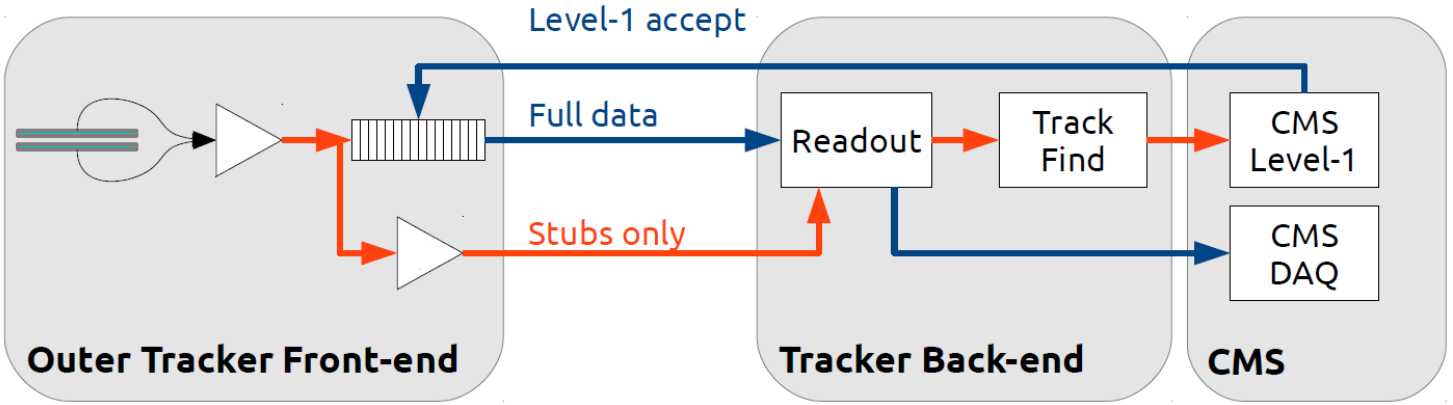
CMS Outer Tracker is part of the L1 Trigger Chain

Modules generate track stubs at BX frequency

Level-1 "stubs" are processed in the back-end

Form Level-1 tracks, pT above ~ 2 GeV, contributing to CMS Level-1 trigger





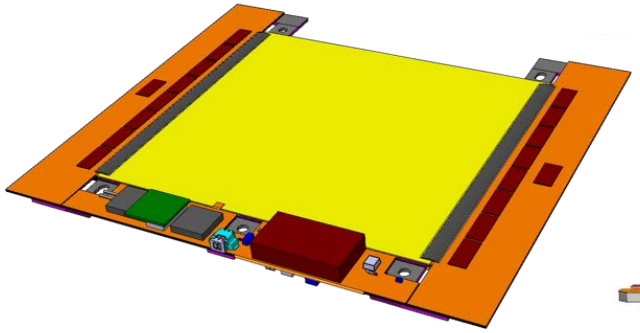
@ 40 MHz – Bunch crossing →Trigger Data

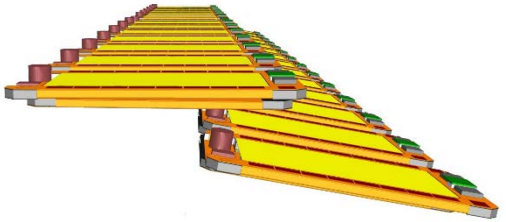
@ <750 kHz – CMS Level-1 trigger →L1 Readout Data

Pt Modules are the Tiles of the Outer Tracker

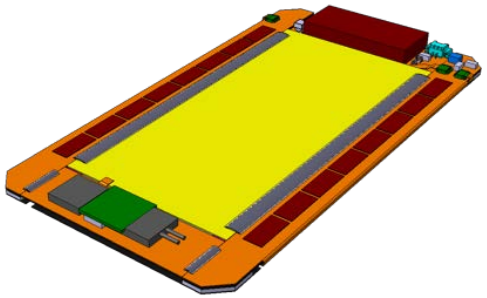
Each Module is an independent unit with its own services

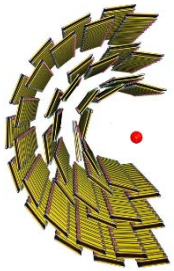
2 Strip sensors
Strips: 5 cm × 90 µm
Strips: 5 cm × 90 µm
P ~ 4W
~ 92 cm^2 active area
For r > 40 cm

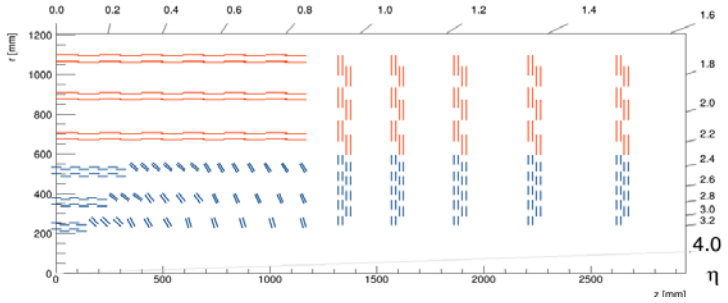




Pixel + Strip sensors
Strips: 2.5 cm × 100 µm
Pixels: 1.5 mm × 100 µm
P ~ 6-8W
~ 44 cm^2 active area
For r > 20 cm



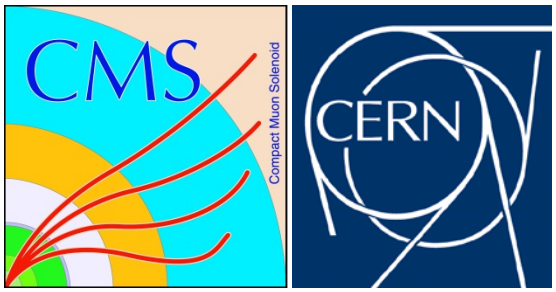




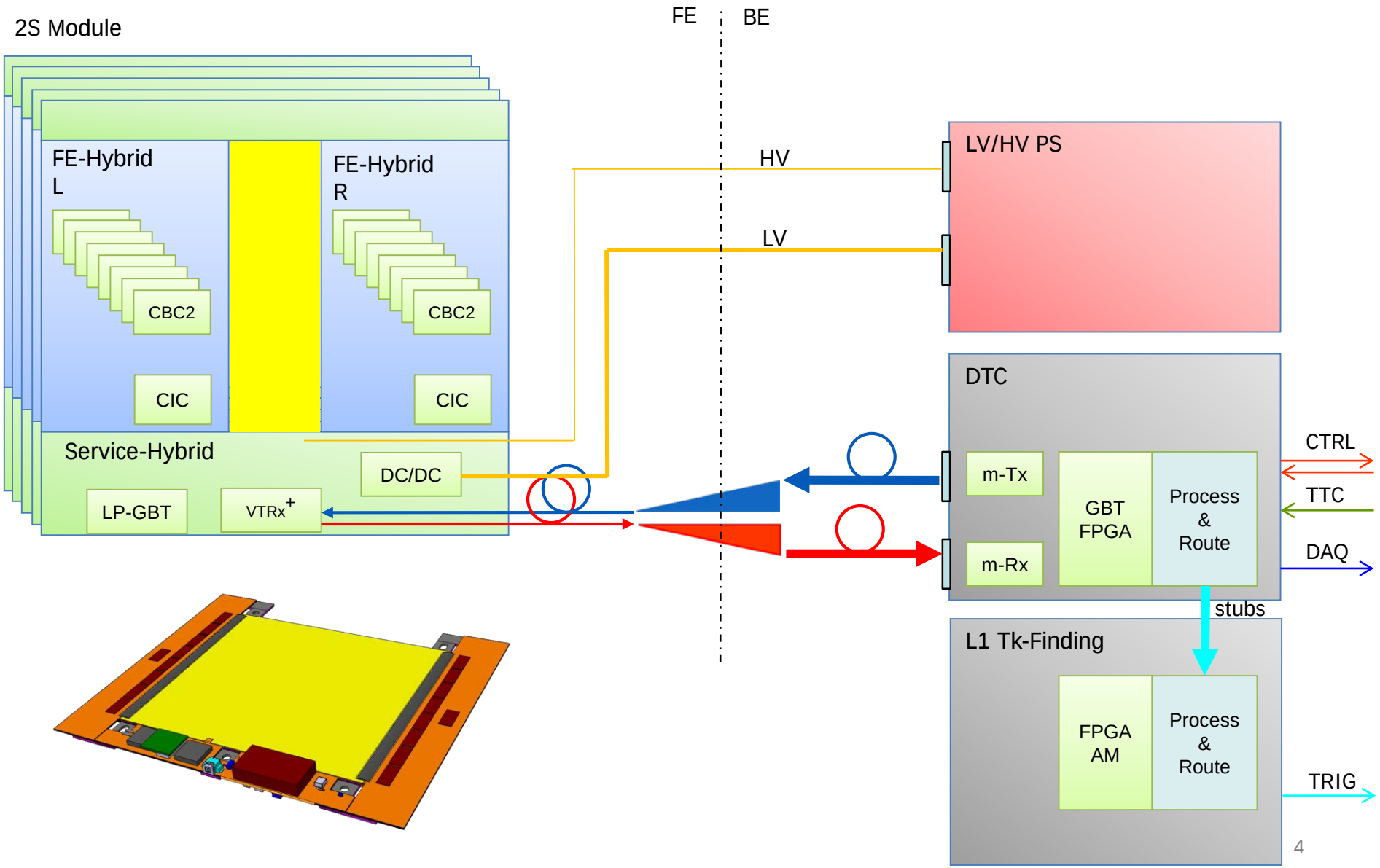
The Electronics for the Upgrade of the CMS Outer Tracker

Outline

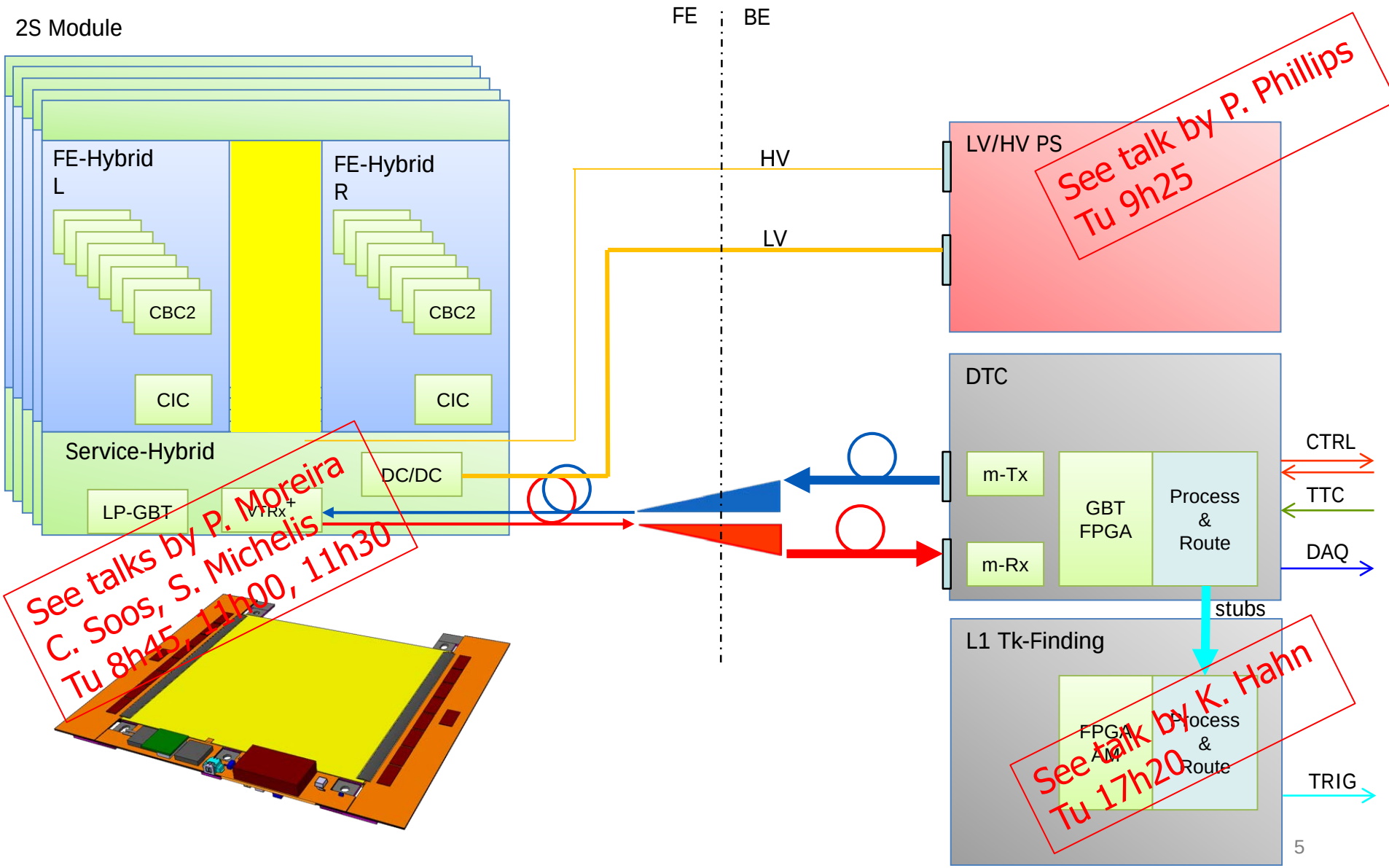
1. System Architecture
2. Front-End
3. Back-End
4. System Tests
5. Conclusions



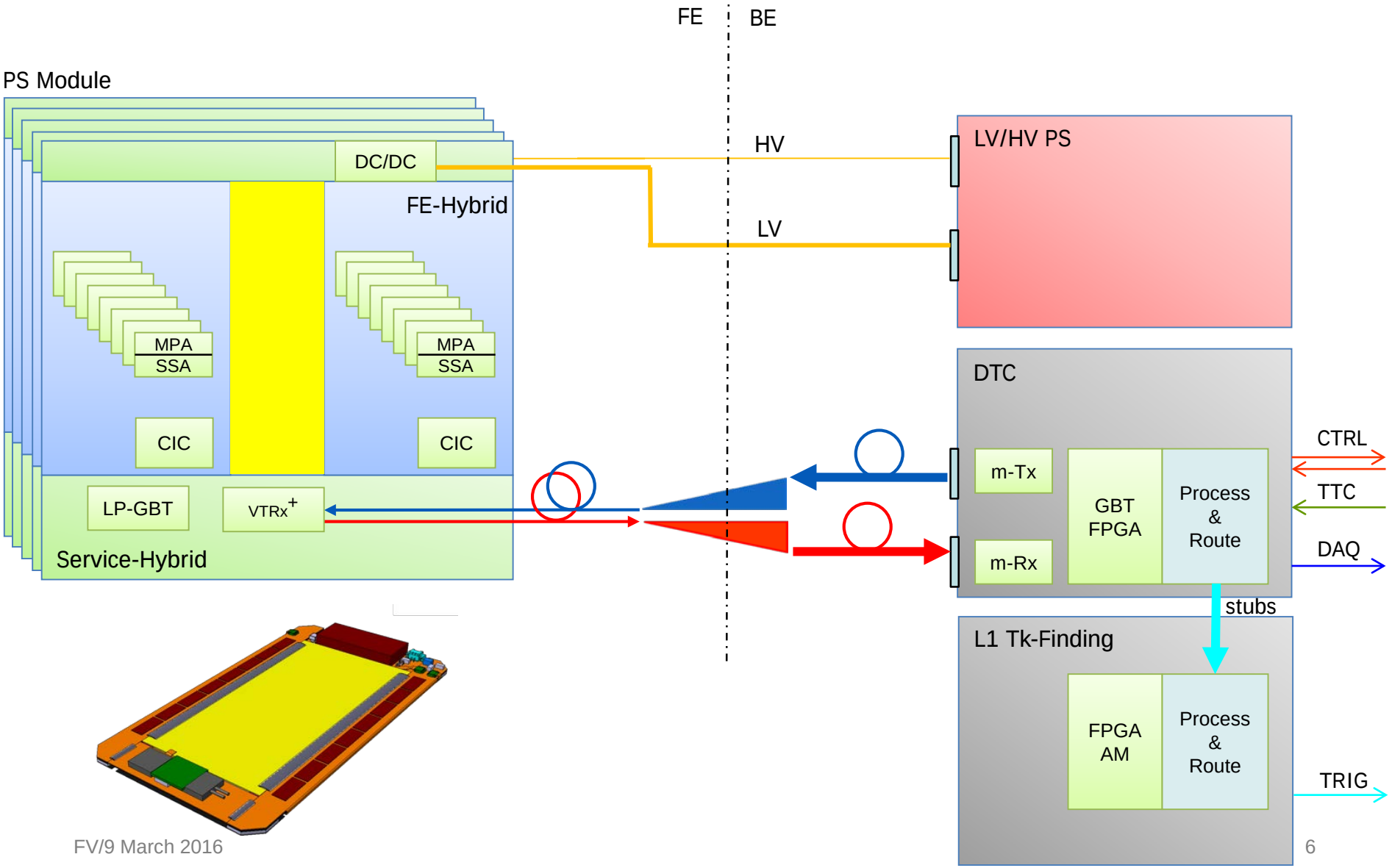
1. Electrical System Architecture: 2S



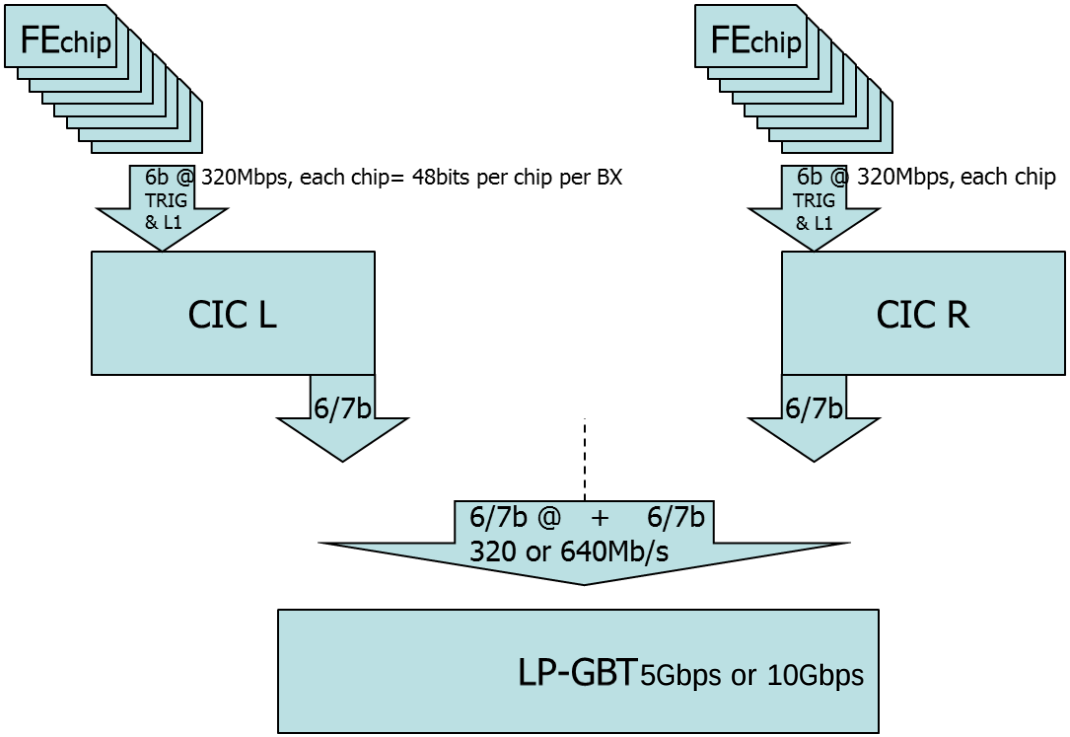
1. Electrical System Architecture: 2S

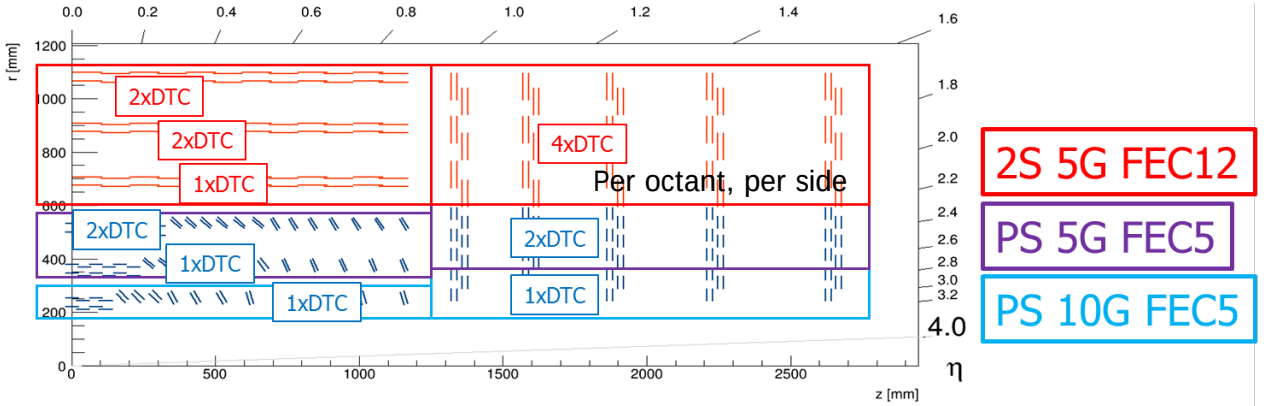


Electrical System Architecture: PS

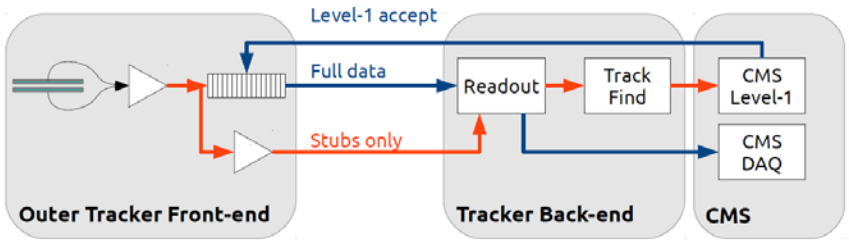


Data Aggregation Chain





Upstream Data Path from Concentrator (CIC)



@ 40 MHz – Bunch crossing →Trigger Data
@ <750 kHz – CMS Level-1 trigger →L1 Readout Data

L1

Trig

1b

5b

2S:Unsparsified
PS: Sparsified

CIC

1b
L1RO

5/6b
Stub

Sparsified
Readout frame
from 8 FE chips

Block synchronous transfer of trigger data:

- Capacity shared over 8BX
- Synchronicity is maintained
- Latency is fixed

200ns = 8BX block length

Shared and capped bandwidth

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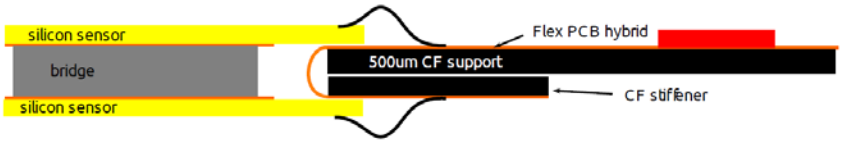
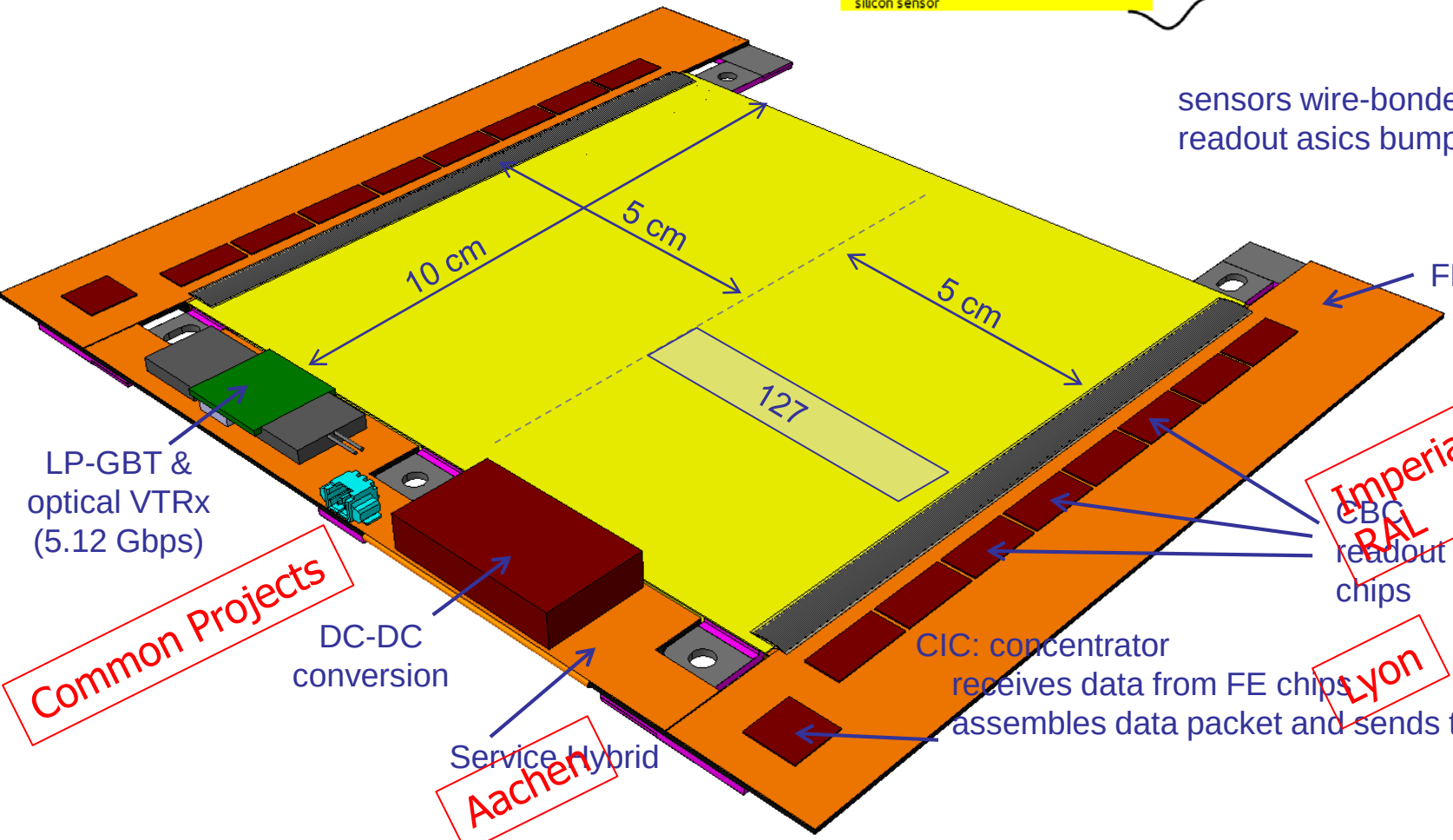
2S module





sensors wire-bonded
readout asics bump-bonded

CERN

FE Hybrid

Imperial College
RAL

CBC readout chips

LP-GBT & optical VTRx (5.12 Gbps)

Common Projects

DC-DC conversion

CIC: concentrator
receives data from FE chips
assembles data packet and sends to LP-GBT

Lyon

Service Hybrid

Aachen

1 module type, ~10 x 10 cm^2 active sensor area for whole of region beyond r = 50 cm (endcaps too)
self-contained single, testable object; only needs power and optical connection to function

2S => 2 silicon sensors, each read out at both ends, strips 5 cm x 90 μm pitch, ~4000 channels total

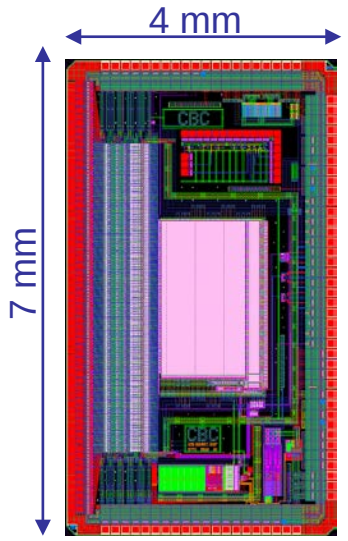
16 bump-bonded CBC readout asics, each reads 127 strips from top layer, 127 from bottom

1. CBC Readout Chip

2 versions have been produced - both in 130nm CMOS

CBC1 (2011)

128 wire-bond pads, 50 μm pitch
front end designed for short strips, up to 5 cm
DC coupled, up to 1μA leakage tolerant, both sensor polarities
binary unsparsified readout
pipeline length 6.4 μsec
no triggering features

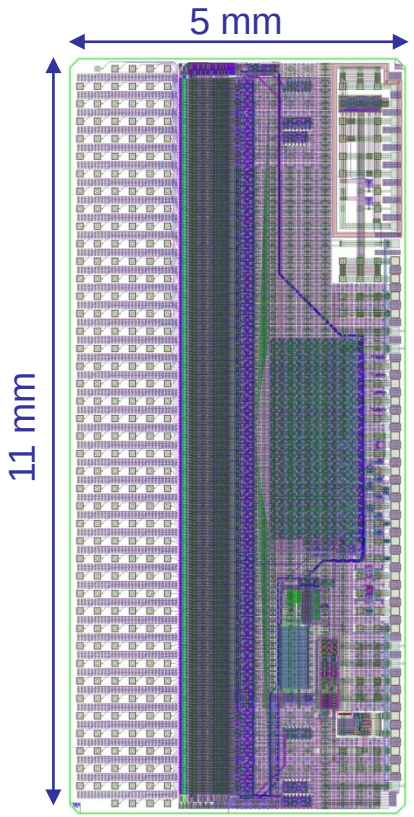


CBC1

CBC2 (January, 2013)

M. Raymond
ACES 2014

254 channels, 90 μm pitch
~same front end, pipeline, readout approach as CBC1
Rudimentary correlation and triggering features
plus
bump-bond layout
- C4 bump-bond layout, 250 μm pitch, 19 columns x 43 rows
includes triggering features
- 30 interchip signals (15 in, 15 out), top and bottom

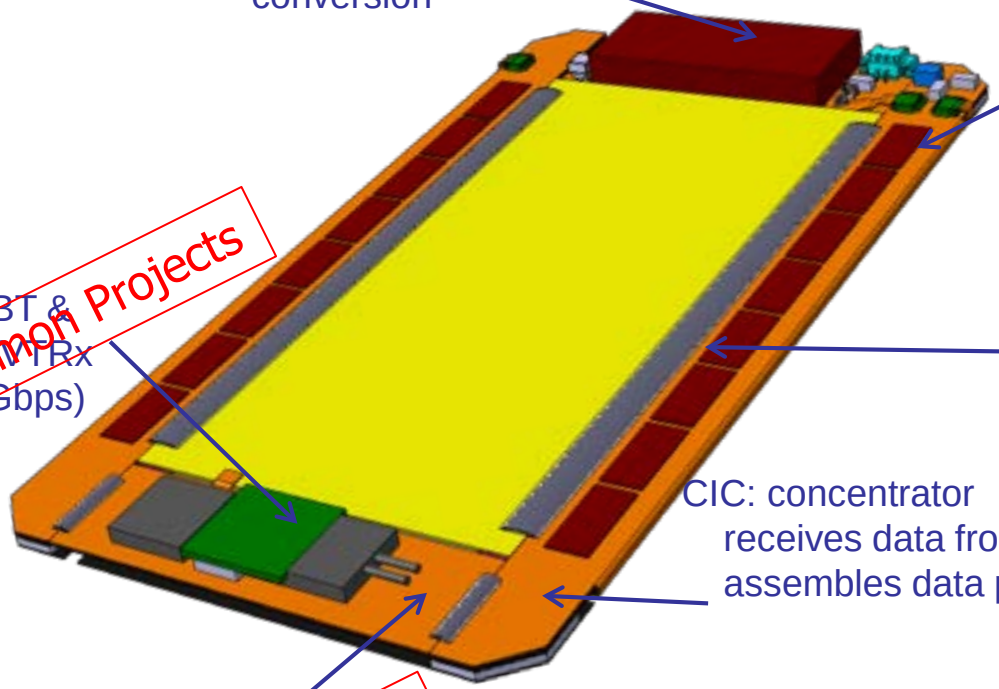


CBC2

CBC3 (in design, submission expected summer 2016)

254 channels
front end optimized for 5cm strips (up to 8cm), n-polarity
Pipeline length 12.8 μsec, based on enclosed layout cell
plus
Full correlation logic, 320Mbps digital interconnects

PS Module



DC-DC conversion

FE Hybrid

CERN

LP-GBT & optical MTRx (5.12 Gbps)

Common Projects

SSA/MPA readout chips

CERN

CIC: concentrator
receives data from FE chips
assembles data packet and sends to LP-GBT

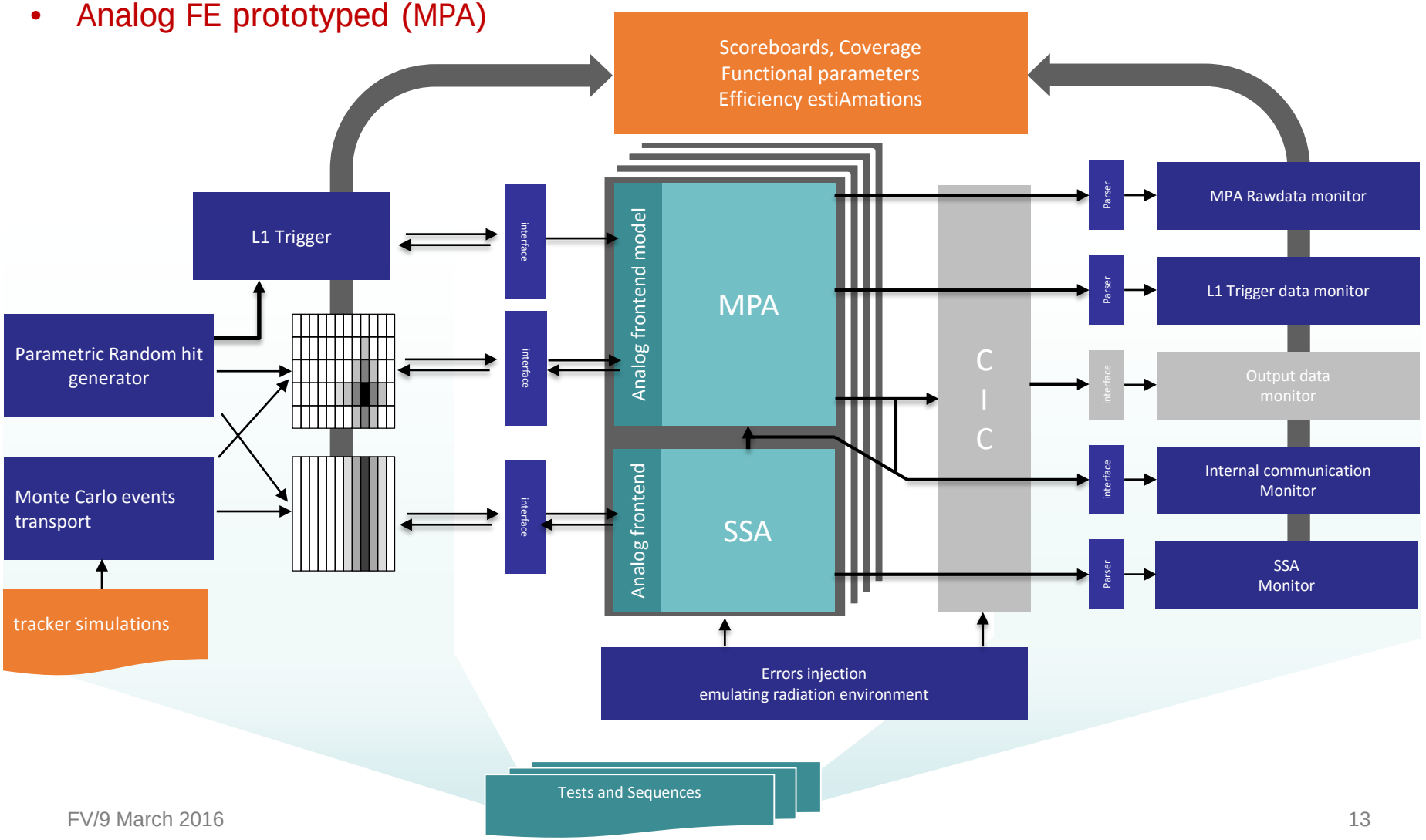
Lyon

Service Hybrid

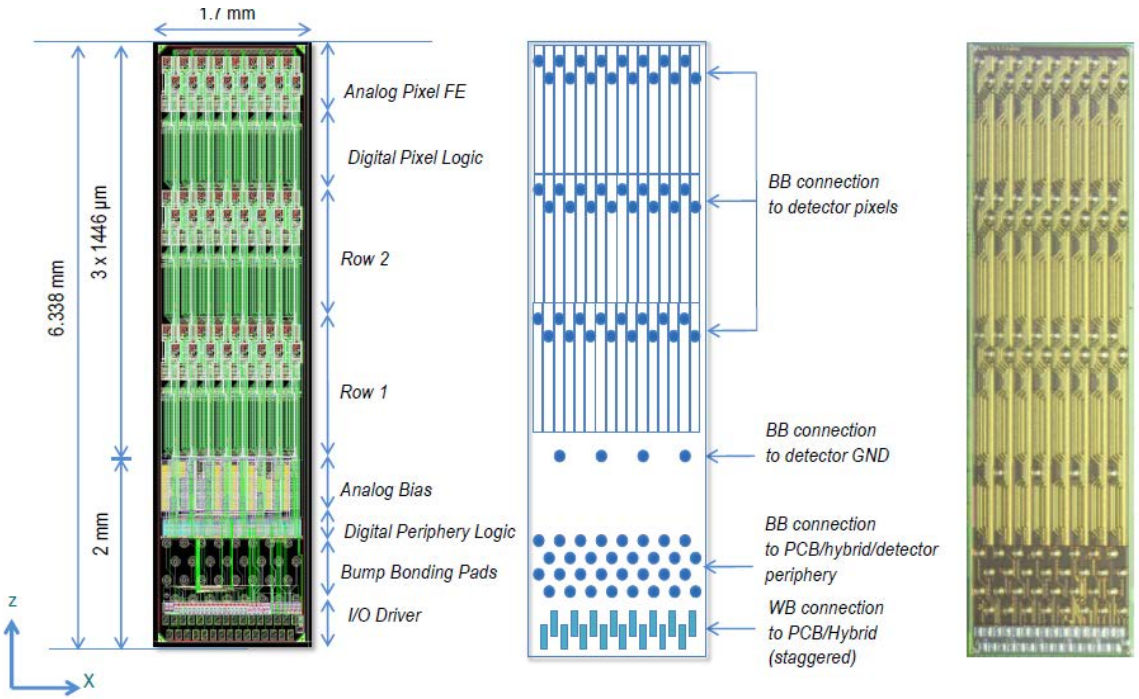
Aachen

2. SSA, MPA and CIC Simulation Framework

- 65nm CMOS
- ASICs are in design stage
- Digital system level modelling on-going
- Analog FE prototyped (MPA)



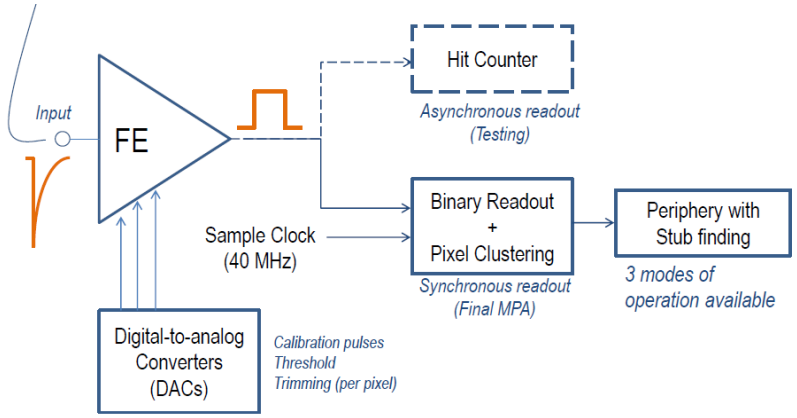
MPA-Light Mini-ASIC



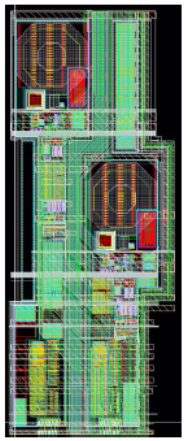
prototype version produced – 65nm CMOS

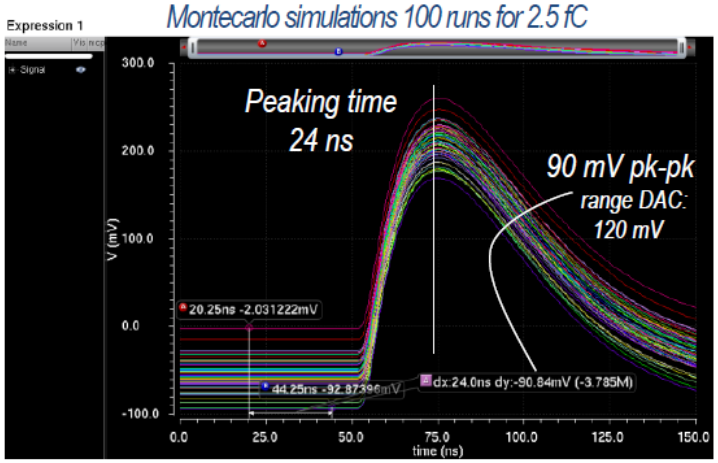
2015

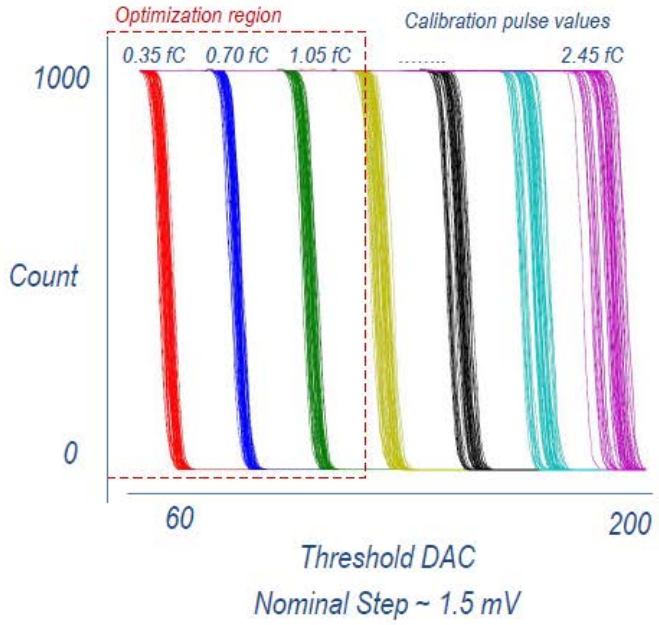
- 3x16 pixels (instead of 16x120)
- Analog pixel cell identical to final MPA one
- Rudimentary digital logic
- Possibility to daisy chain chips
- Possibility to emulate strip



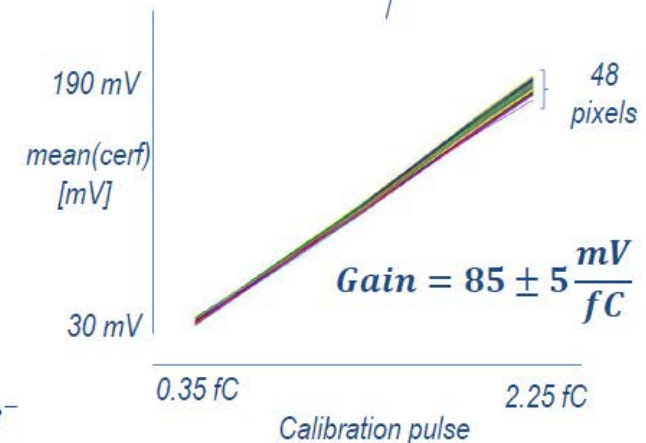
MPA-Light Test Results







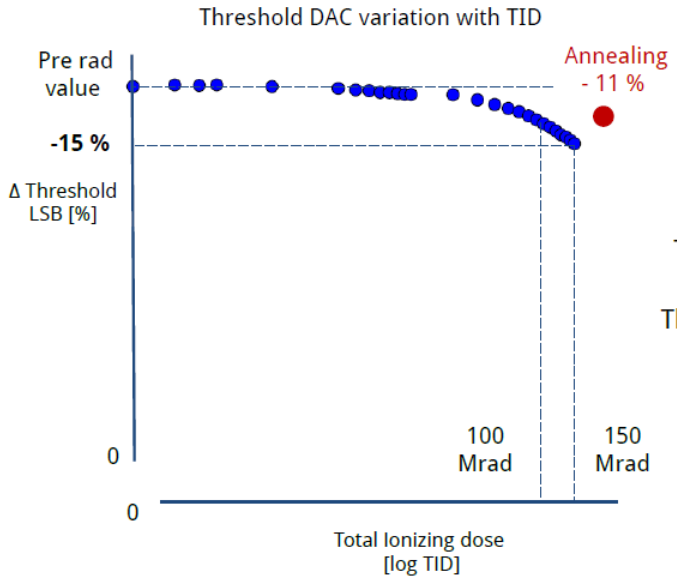
For every pixel, the gain is extracted with the complementary error function fitting



sigma(cerf) = Eq. Noise Charge = $276\, e^- \pm 27 e^-$

MPA-Light Radiation Test Results (1/2)

Analog FE characterization

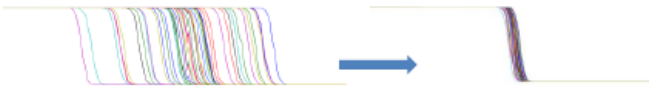


The largest variation due to TID is observed on the threshold DAC.

The variation **can be compensated** thanks to the DAC range

Drift of discriminator offset

- Need of re-trimming after irradiation



Calibration DAC step variation is < 10 %

Analog power consumption decreased

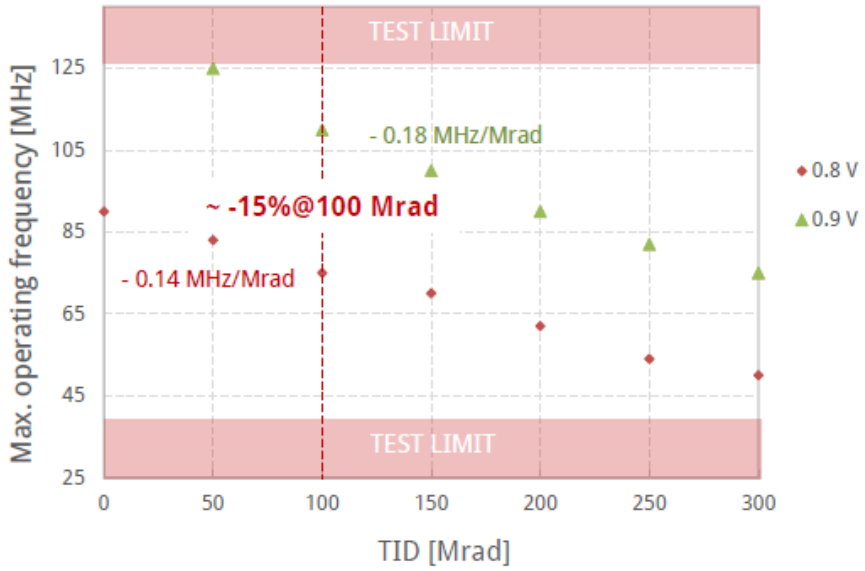
- - 7 % after 150 Mrad
- - 4 % after Annealing
- Digital power consumptions variation is negligible

Digital Pass/Fail checks do not show any fail at nominal condition (1.2 V, 40 MHz)

MPA-Light Radiation Test Results (2/2)

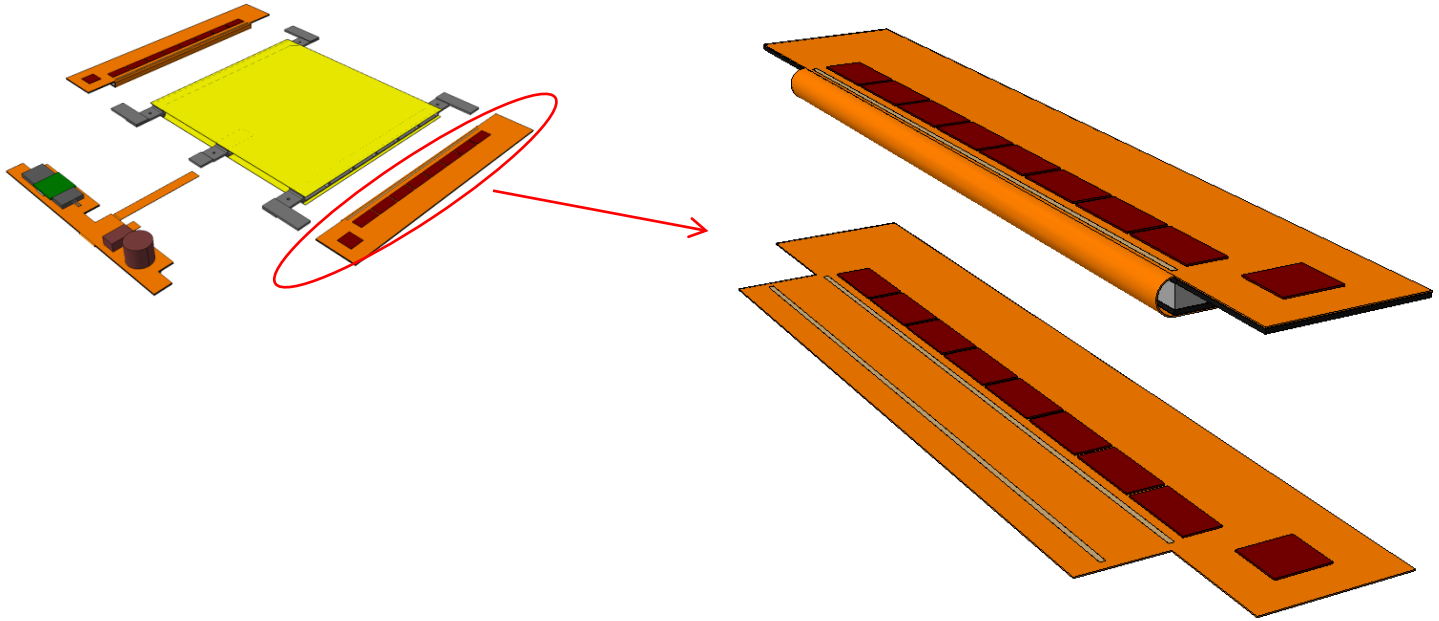
Digital characterization

We observe a **linear degradation** of the frequency between 0 and 300 Mrad

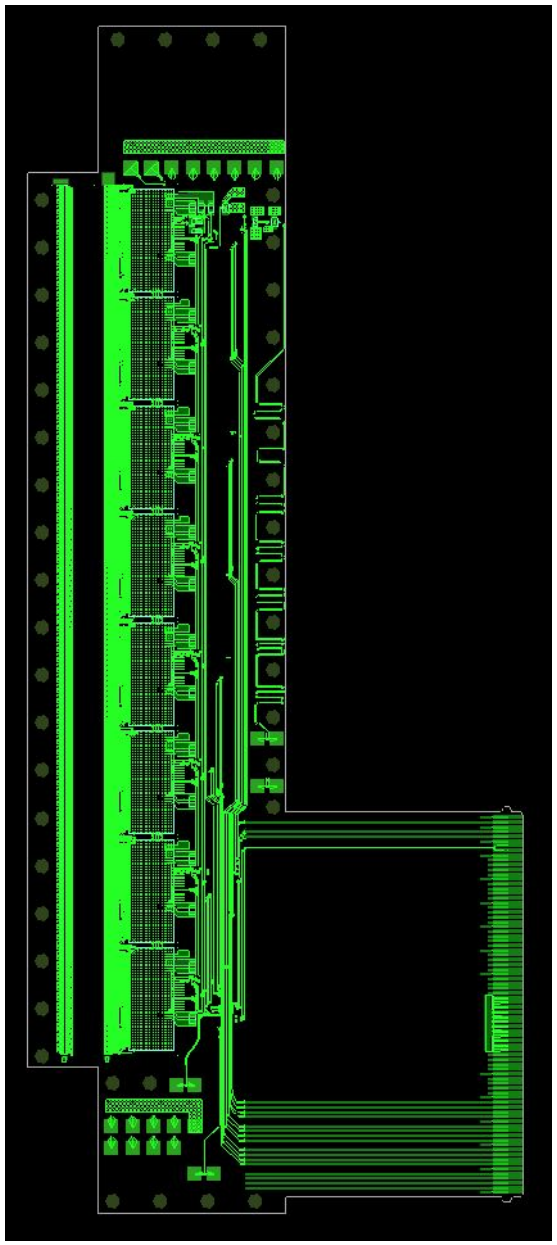


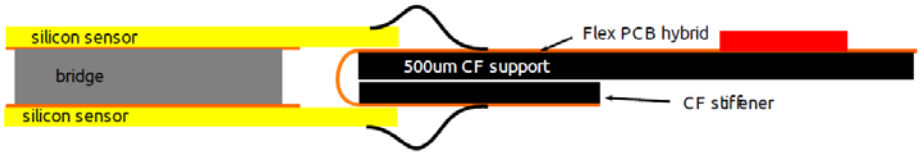
The effect is related with **short channel** in the periphery logic.
This is the dominant effect in standard cell logic.

3. Front-End Hybrid (FEH) Developments



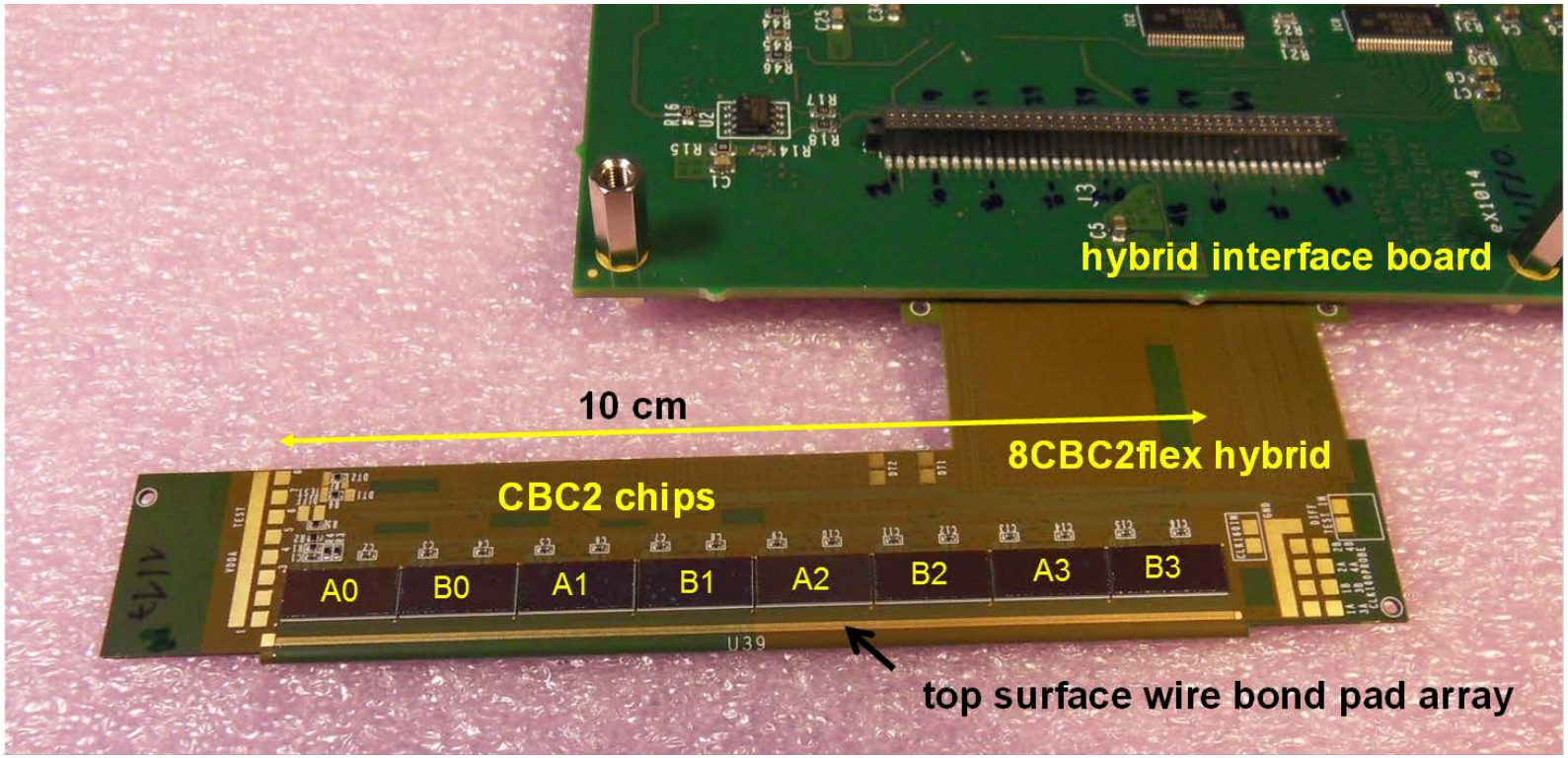
2S FEH (1/2)



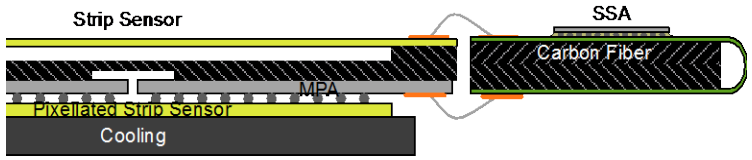


- **The 8CBC2Flex is a full 8 CBC2 readout system.**
  - 4 layer, 150µm thick
  - One 40 MHz clock input.
  - All chips configured separately through a common I2C bus.
  - All chips are powered at 1.25V.
- **Common back end signals to control the readout:**
  - Reset, Clock 40, I2C bus.
- **Paired control signals:**
  - Fast reset, I2C refresh, T1Trig, Test Pulse.
- **All readout signals are handled per chip:**
  - Trigger and Data lines.
- **All signals are brought to a FPC connector.**
  - No concentrator

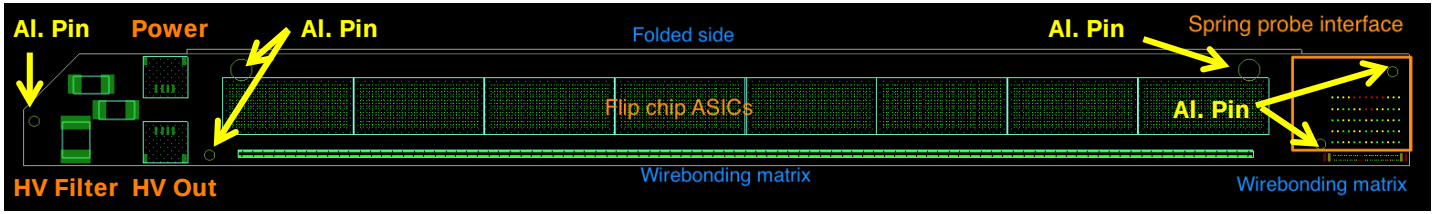
2S FEH (2/2)


hybrid interface board
10 cm
8CBC2flex hybrid
CBC2 chips
A0
B0
A1
B1
A2
B2
A3
B3
top surface wire bond pad array

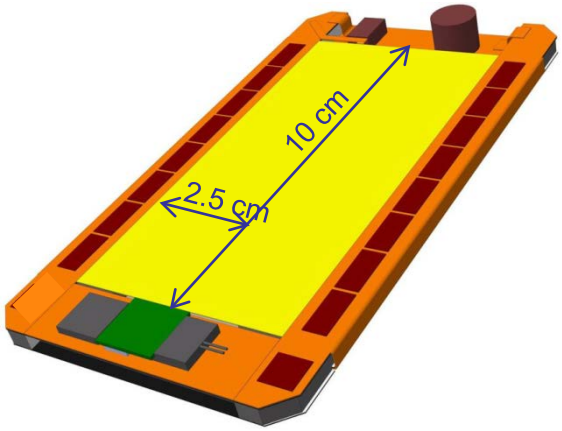
PS FEH Mockup

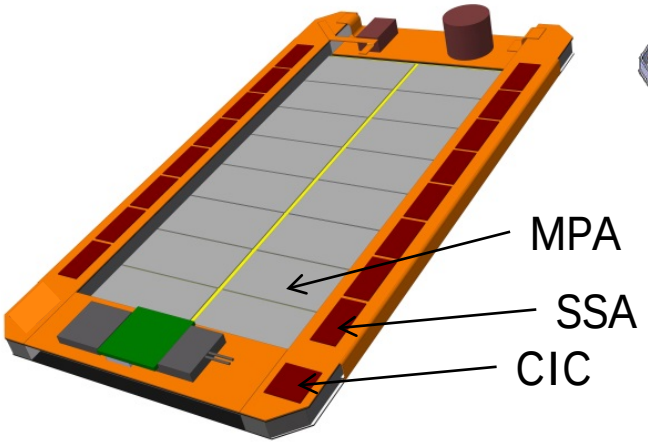


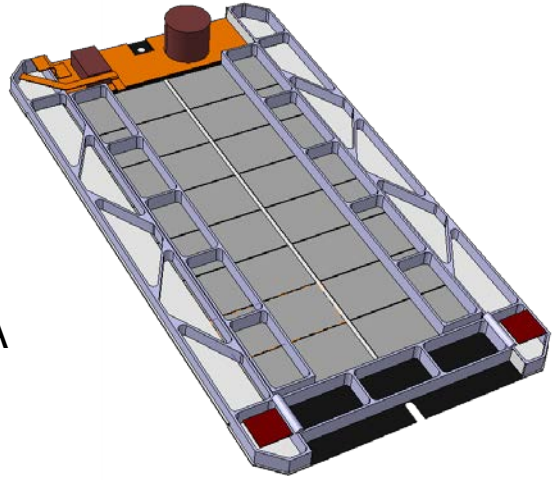
- **A baseline circuit has been drafted:**
  - Outline of the folded circuit to enable discussions with test probe suppliers.
  - SSA and CIC footprint is the one of the CBC2, will be adjusted later.
    - SSA and MPA due Q2-2017
  - Power and HV connectors placed, but we are still missing the input HV connection.
  - Alignment holes for folding and electrical test socket
  - Test probe interface proposal next to OPTO Service Hybrid wirebond interface.

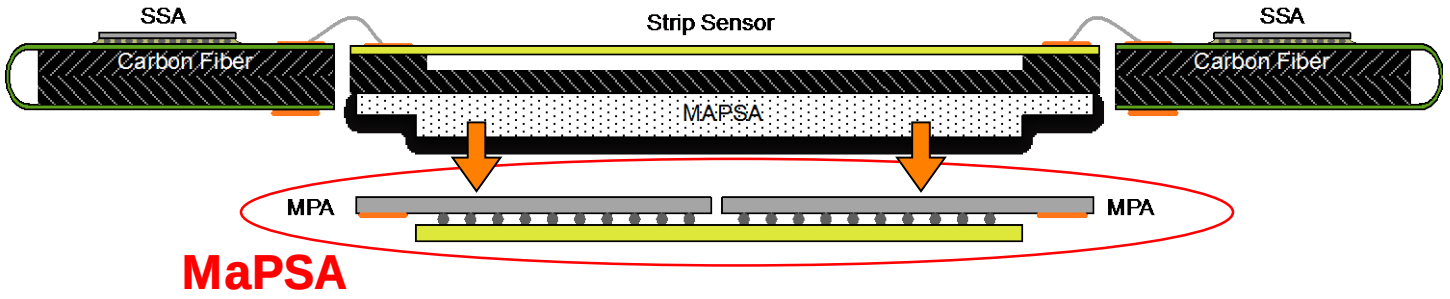


4. PS Macro Pixel SubAssembly (MaPSA)



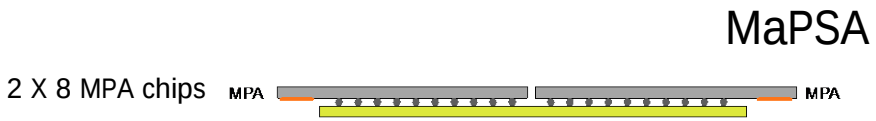




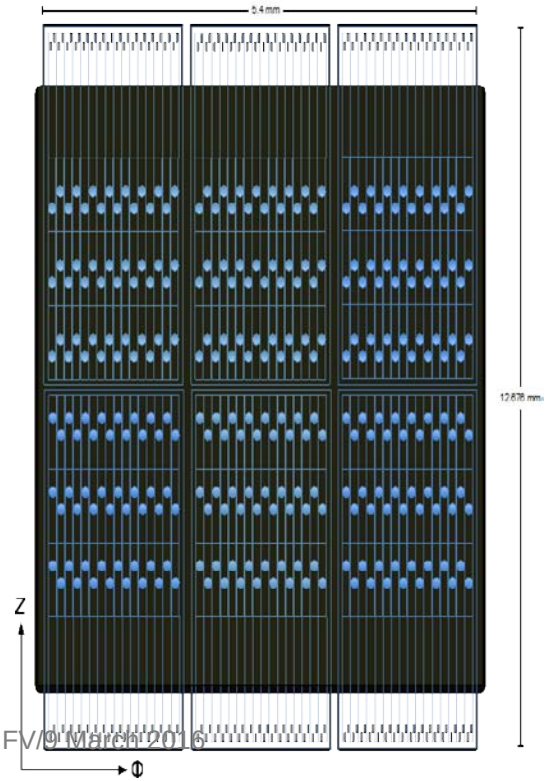


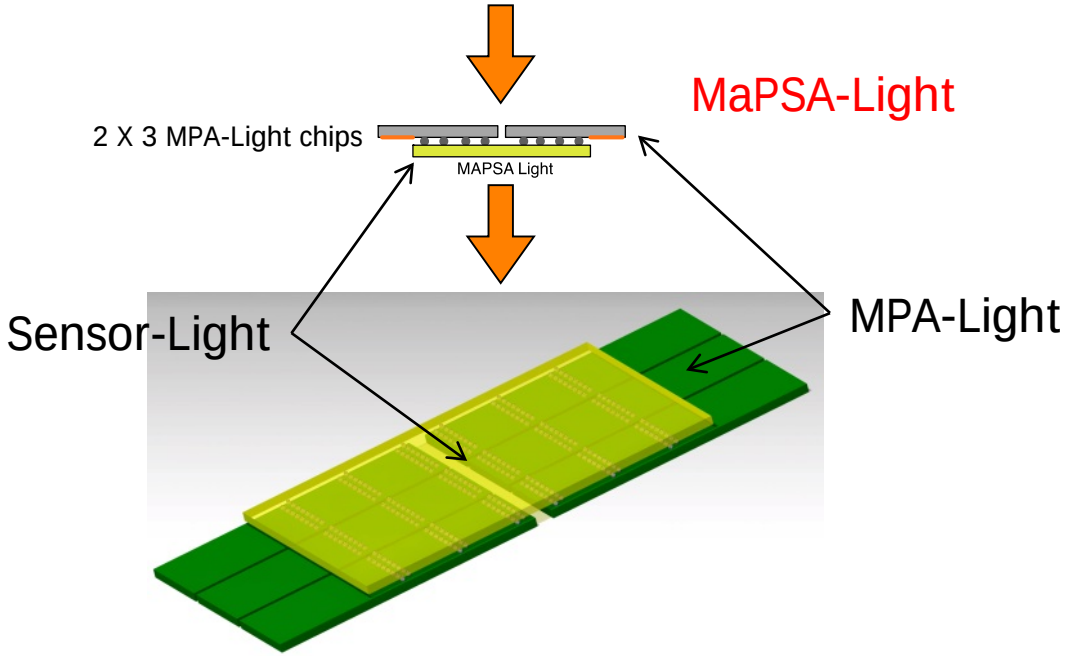
MaPSA-Light Development

- Assembly of 3 x 2 MPA-light chips for a total of 288 pixels
  - Bump-bondable to detector
  - Wire-bondable to hybrid
  - 5.4mm x 12.7mm

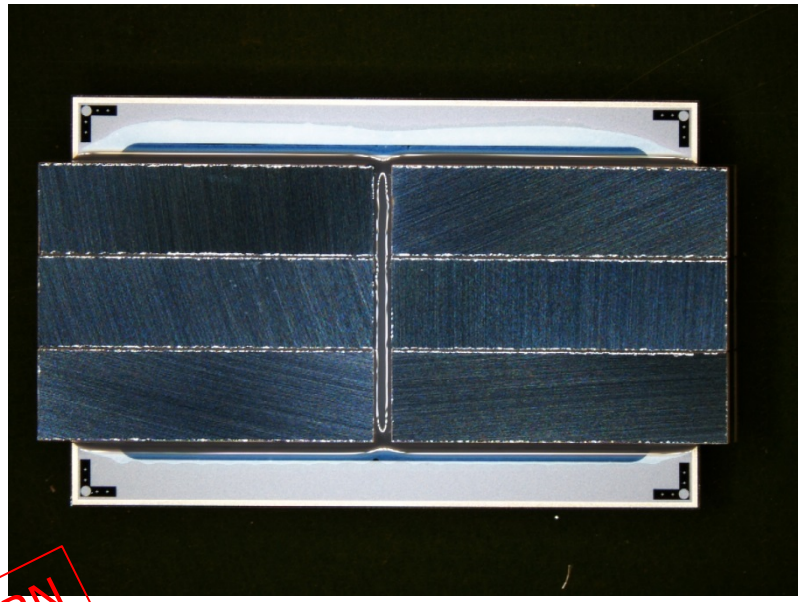


- MaPSA-Light is test vehicle in 2015-2017 timeframe

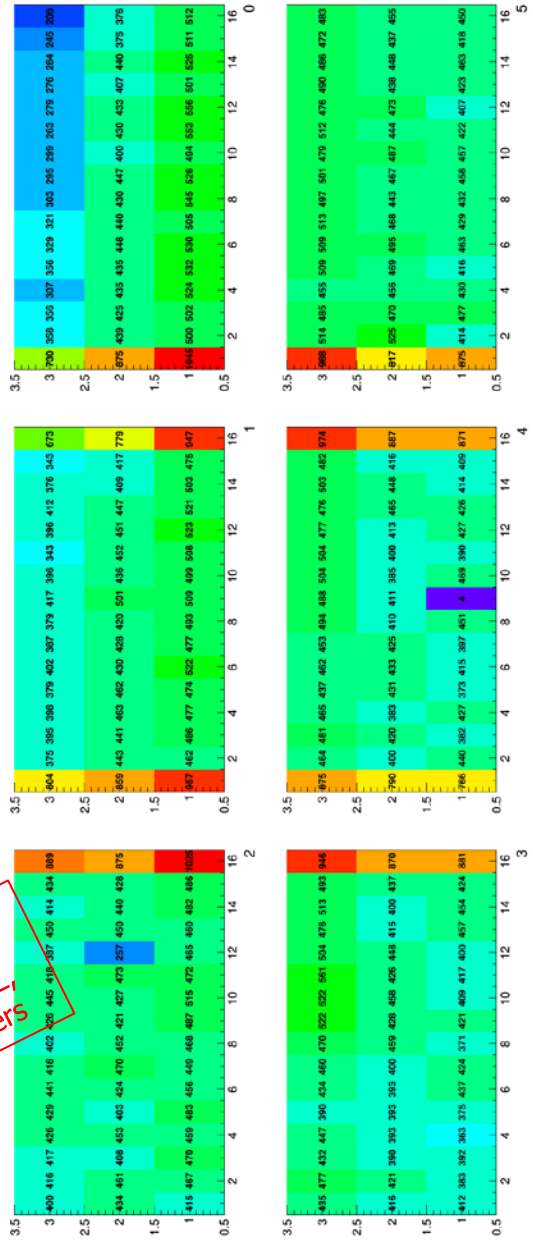




MaPSA-Light Assemblies

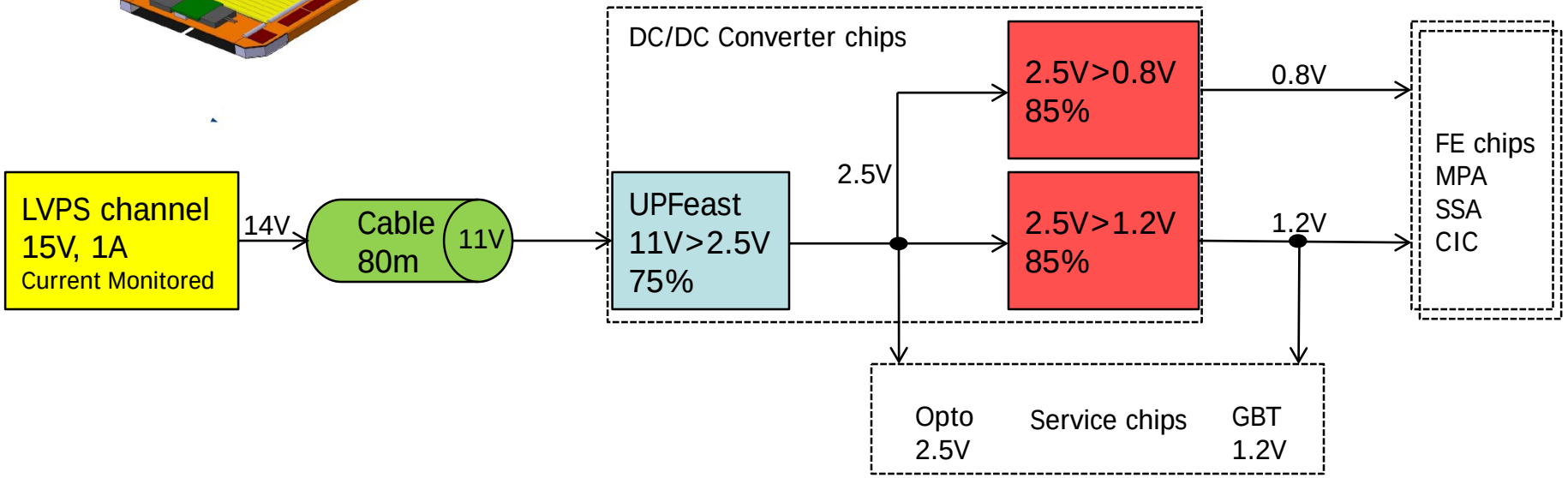


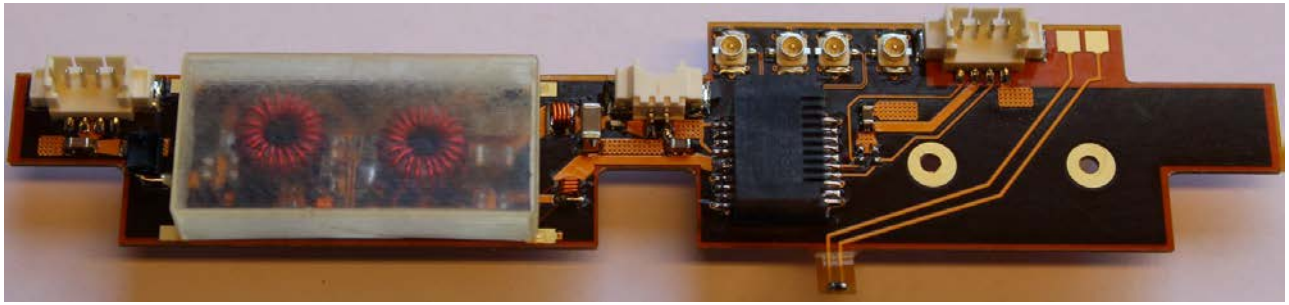
CERN



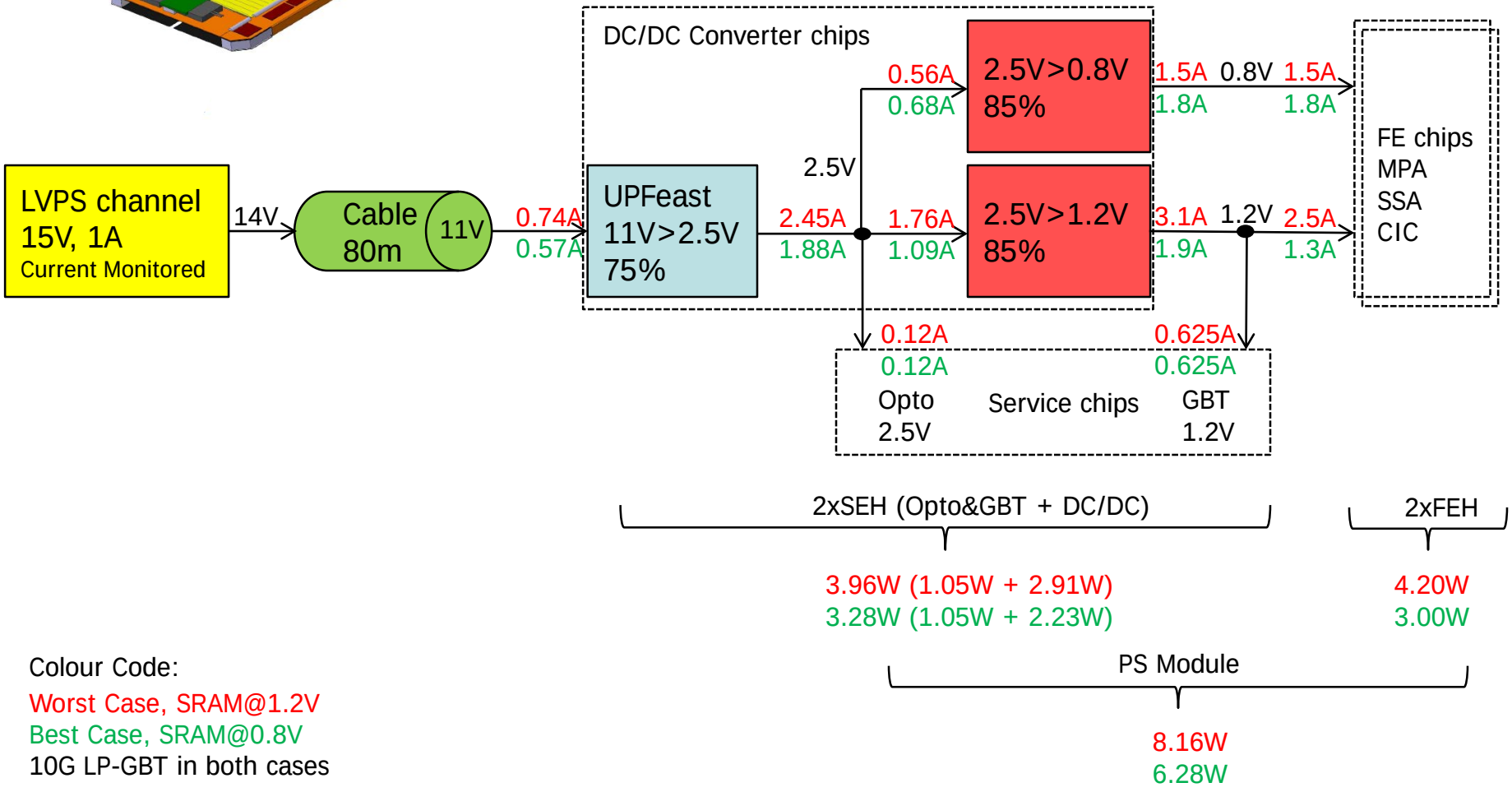
US- «East-Coast»
Boston, Brown, Cornell, FNAL,
Princeton, Rochester, Rutgers

5. Module Powering Scheme





5. Module Powering Scheme



Colour Code:
Worst Case, SRAM@1.2V
Best Case, SRAM@0.8V
10G LP-GBT in both cases

The Electronics for the Upgrade of the CMS Outer Tracker

Outline

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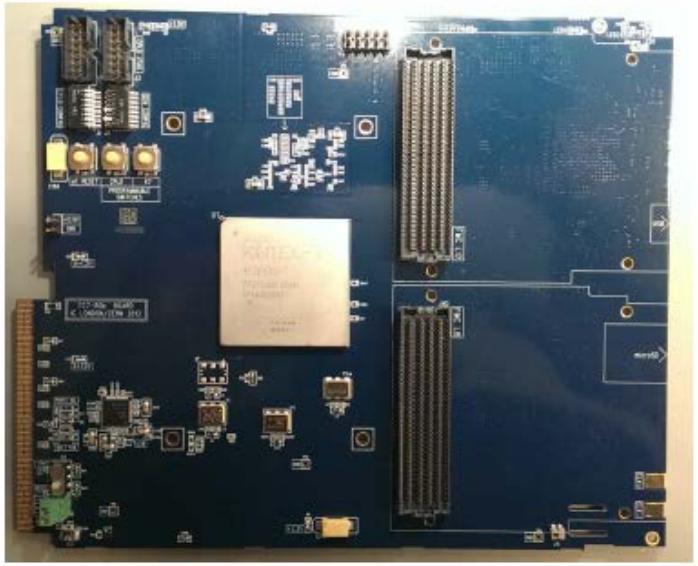
3. Back End DTC

CERN, Imperial College, Strasbourg

Back-End DTC will be developed as late as possible to profit from latest available technology and cost reduction.

In the meantime, GLIB and FC7 boards have been developed:



GLIB (Gligabit Link Interface Board)

- FPGA **Virtex 6** (~130k logic cells)
- **4 I/O SFP+ native** up to 6.5 Gbps (were used to connect 2 GLIBs)
- Port **Gbit Ethernet**: 1 Gbps with IPBUS
- µTCA connector
- 2*72Mb **SRAM** (static)
- 2 FMC slot supporting **HPC** mezzanines

FC7 (FMC carrier - Xilinx Series 7)

- FPGA **Kintex 7** (~420k logic cells)
- **No native SFP+** cages
- **No port Gbit** Ethernet
- µTCA connector
- 4 Gb **DDR-3 RAM** (dynamic)
- 2 FMC slots supporting **LPC** mezzanines, located on the same side (front side of xTCA crates)
- µSD card to select f/w versions, I2C values…

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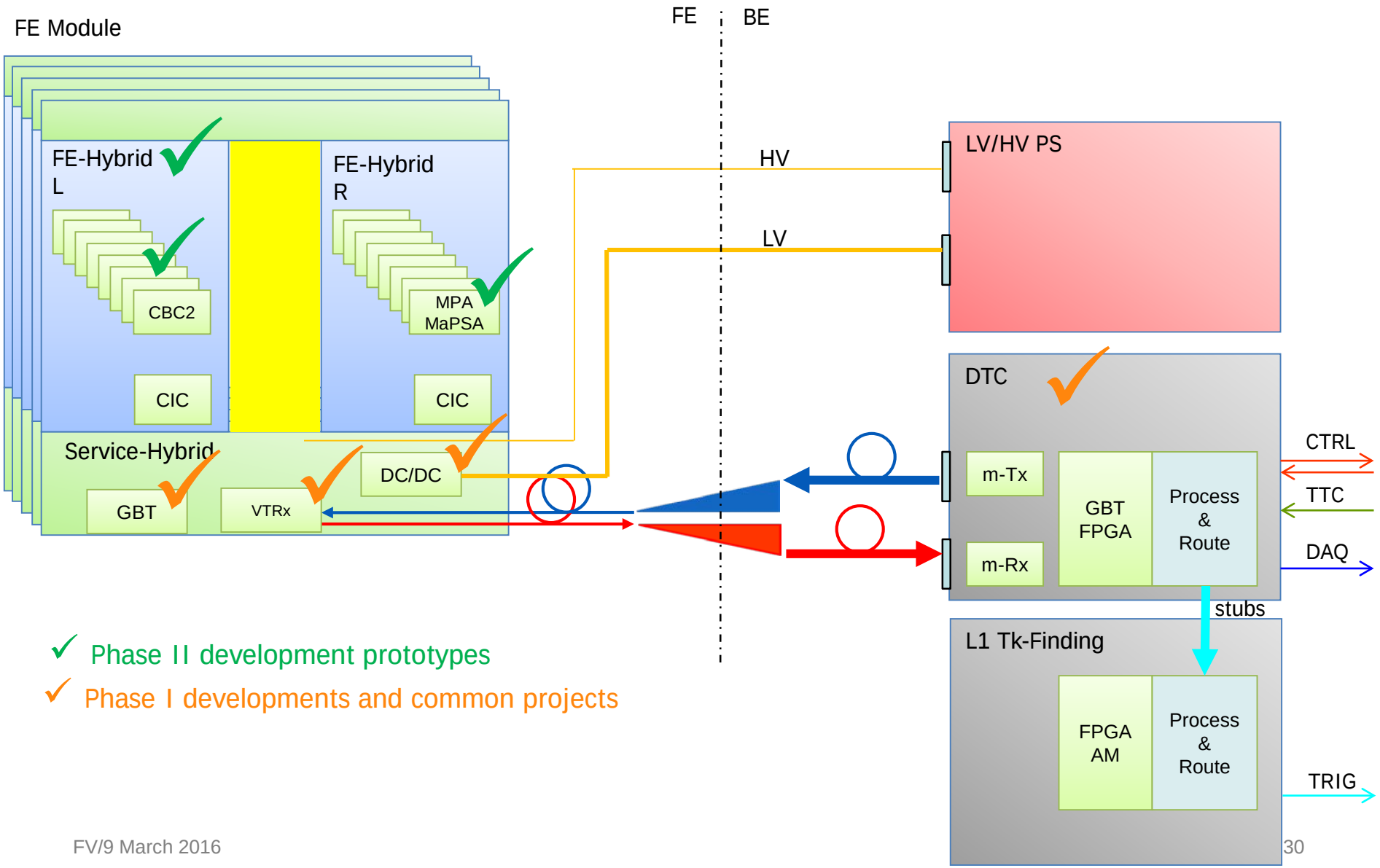
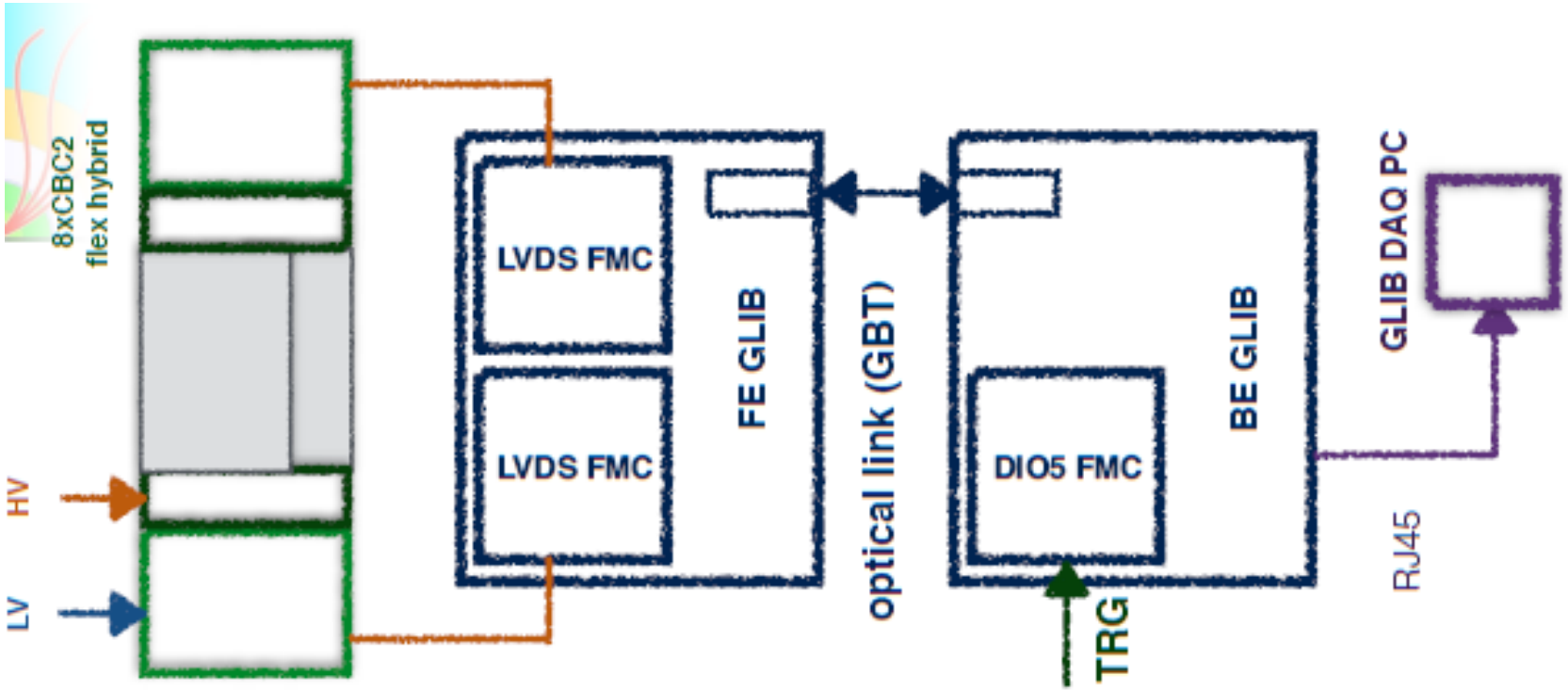
Electrical System: Recap



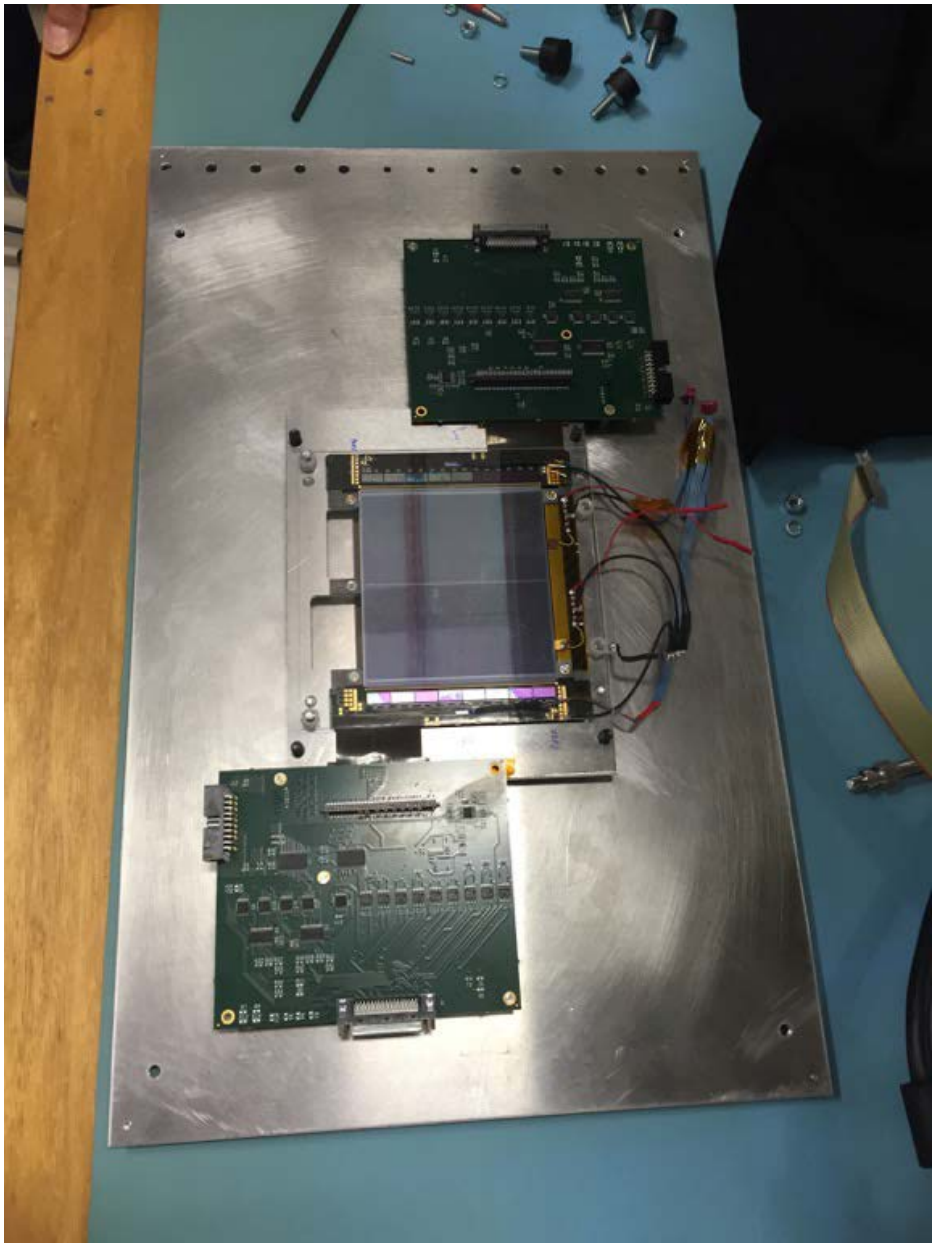
✓ Phase II development prototypes

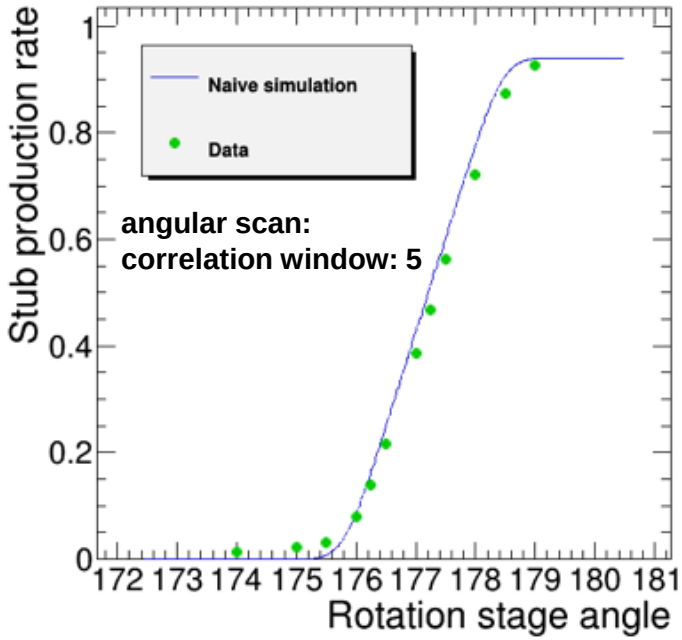
✓ Phase I developments and common projects

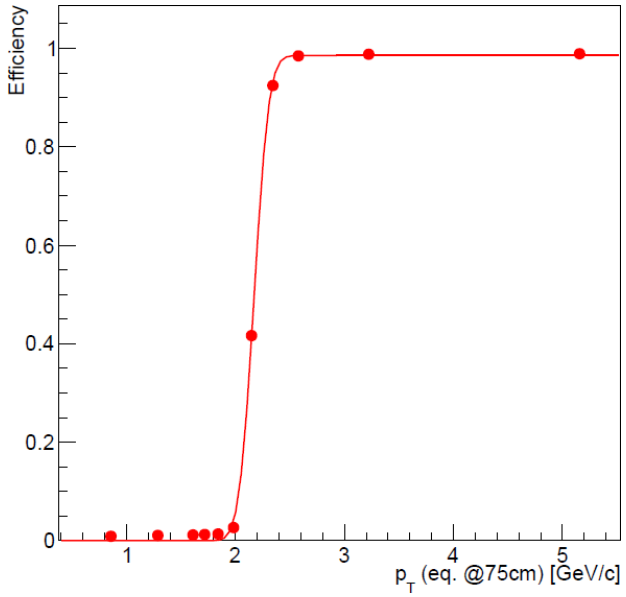
2S Beam Test 2015: Block Diagram



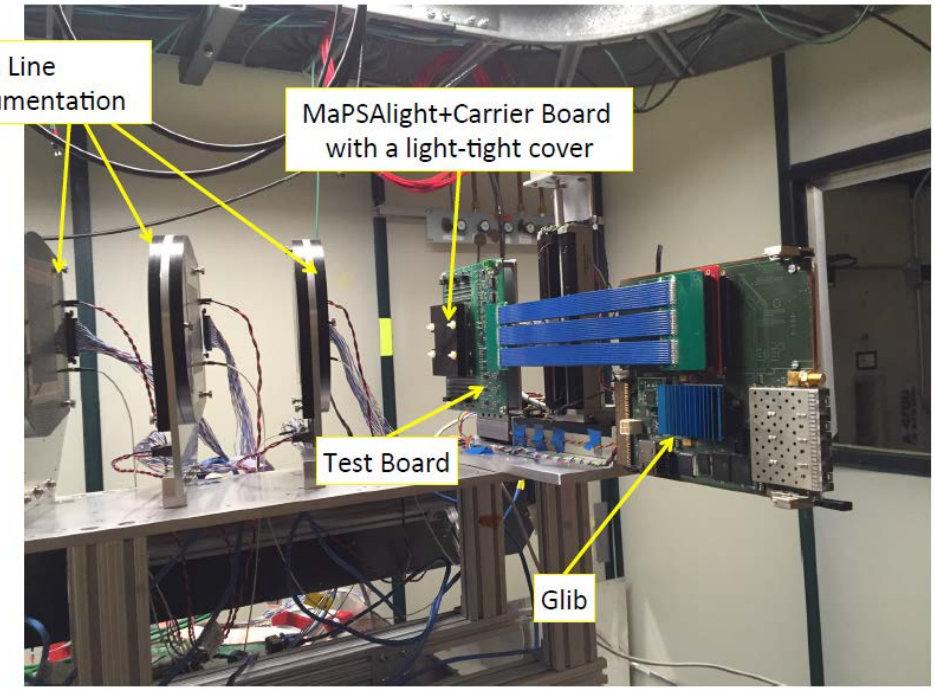
2S Beam Test 2015: Results

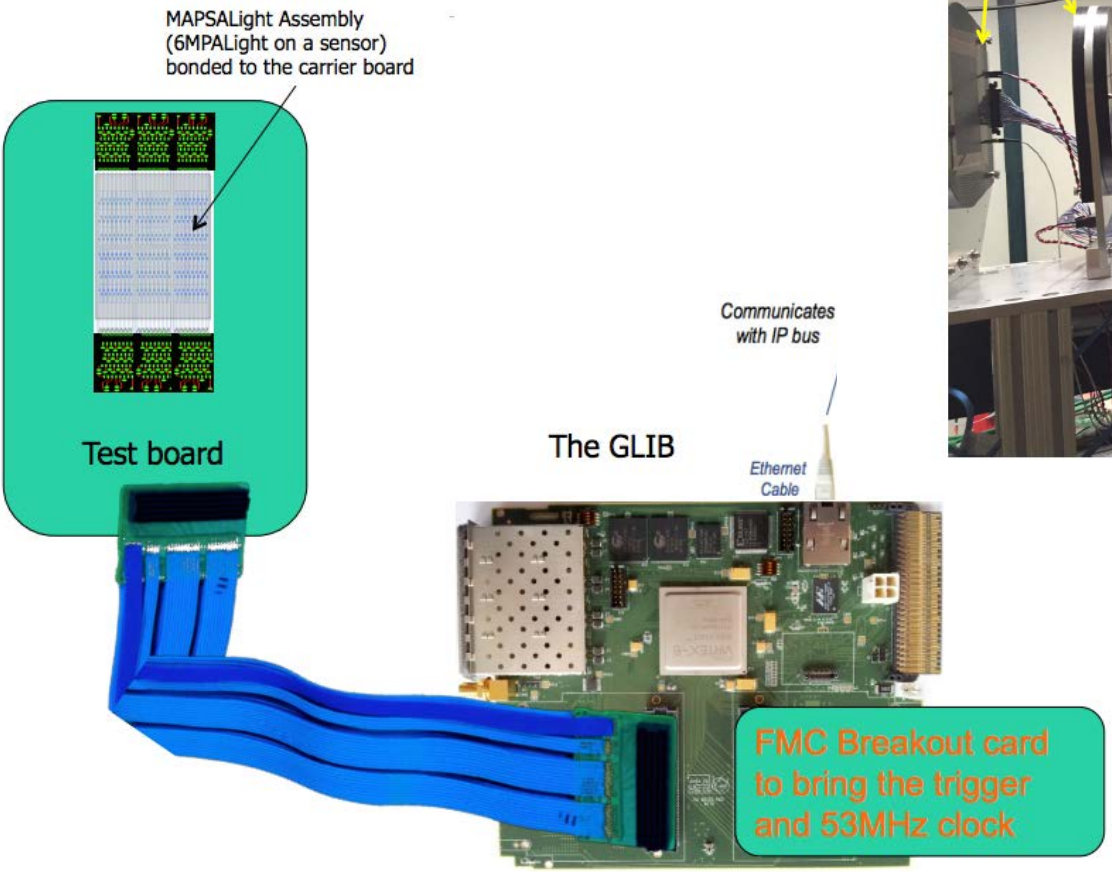






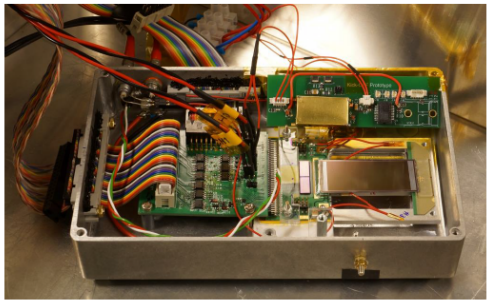
PS Beam Test 2015

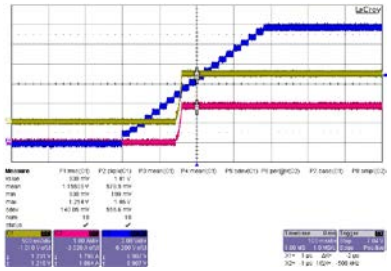


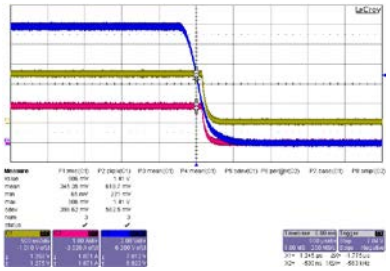


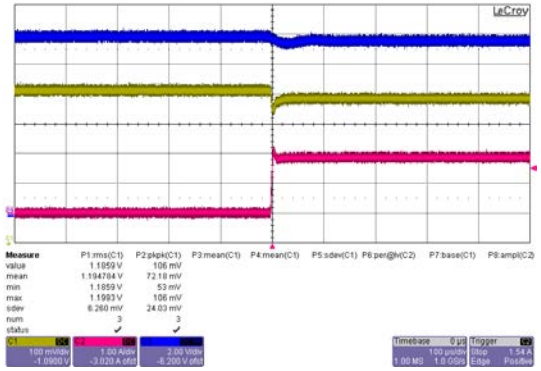
Powering system test 2016

- The power chain has been set up with presently available prototypes
  - CAEN A1516B power supply
  - An 86m long cable from the pixel detector
  - The rigid SH prototype with a hand-made shield
  - A 2-CBC2 mini-module with two sensors, read out electrically
- Allows to study module noise with different powering schemes, and dynamic behaviour of power supply

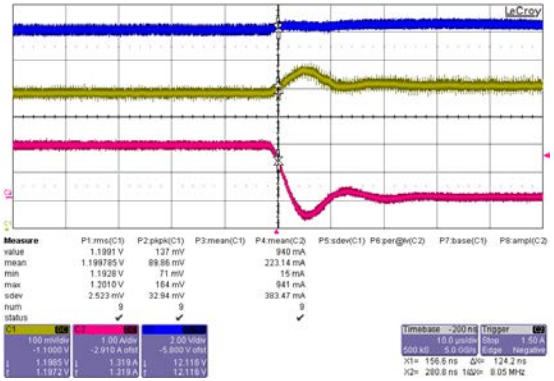








Vin at SH
Vout at SH (1.2V)
Iout of SH



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Conclusions

- Outer Tracker electronic system in good shape
  - Most FE functionality demonstrated with full-scale or mini-ASICs
  - Concentrator being simulated at system-level
  - Technology for FEH at industrial cutting edge
  - Power dissipation under constant scrutiny
- Rely heavily on common projects for data transfer and power
  - LpGBT, VTRx+, DC/DC converters, bulk power supplies
  - Will need to support them in all possible ways
- Full 2S DAQ chain demonstrated in beam (GLIB-based)
  - DTC backend being discussed, likely to be ATCA blade

- Next major demonstrators:
  - Full PS DAQ chain in 2016 (micro-module-based)
  - Full-size ASICs (CBC3, MPA, SSA, CIC) by late 2016 / early 2017
  - Full-size MaPSA in 2016 (Mockup) and 2017 (Functional)
  - Full TRIGGER chain by late 2017

- Detailed system integration now starting
  - Large enterprise with many pitfalls
  - Simulation and Documentation
  - Component and system-level qualification