CMS phase 2 pixel detector and its **electronics**

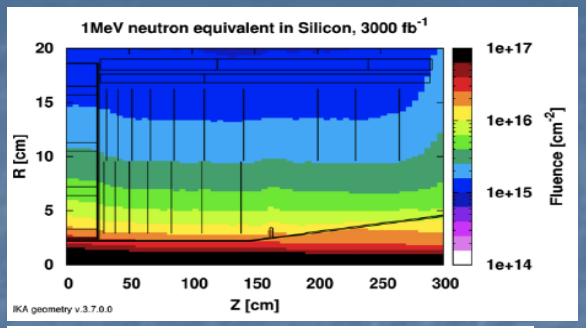
Jorgen Christiansen, CERN on behalf of the CMS phase 2 pixel community

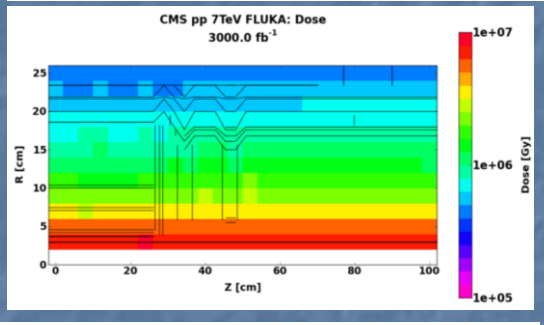
Outline

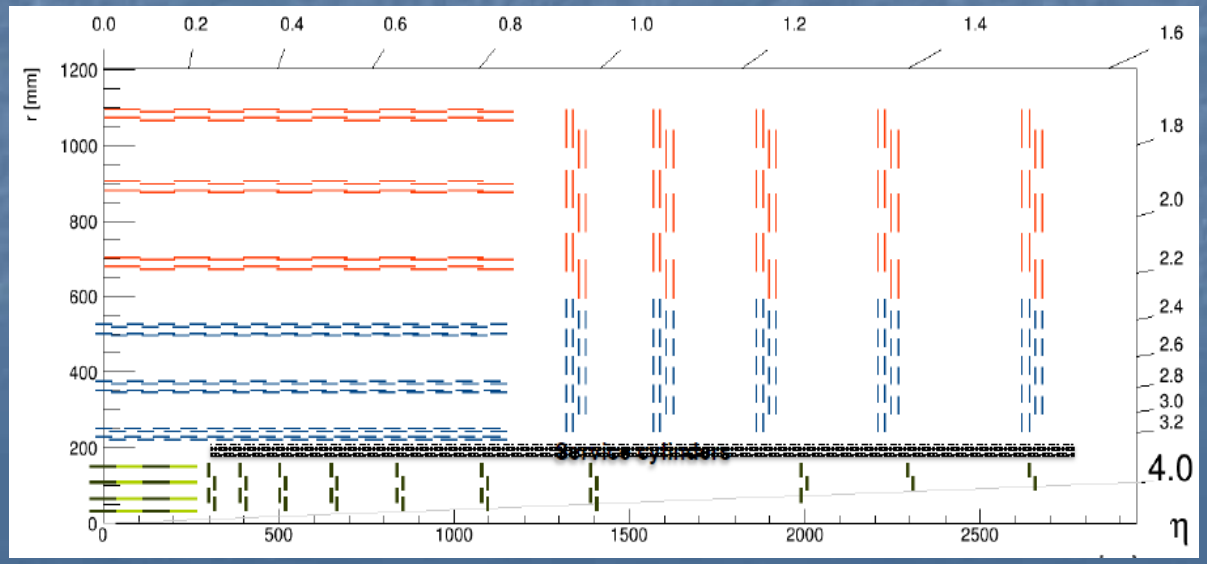
- Detector:
  - General layout
  - Requirements and challenges
  - (Pixel sensor)
- **Electronics:**
  - Pixel chip
  - Readout
  - Powering
- Summary and outlook

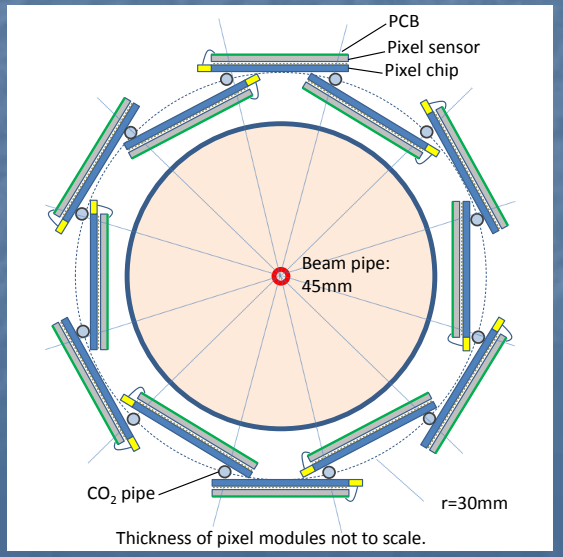
Phase 2 pixel detector

- Layout: Similar to CMS phase 1 pixel upgrade with extended forward coverage
  - 4 barrel layers: r = 3.0 ; 6.8; 10.2; 16.0 cm
  - 10 forward disks on each side (7 additional disks for forward coverage)
    - Forward layout under review to enable replacement with beam pipe in place.
  - Service cylinder(s) for services.
  - CO_2 cooling
- Pixel size:
  - Inner layers: 25x100um^2 and 50x50um^2 (100-150um thick)
    Outer layers: 50 or 100 x 100um^2
- Pixel sensor: Planar and possibly 3D
- Radiation: 1Grad , 2 10^{16} neu/cm^2, inner layer, 10 years
  - 1/r^2 dependency





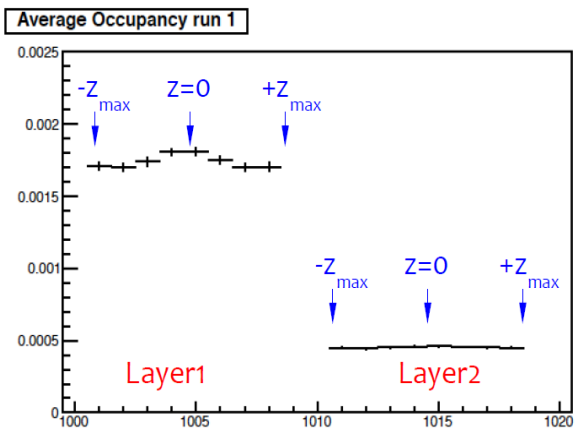




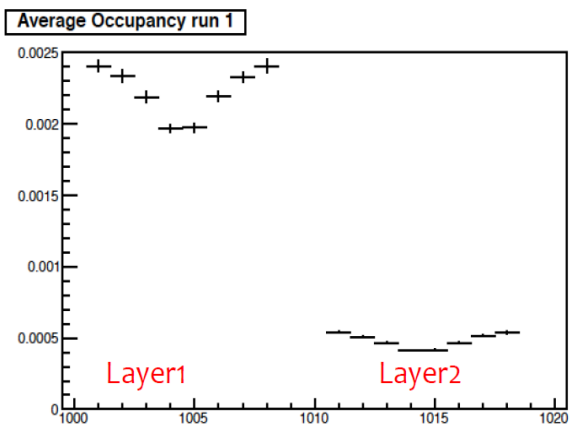
Electronics challenges

- Extreme hit rates: 3GHz/cm^2, inner layer, PU=200
  - Can be higher if not well optimized pixel aspect ratio and pixel sensor thickness
- Extreme radiation tolerance: 1Grad (10years)
- Small/thin pixels maintaining 25ns time tagging: Threshold and Time walk
- Long trigger latency: 12.5us
  - Buffering requirements increased factor ~100, High density technology critical
- High trigger rate: 750KHz
  - Readout rate increased by factor ~100: ~1TBytes/s
- Low mass -> Low power, "exotic" powering system

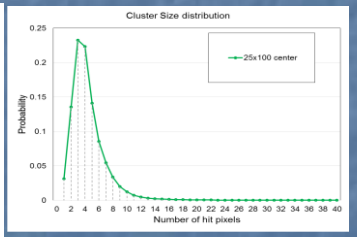
Large, complex, high rate, high density, mixed signal, low power, rad hard, expensive, , pixel chip critical: **RD53**

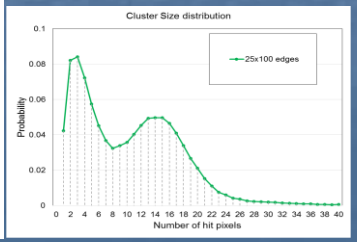


Rectangular cell 25x100x150 µm^3

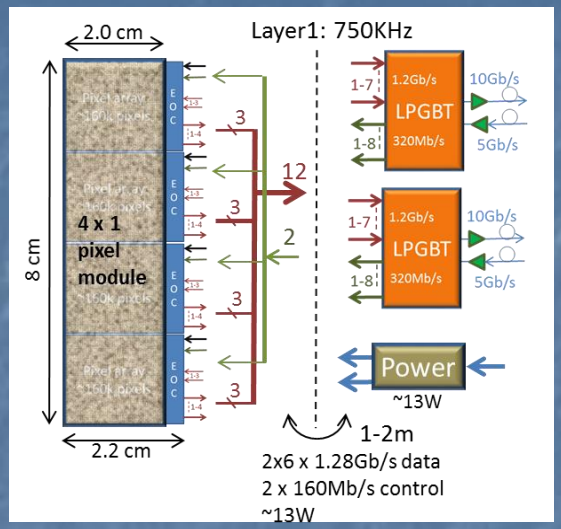


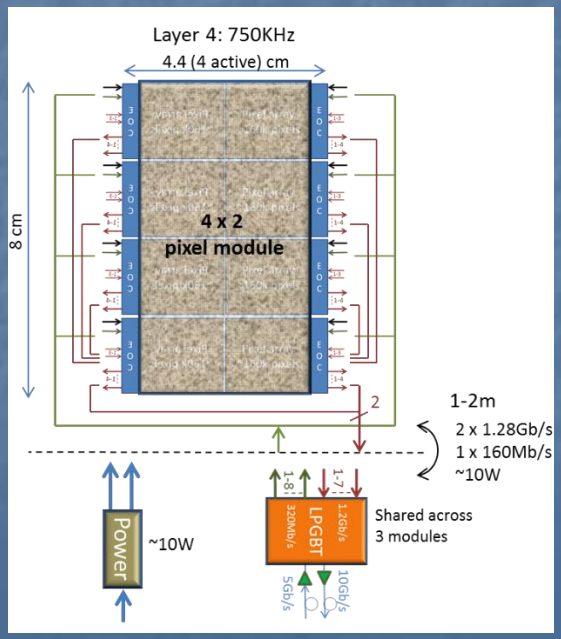
Square cell 50x50x150 µm^3



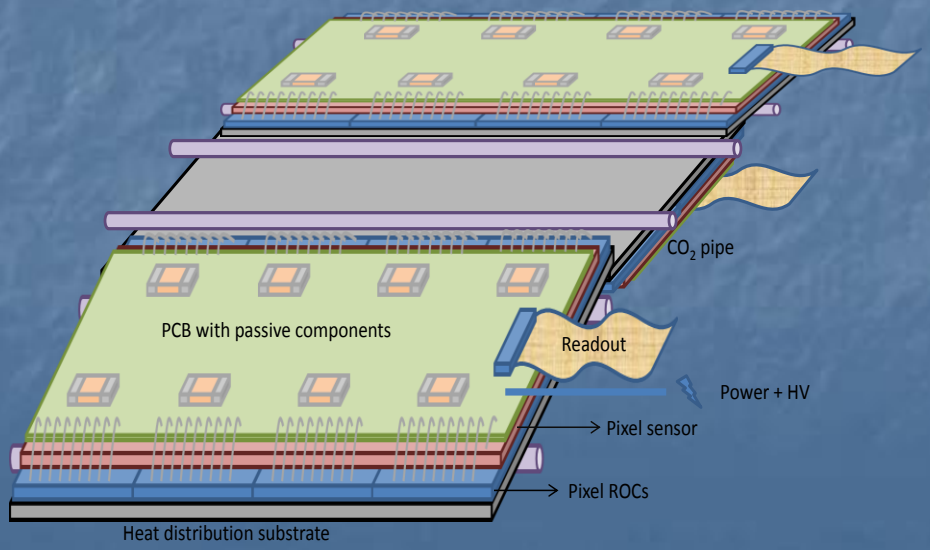


Modularity





- Modular building blocks
  - Minimize number of different module types.
- Will be adapted to:
  - Bump bonding to pixel sensors: Module size and yield
  - Pixel sizes and sensor types
  - Mechanical and cooling constraints
  - Powering structure and granularity
  - Readout rates and granularity

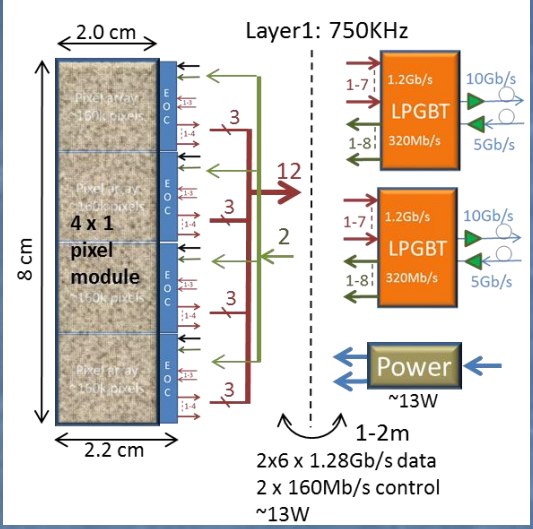


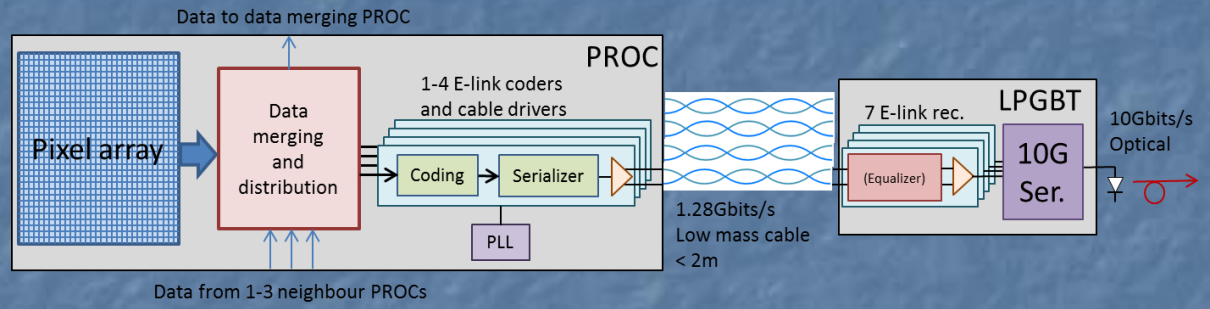
System summary

with 1x4 and 2x2 modules

Pixel system (1x4 & 2x2 modules) (PU=200, Trg=750KHz)	L1	L2	L3	L4	RingI disks	RingII disks	RingIII disks	Total
r inner (mm)	30	68	102	160	45.0	83.3	120.0	
r outer (mm)					85.0	123.3	160.0	
Pixel size (um^2)	50x50	50x50	50x50	100x100	50x50	100x100	100x100	
Track rate @ PU200 (MHz/cm^2)	750	188	94	47	150	94	75	
Track rate (relative)	1	1/4	1/8	1/16	1/5	1/8	1/10	
Hit rate @ PU200 (MHz/cm^2):	3000	750	375	188	600	375	300	
Relative	1	1/4	1/8	1/16	1/5	1/8	1/10	
Facets:	12	24	40	60				
Modules per ladder/disk:	8	8	8	8	16	20	28	
Module size x (chips)	**4**	4	4	**4**	2	2	2	
Module size y (chips)	**1**	1	1	**1**	2	2	2	
Module size x (cm)	8.0	8.0	8.0	8.0	4.0	4.0	4.0	
Module size y (cm)	2.0	2.0	2.0	2.0	4.0	4.0	4.0	
Disks					12	16	20	
Modules	96	192	320	480	192	320	560	**2160**
Power per module (W)	13	9	9	5	9	5	5	
Chips	384	768	1280	1920	768	1280	2240	**8640**
Power per chip (W)	3.2	2.2	2.2	1.3	2.2	1.3	1.3	
Power per stave, per ring per disk (W)	101	69	69	41	138	102	143	
Power per layer, per all rings (W)	1210	1653	2755	2458	1653	1638	2867	**14234**
Sensitive surface (m^2)	0.15	0.31	0.51	0.77	0.31	0.51	0.90	**3.46**
Pixel channels (M)	61	123	205	77	123	205	90	**883**
Tracks/clusters per chip per Bx	75	19	9	5	15	9	8	
Hits per chip per bx	300	75	38	19	60	38	30	
(Raw hit event size per chip (bits))	7264	1864	964	514	1504	964	784	
Clustered event size per chip (bits)	5014	1302	683	373	1054	683	559	
Total event size, clustered hits (Kbytes)	235	122	107	88	99	107	153	**910**
(Raw data rate per chip (Gbits/s))	5.45	1.40	0.72	0.39	1.13	0.72	0.59	
Clustered data rate per chip (Gbits/s)	**3.76**	0.98	0.51	**0.28**	0.79	0.51	0.42	
Data rate per module	**15.04**	3.90	2.05	**1.12**	3.16	2.05	1.68	
Readout links per module @1.2Gbits/s	**12**	4	2	**1**	4	2	2	
Total readout links	1152	768	640	480	768	640	1120	**5568**

Readout: E-links, LPGBT, optic



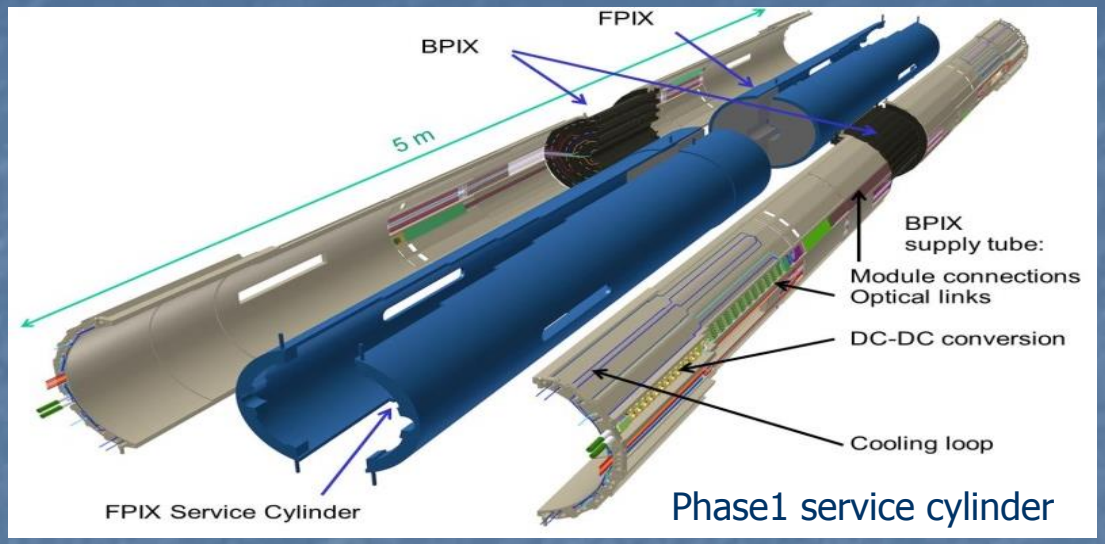


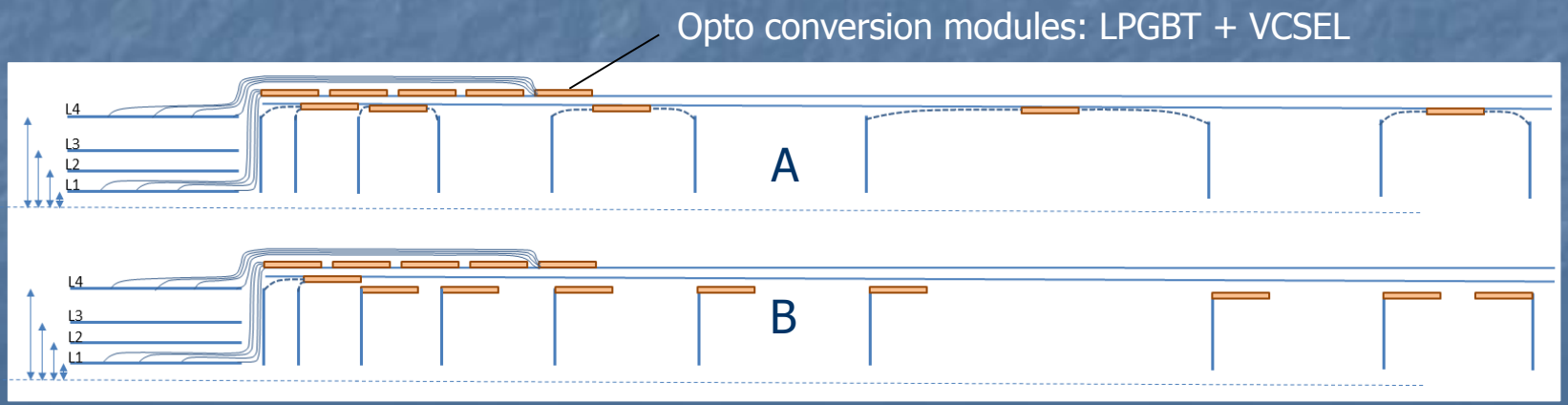
- Modest rate (1.28Gbits/s) E-links to "remote" LPGBT
  - Rate that makes sense for input to LPGBT (10Gbits/s)
    - Requested 1.28 and 2.56 Gbits/s
    - Would have preferred 8 (instead of 7) input links
  - Speed could be seriously affected by radiation damage
  - Very low mass cables critical
  - High rate regions: Max 4 E-links per chip
  - Low rate regions: Shared E-link between 2 – 4 pixel chips
- One control link per module @ 160Mbits/s
- ~5500 readout + ~2000 control E-links, 0.1-1m
  - Alu Kapton Flex or twisted pair
  - 20% of links from inner barrel for 4% of pixel surface
- 1k 10Gbits/s optical links: ~1 TBytes/s
- LPGBT / VCSEL located on service cylinder
  - 100Mrad, 10^{15} neu/cm^2
  - In forward acceptance so mass also critical
- Readout rates under verification.
  - Monte Carlo hit data
  - Data formatting, Clustering, Data compression

Alternatives:

- Single High rate (4-6Gbits/s) electrical link per chip to remote laser (ATLAS)
  - No use of LPGBT
- Opto conversion on pixel module
  - Outer modules with "low" radiation and low rates and less space constraints
  - Silicon photonics

Service cylinder



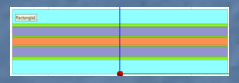
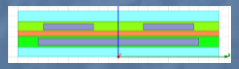
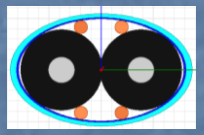
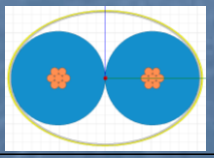
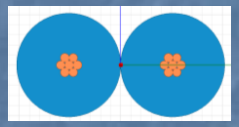


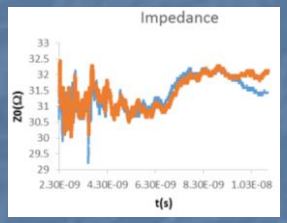
E-link cable options

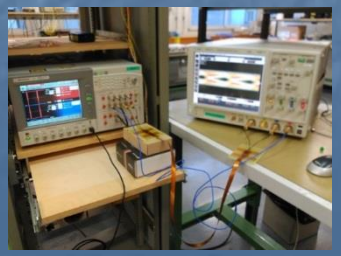
Cable Option:	Conductor size/dia. (µm)	Wire resistance (Ohm/m)	Mass (g/m)	Mass ~9000 Cables 0.5m (kg)	Signal pair	Ground/ shield	dielec.	isolator
36AWG Twisted pair, Cu with shield	125	2.74	0.82	**3.70**	27%	40%	0%	33%
36AWG Twisted pair, Cu, no shield	125	2.74	0.49	**2.21**	45%	0%	0%	55%
Twisted pair Cu with polymide insulation, no shield	125	2.74	0.24	**1.08**	92%	0%	0%	8%
Cu cladded Al twisted pair, polymide insulation, no shield	125 Al 5 Cu	4.04	0.10	**0.46**	83%	0%	0%	17%
75µm Differential pair Kapton and Cu, with soldermask. 35µm gnd plane	140 x 35	6.86	0.57	**2.56**	15%	55%	19%	11%
75µm Differential pair Kapton and Cu, with soldermask. 10µm meshed gnd	140 x 35	6.86	0.27	**1.23**	32%	7%	39%	22%
75µm Differential pair Kapton and Cu, without soldermask. 10µm meshed gnd.	140 x 35	6.86	0.21	**0.96**	41%	8%	50%	0%
75µm Differential pair Kapton and Al, with soldermask. 35µm gnd plane	140 x 35	11.51	0.29	**1.29**	9%	33%	37%	21%
75µm Differential pair Kapton and Al,with soldermask. 10µm meshed gnd	140 x 35	11.51	0.20	**0.89**	13%	3%	54%	30%
75µm Differential pair Kapton and Al,without soldermask. 10µm meshed gnd.	140 x 35	11.51	0.14	**0.62**	19%	4%	77%	0%

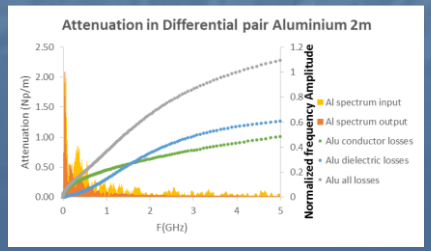
Cable simulation and test

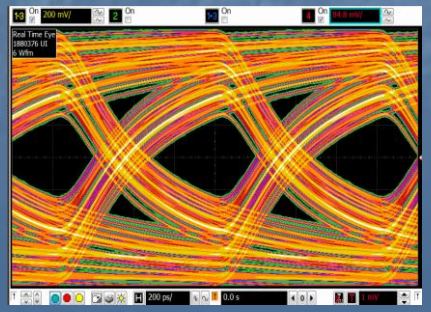
- Alu kapton flex and twisted pair: 0.1 – 1(2)m
- Minimize mass for acceptable cable losses
- S-parameter models
  - Verification of link: Eye diagrams, etc.
  - Cable driver optimization: Pre-emphasis, etc.
- Extraction of cable models
  - Q3D simulation models
  - TDR measurements
  - VNA measurements
  - FPGA/pre-emphasis measurements
- Cross coupling between cables: To come
  - Shielded/Unshielded twisted pairs
  - Stacking of multiple flex cables
- Prototyping: To come
  - Connectors or soldered ?
- Collaboration with ATLAS

Image of the cable	Cross section for simulation in Q3D	Specifications
A. 		W_{trace} = 750µm W_{ground} = 252µm $T_{dielectric}$ = 25.63 µm T_{trace} = 33.32 µm T_{ground} = 36.47 µm
B. 		W_{trace} = 250µm W_{ground} = 800µm $T_{dielectric}$ = 25.14 µm T_{trace} = 31.54 µm T_{ground} = 35.98 µm d = W_{trace}
C. 		D_{Cu} = 125 µm $D_{isolator}$ = 390 µm T_{AlFoil} = 10 µm $D_{shieldWires}$ = 63.5 µm $T_{polyesterFoil}$ = 30 µm
D. 		$D_{CuStrands}$ = 42 µm $D_{isolator}$ = 512 µm T_{AlFoil} = 10 µm $T_{polyesterFoil}$ = 30 µm
E. 		$D_{CuStrands}$ = 42 µm $D_{isolator}$ = 512 µm T_{AlFoil} = 10 µm $T_{polyesterFoil}$ = 30 µm

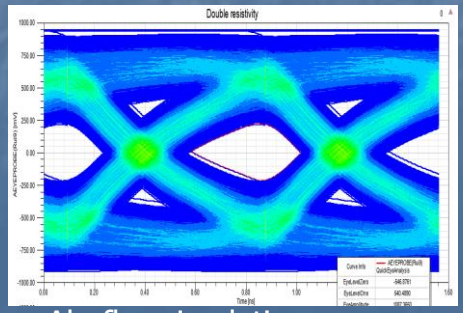








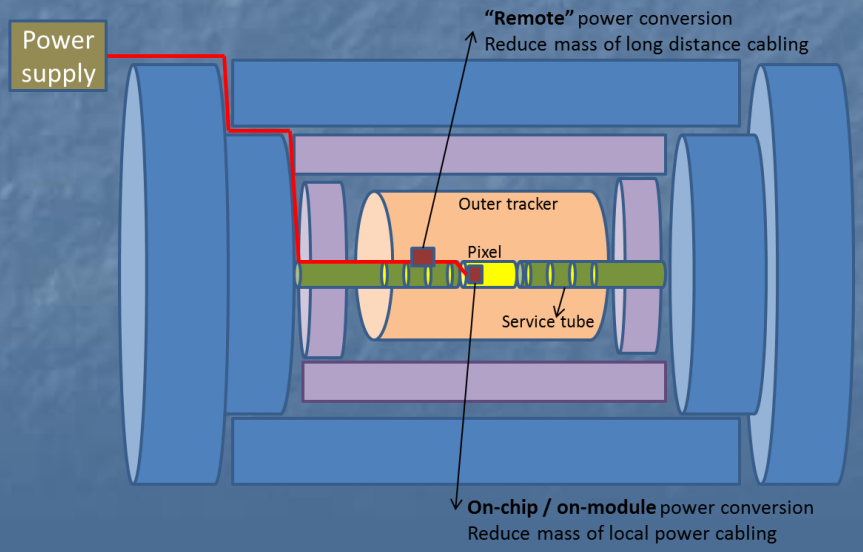
Alu flex measurement



Alu flex simulation

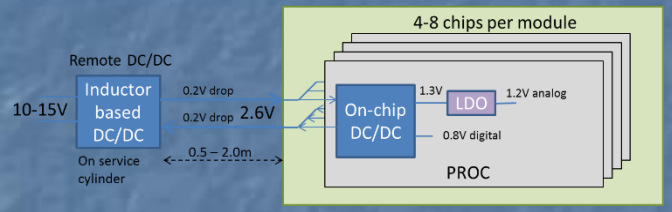
Power distribution

- Deliver required power to pixel modules/chips
  - 8-16KW total power for ~4m^2 pixel detector (estimate)
  - Power density:
    - **Inner**: High rate (~3GHz/cm^2) – Small pixels (50x50um^2): 0.5W – **1W/cm^2**
    - **Outer**: Low rate (200MHz/cm^2) - Large (100x100um^2) pixels: **¼ - ½ W/cm^2**
    - **Previous** generation pixel systems: **~ ¼ W/cm^2**
  - ~1V for 65nm pixel chips -> 8000 – 16000A !
  - Low noise for analog critical
  - HV sensor bias
- Minimal mass in central tracker, including forward region

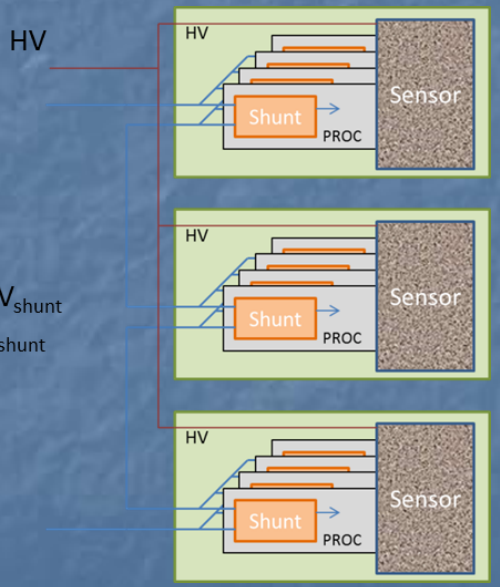


Power options

- **Direct from external PS: Excluded**
  - Huge power cables and huge power losses in cables
  - **Local power cabling** within acceptance: 1-2m
    - L=1m, V_{drop}=0.2V, I=16kA => Mass= **12kg**
    - L=2m, V_{drop}=0.2V, I=16kA => Mass= **48kg** (L^2 dependency)
  - **Global power cabling**: 50m
    - L=50m, V_{drop}=1V (problematic !), I=16kA => **Mass= 6100kg**, 2/3 power lost in cables
- **One-stage on-chip/on-module DC/DC: Not attractive for low conversion factors**
  - Low conversion ratio limited by technology and radiation: **2-4**
    - Local 1m: 12kg/ 2-4 = **3-6kg**
    - Local 2m: 48kg / 2-4 = **12-24kg**
    - Global 50m: 6100kg/ 2-4 = **1500 – 3000kg**
  - **If on-chip/on-module power conversion factor of ~10 can be envisaged then this can be an option**
    - **Radiation and high voltages makes this extremely difficult**
- **One-stage remote DC/DC: Excluded**
  - Local power cables mass will be the same as "direct from external".
    - Local 1-2m power cabling: **12-48kg**
    - Global power cabling: 6100kg / ~10 = **610kg**
- **Two stage DC/DC (remote + on-chip): Not attractive**
  - Local power cabling: 6-24kg
  - Material + required space on service cylinder for DC/DC plus related services
  - Complicated
- **Serial powering: Attractive, test and detailed studies to be made**
  - Cable mass reduced proportional to number of units put in series (e.g. 8)
  - System aspects delicate and critical



Two stage DC/DC



Serial powering

Comparison

Power system	Two stage DC/DC		In-module Serial		Across-Module serial		Unit
Power scenario	Cons.	Opt.	Cons.	Opt.	Cons.	Opt.	
Active pixel chip power	15.8	8.8	15.8	8.8	15.8	8.8	kW
On-chip DC/DC, LDO	2.4	1.4	6.1	3.1	6.1	3.1	kW
Excessive power			2.2	1.2	2.2	1.2	kW
Total module power	**18.2**	**10.2**	**24.1**	**13.1**	**24.1**	**13.1**	kW
Power cable losses	**2.8**	**1.6**	1.1	0.6	**0.9**	**0.5**	kW
Total power	21.0	11.8	25.2	13.7	25.0	13.6	kW
Power cabling mass	**5.33**	**2.99**	**2.08**	**1.14**	**1.79**	**0.97**	kg
Power cabling in barrel	0.45	0.25	0.17	0.09	0.15	0.08	kg
Remote DC/DC mass	**2.8**	**1.4**					kg
Local cable reduction	**1.5 (2.2)**		**5.8 (4)**		**6.9**		

Same Basic assumptions:
- 1m local power cabling counted
- Max 0.2V voltage drop on 1m wire

Other materials:
- Chips + sensors: ~2kg
- Readout links: 0.5-4kg
- Cooling, Mechanics, beam pipe: ?

- Serial power attractive (only viable solution for sufficiently low mass)
  - ~1/3 material in power cables
  - ~1/3 power losses in cables (less worries about cabling cooling)
  - No remote DC/DC with associated mass and integration problems
  - Smart Shunt – LDO currently under design in 65nm for RD53
  - Can possibly be even more advantageous:
    - Higher voltage drop on local power cables can possibly be supported.
    - Long distance power cabling of which some will be in forward acceptance
  - Major worries: Noise injection, Failure propagation, Grounding
    - R&D and extensive testing required

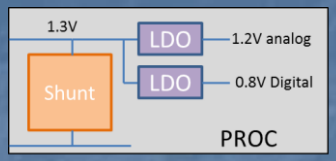
CMS pixel Power review

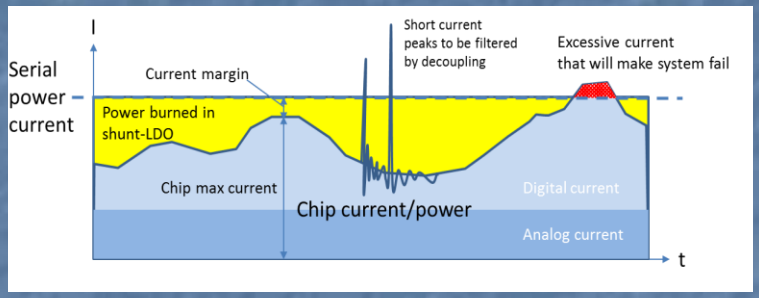
- Direct powering:
  - Excluded
- DC/DC on service cylinder (CMS phase 1 pixel upgrade)
  - Excluded
- DC/DC on pixel module:
  - Additional material from inductors/capacitors on pixel models
  - Further R&D required, but no groups working on this.
  - High risk that combination of radiation and high voltage (8-10v) will not be possible
- Two stage DC/DC: Service cylinder + pixel module
  - Complicated and not attractive (but a possible backup option)
- **Serial powering:**
  - **Baseline option: lowest possible material budget**
  - **R&D required at both chip level and system level**

Serial power R&D

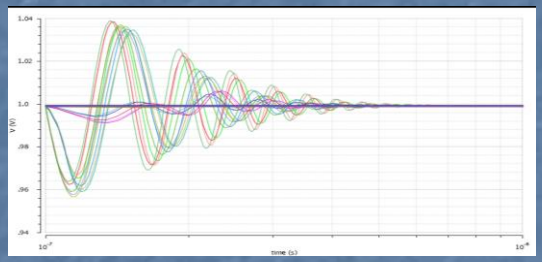
- System tests/learning: Now
  - Start with FEI4 chips that have built-in shunt-LDO
  - Collaborate with / learn from ATLAS pixel powering groups
- System level simulations with behavioural/detailed model of shunt-LDO regulator: Now
  - Current steps with different time constants and realistic inductances and local decoupling.
  - Detailed power profiles from simulations of chip implementation
- System tests with shunt-LDO prototype: 2016
- System tests with RD53A with shunt-LDO: 2017
- System aspects: To come
  - EMC, Noise propagation, cabling, services, connectors, DSS, fault propagation, etc.
- Off detector power supplies for serial powering

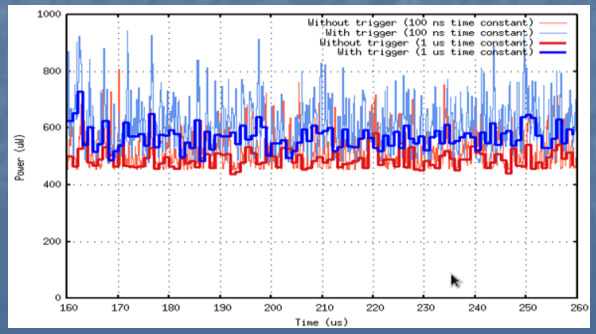
Physicists dream and/or engineers nightmare ?





Shunt-LDO simulations with 100% current change, Different current changing rates, including wire bonding inductances, local de-coupling, etc.

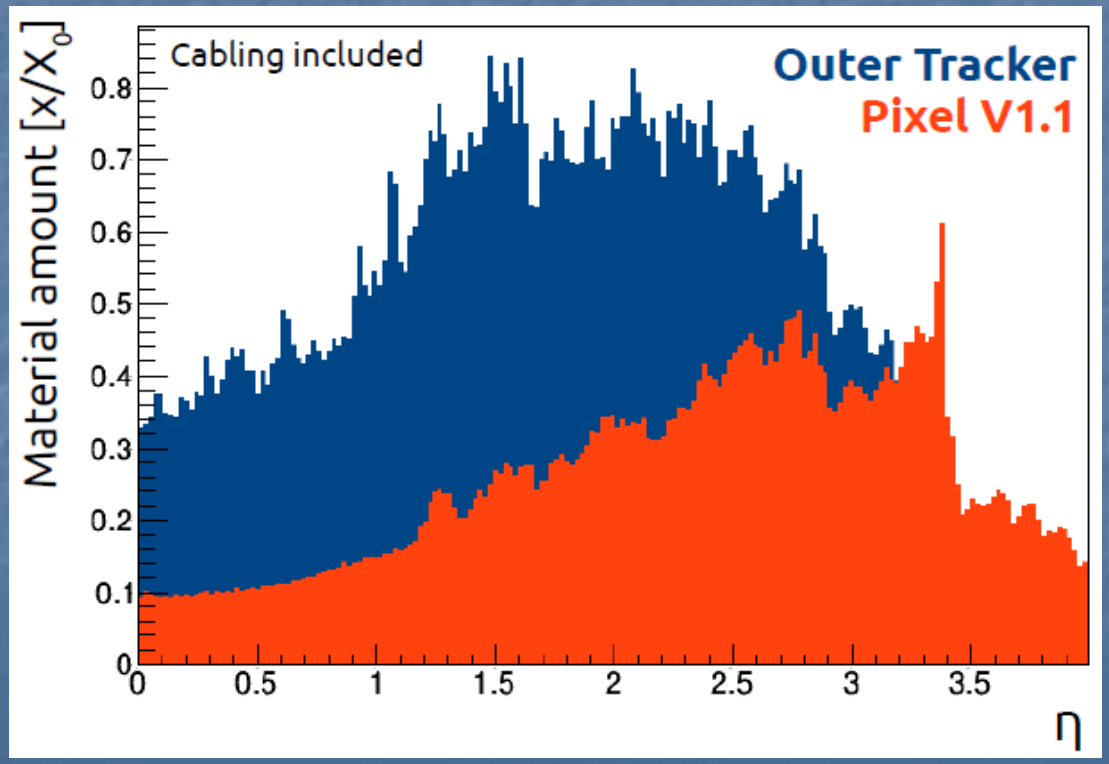




Power profiles with Monte Carlo hits, Triggers and different implementations/architectures. From detailed gate level simulations after place and route and with circuit parasitics

OK for physics ?

- Material budget of tracker/pixel estimated with assumed baseline solutions
- Tracking performance evaluated and looks acceptable.
- Detailed effects on physics channels to be studied



Summary

- Phase 2 Pixel detector and its electronics is very challenging
  - Highest rates, Highest radiation, Highest detector granularity/resolution, Long trigger latency, High trigger rate, and not to make things too "easy" ~Zero mass required.
  - Focussed R&D Vital NOW
- Critical pixel chip design in 65nm CMOS progressing well in RD53
  - Radiation tolerance remains an issue
    - Replacement strategy: Inner layers after ~5 years.
    - Analog demonstrated to work well after high radiation
    - Focussed R&D on digital: Dedicated digital radiation test chip (RD53, MPA and LPGBT) and small scale pixel chip demonstrators: FE65-P2, CHIPIX65
  - Full scale RD53A demonstrator end this year
  - Time will show if final pixel chip(s) for CMS and ATLAS will be the same or differently optimized versions.
    - ATLAS and CMS trigger requirements have become more compatible over the last year.
- 1TB/s readout with 7k short 1Gbits/s E-links and 1k 10Gbits/s optical conversion on service cylinder
- Serial powering for low mass 10 - 20kW power distribution.
  - R&D ongoing at chip and system level
- Good collaboration between CMS and ATLAS groups to face these challenges: RD53, readout, powering, sensors, ,
- Fortunately pixel detector is relatively small and will be last detector to be installed giving us some time to resolve the challenges.