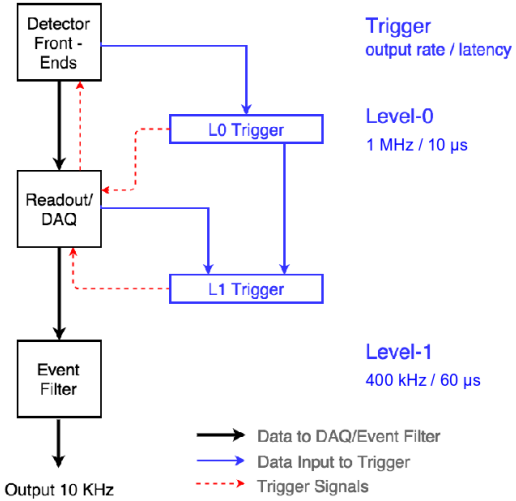
ATLAS Phase-II trigger upgrade

David Sankey on behalf of the ATLAS Collaboration

Thursday, 10 March 16



Overview

Setting the scene

Goals for Phase-II upgrades installed in LS3

- HL-LHC Run 4 and on

Run 3 Phase-I system

High level overview of the two proposed trigger architectures

Two hardware trigger level architecture

- Level-0, Level-1 then Event Filter

Single hardware level architecture

- Level-0 straight into Event Filter

Description of trigger levels in both architectures

Level-0

Level-1

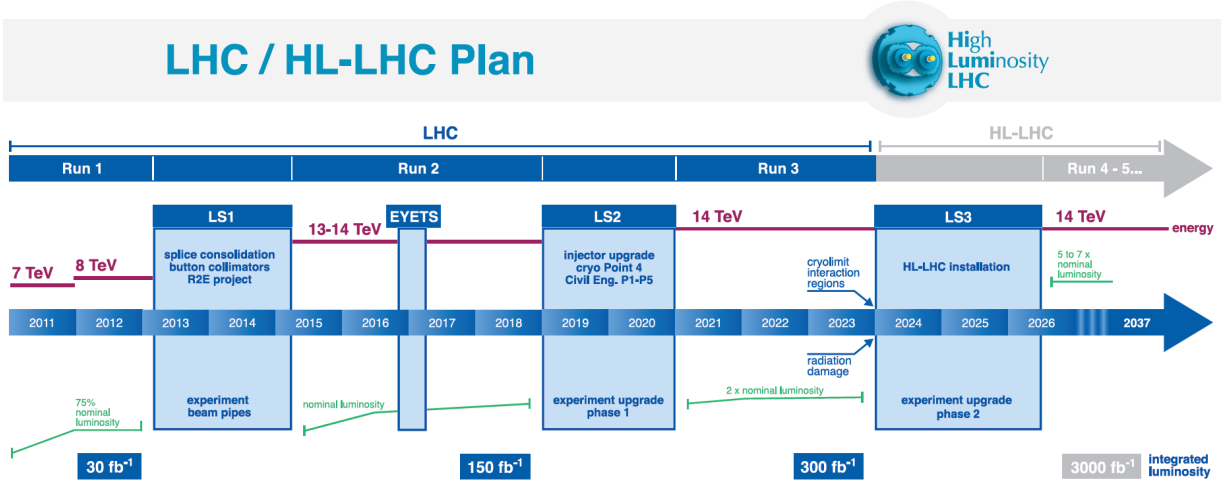
Readout

Dataflow

Event Filter

Summary

ATLAS Phase-II upgrades in LS3 for HL-LHC Run 4



Already described in talks earlier this week

- Track trigger
- Inner Tracker
- Calorimeters
- Muon spectrometer

The subject of this talk

- Trigger and data acquisition

ATLAS trigger goals for HL-LHC

Physics

Higgs boson studies require precision at electroweak scale

- Higgs Boson is light and requires triggers at the EW scale
- precision measurement of Higgs couplings a window into new physics (including much higher mass scales than the LHC)

BSM may require low cross section processes with large backgrounds, *e.g.* SUSY

- subtle BSM physics can only be found if SM is well understood – *Standard Model studies are essential*

European Strategy report (ECFA), P5 (DOE/NSF) conclude that HL-LHC needs $3000\ \mathrm{fb}^{-1}$

- 10 years at $\mathcal{L} = 7.5\times10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$
- high efficiency essential to avoid even longer running…

Trigger

Thresholds low enough to capture as much physics as possible

Trigger techniques as similar as possible to offline selection

- *e.g.* if analysis uses fat jet trigger, trigger should use fat jet trigger

Triggers should keep systematic errors to a minimum

- many Higgs measurements will be systematics limited

ATLAS Run 3 Phase-I trigger

Upgraded Level-1 trigger

- L1Calo with increased granularity:– low energy thresholds with improved isolation
- New Small Wheel Muon Endcap trigger:– suppress fake rates with new detectors

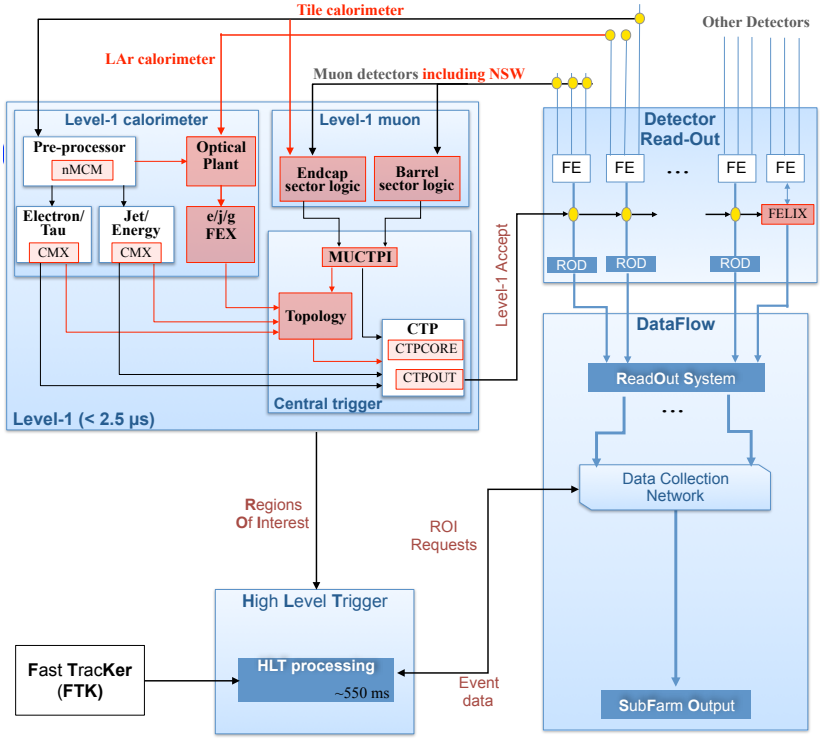
Upgraded Dataflow

- FELIX:– custom boards hosted on commodity PCs

Upgraded High Level Trigger

- multi-threading, seamless integration of offline algorithms
- Fast TracKer (FTK):– full event hardware tracking *evolving during Run 2*

Level-1 Accept rate 100 kHz, Event Filter output 1 kHz



Performance of Phase-I hardware trigger at Phase-II

Hardware trigger rates for desired physics come in at around 1 MHz

Target thresholds at or better than Run 1

- single electron 22 GeV, single muon 20 GeV, compared to 25 GeV in Run 1

Item	Run 1 Offline p_T Threshold [GeV]	Phase-I Level-1 system performance at $L = 7.5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ Offline Threshold for Phase-II Goal [GeV]	Level-1 Rate [kHz]
isolated Single e	25	22	200
single μ	25	20	40
di-γ	25	25	8
di-e	17	15	90
di-μ	12	11	10
$e-\mu$	17,6	17,12	8
single τ	100	150	20
di-τ	40,30	40,30	200
single jet	200	180	60
four-jet	55	75	50
E_T^{miss}	120	200	50
jet + E_T^{miss}	150,120	140,125	60

Many individual triggers in excess of the Phase-I overall Level-1 limit of 100 kHz

- single electron, di-τ

Setting thresholds to keep total rate to 100 kHz incompatible with physics aims

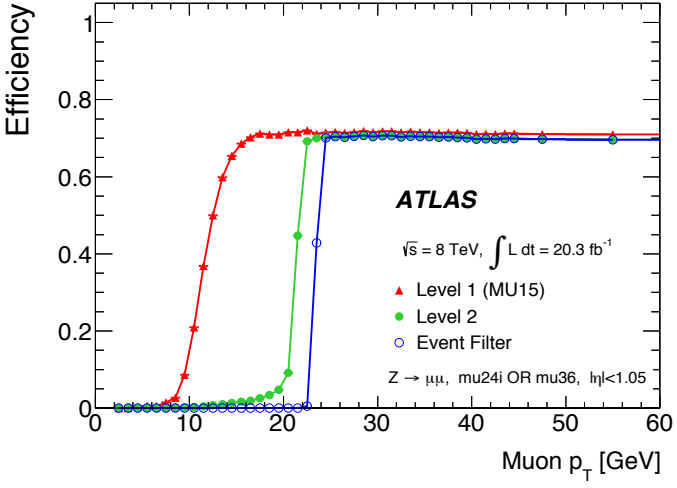
- for single leptons would imply 32 GeV electron and 40 GeV muon

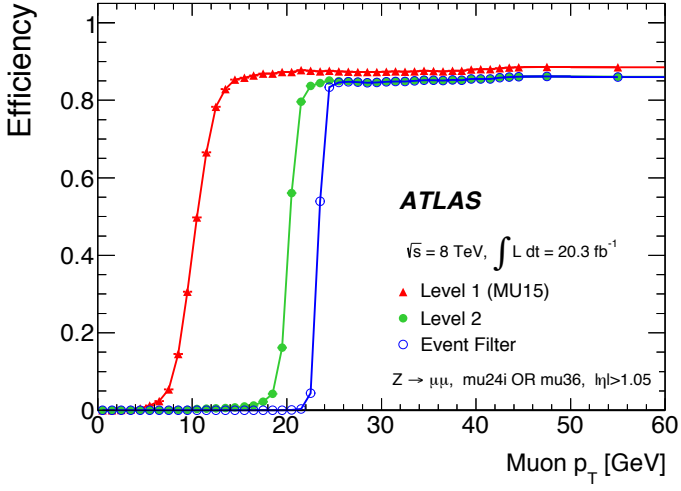
Hardware muon efficiency and acceptance

Muon barrel efficiency and acceptance are crucial trigger issues for ATLAS

Largely driven by geometrical acceptance

- purity cannot be relaxed because of high background rates





Without changes barrel efficiency likely to be worse due to trigger chamber aging

Redundancy added into hardware trigger

- in barrel add new muon trigger chambers and include precision muon detectors
- in forward region include precision muon detectors

Overview of the two proposed trigger architectures

Initial Level-0 hardware trigger

Reduced granularity input from calorimeters and muons, developed from Phase-I Level-1 trigger

Further hardware trigger including inner tracker

In two level system as part of Level-1 trigger

- prior to readout reducing readout rate

In single level system as part of Event Filter

- after readout providing fast reject

Both systems have regional tracking in hardware down to $p_{\mathrm{T}} > 4\,\mathrm{GeV}$ *at Level-0 Accept rate*

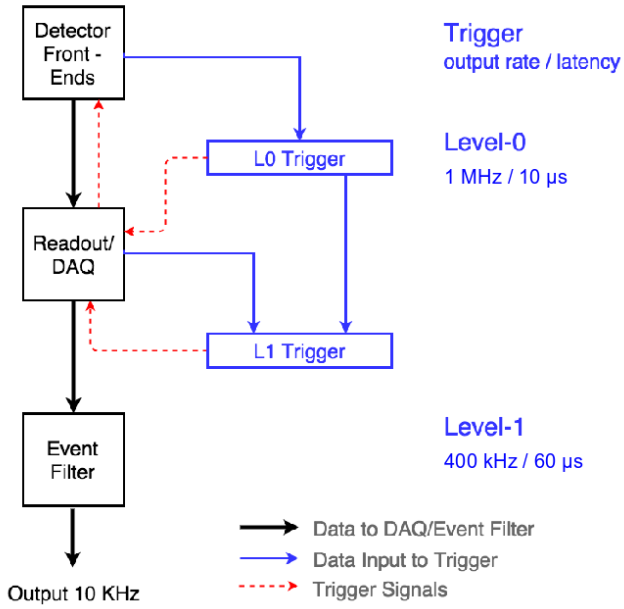
Readout/DAQ

Data Handler, Event Builder, Storage Handler

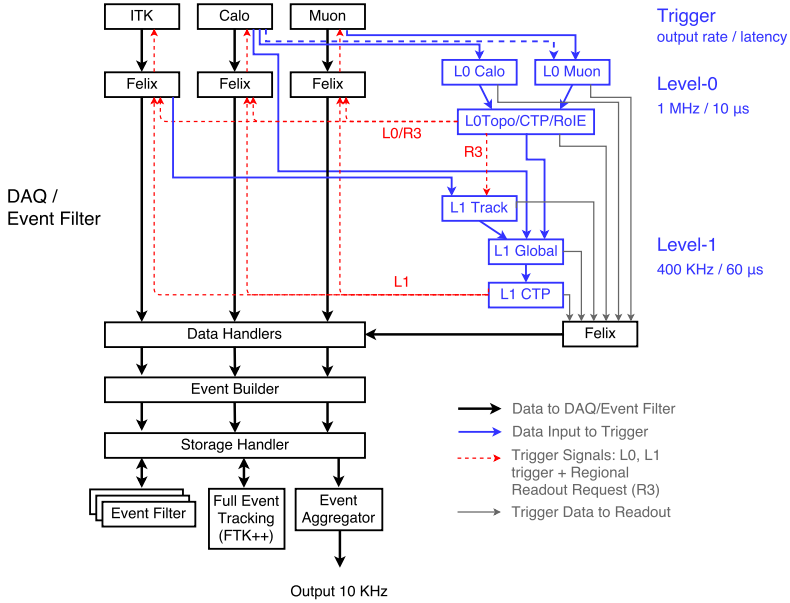
Event Filter

Phase-I framework taken further for Phase-II

Output to permanent storage via Event Aggregator



Two hardware level architecture



Two hardware trigger Levels:

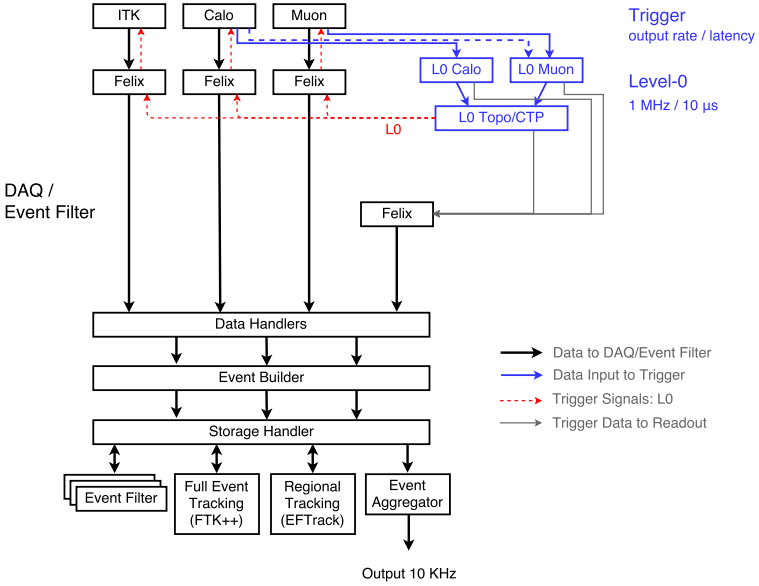
Level-0 1 MHz accept rate, trigger latency 6 μs, minimum detector latency 10 μs

Level-1 400 kHz accept rate, trigger latency 30 μs, minimum detector latency 60 μs

Event Filter delivers a factor 40 reduction down to output rate of 10 kHz

FTK++ full event tracking processor down to $p_{\mathrm{T}} > 1\,\mathrm{GeV}$ at 100 kHz

Single hardware level architecture



Single level hardware trigger straight into Data Handler

1 MHz accept rate, trigger latency near 6 μs, minimum detector latency around 10 μs

Event Filter now delivers a factor 100 reduction down to output rate of 10 kHz

Naively a factor 2.5 larger than in two level system, at least 10 times larger than Phase-I

- EFTrack regional tracking processor alongside FTK++ full event tracking

Expected trigger rates

Item	Offline p_{T} Threshold [GeV]	Offline $\lvert\eta\rvert$	L0 Rate [kHz]	L1 Rate [kHz]	EF Rate [kHz]
isolated single e	22	< 2.5	200	40	2.20
forward e	35	$2.4 - 4.0$	40	8	0.23
single γ	120	< 2.4	66	33	0.27
single μ	20	< 2.4	40	40	2.20
di-γ	25	< 2.4	8	4	0.18
di-e	15	< 2.5	90	10	0.08
di-μ	11	< 2.4	20	20	0.25
$e - \mu$	15	< 2.4	65	10	0.08
single τ	150	< 2.5	20	10	0.13
di-τ	40,30	< 2.5	200	30	0.08
single jet	180	< 3.2	60	30	0.60*
large-R jet	375	< 3.2	35	20	0.35*
four-jet	75	< 3.2	50	25	0.50*
H_{T}	500	< 3.2	60	30	0.60*
E_T^{miss}	200	< 4.9	50	25	0.50*
jet + E_T^{miss}	140,125	< 4.9	60	30	0.30*
forward jet**	180	3.2 - 4.9	30	15	0.30*
Total			$\sim$1000	$\sim$400	$\sim$10

Reduction in two hardware level system at Level-1 mainly using tracks from L1Track

Especially for electrons and taus

- *e.g.* single electron 200 kHz Level-0, 40 kHz Level-1, 2.2 kHz output
- also improvements from individual cell information for calorimeter at Level-1

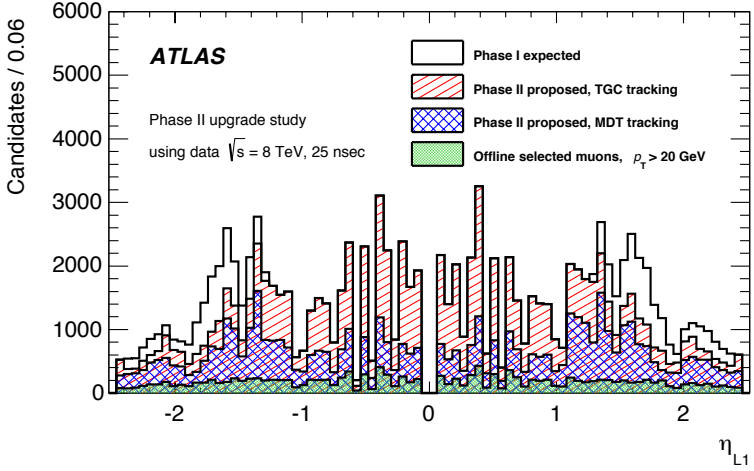
In single level system Level-0 rates feed directly into Event Filter

Level-0

L0Muon

Information from precision muon chambers (MDT) and additional muon trigger chambers added to significantly improve efficiency and purity

- building on existing muon trigger system and Phase-I NSW



L0Calo

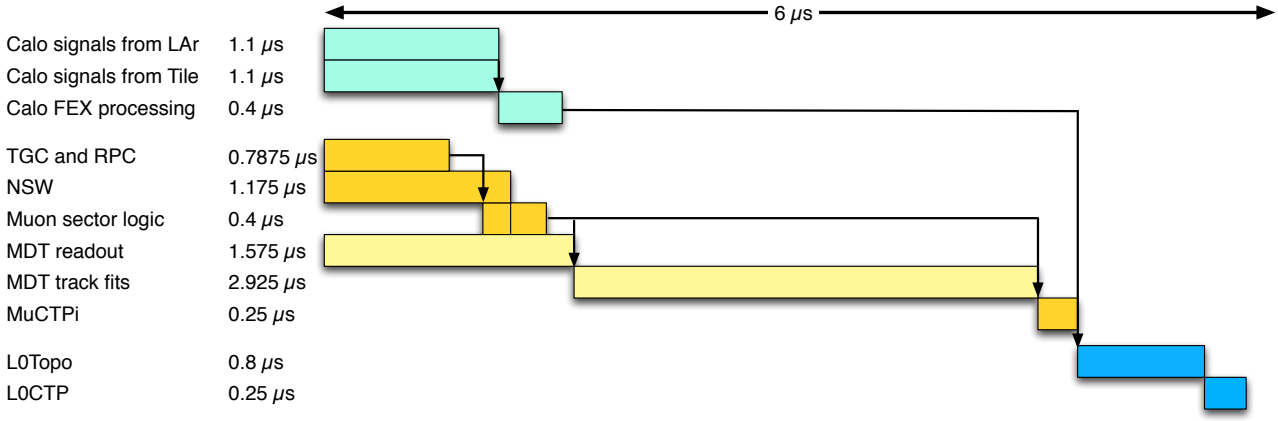
Hardware mostly from Phase-I Level-1 system

- Feature Extractors eFEX, gFEX, jFEX, with relaxed latency compared to Phase-I
- new digital signals from Tile and new forward calorimetry

Level-0

Phase-I systems take ~1.5 μs

MDT full readout in similar time, then track fits seeded by RPC, TGC and NSW



L0Topo topological processor

Phase-I hardware with additional processing time

- may be time-multiplexed

L0CTP central trigger processor

In two level system followed by RoI Engine

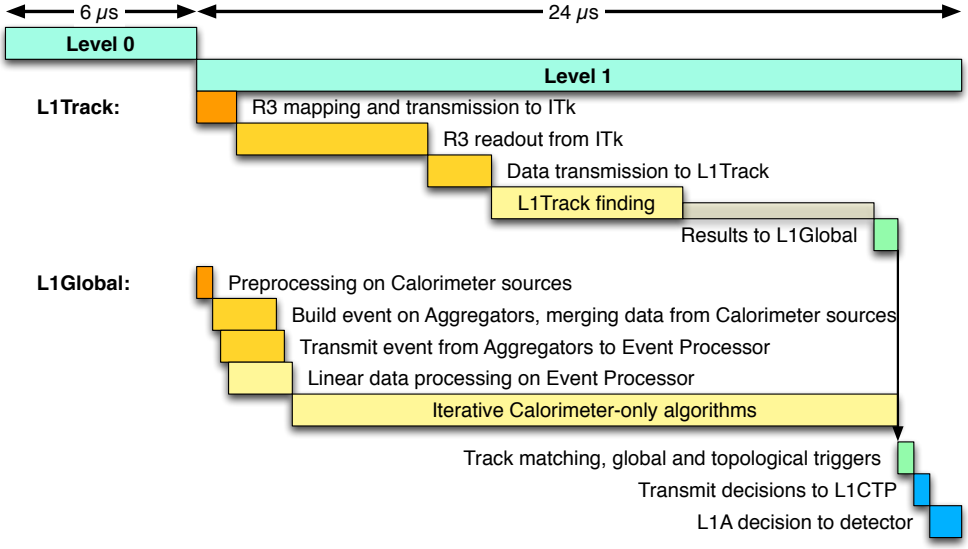
New system to send Regional Readout Requests (R3) to ITk for L1Track

Level-1 in two level system

L1Track

Regional track processor with variable latency

- up to 6 μs queue in L1Track



L1Global

Time multiplexed full calorimeter processor with fixed latency for linear data processing

- track matching, global and topological triggers as final step

Level-1 track trigger

Overview

Receives ITk data from regions around suitable RoIs contributing to Level-0 accept

- finds all tracks in those regions above 4 GeV momentum cut
- quasi-offline resolution, reconstruction efficiency at least 95% for offline tracks

Rejection factor of 5 for single lepton triggers, pileup track z_0 resolution < ~10 mm

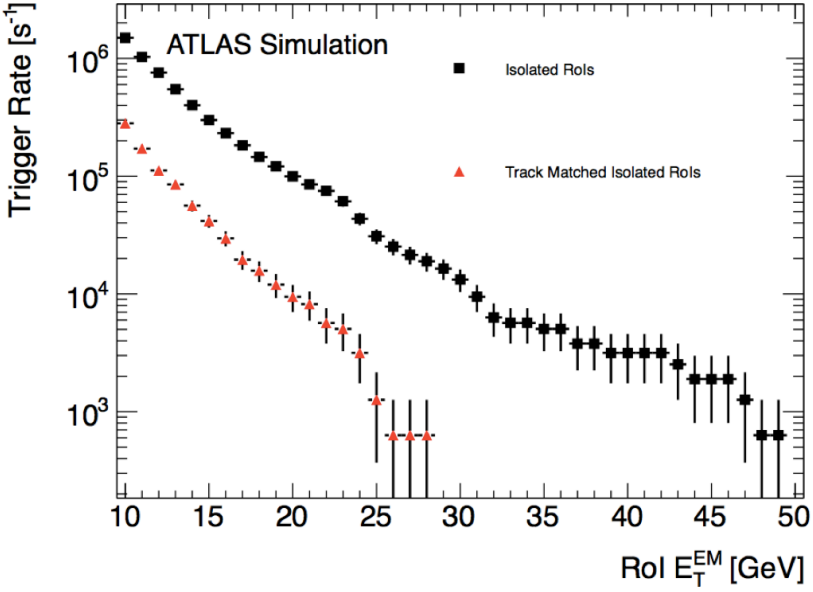
System requirements

Regional readout of 10% ITk in ~6 μs

- R3/Level-0 Accept prioritisation
- strip front-end readout chips with double-buffer capability
- full pixel readout at 1 MHz

FTK next generation associative memory chip and track-fit on FPGA

- 500k track patterns per AM chip at 200 MHz
- 4 fit/ns on modern FPGA



Level-1 global trigger

Overview

40 Event Processor time-multiplexed system, better than 0.1% dead time at 1 MHz

Receives

- calorimeter information from every cell
- L0Muon objects
- Level-1 tracks

Input up to 8 events in parallel each taking 2 μs to arrive

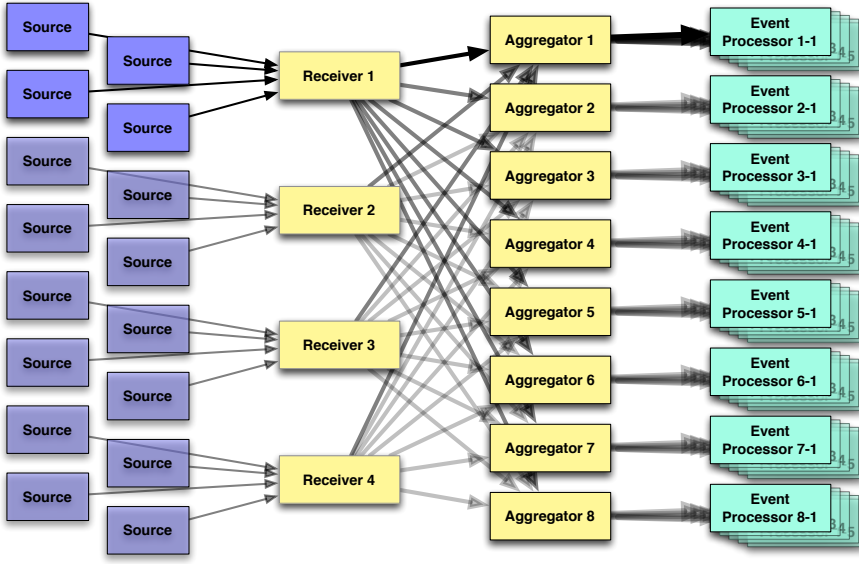
- linear processing of calorimeter data on arrival

Iterative processing for calorimeter jets and E_{T}^{miss}

- RoI processing for e, γ, τ

Global and topological selections

- tracks vital for taus and pileup suppression



Detector readout

FELIX

Router between serial/synchronous links (lpGBT and other lightweight protocols) and high level network links (40/100G Ethernet, InfiniBand)

Detector-agnostic encapsulating common functionality

- merges and/or splits data streams but leaves content untouched

Handles detector configuration and control of calibration procedures

- ensuring connectivity to detector (critical for DCS)

Low latency links to L1Track and L1Global

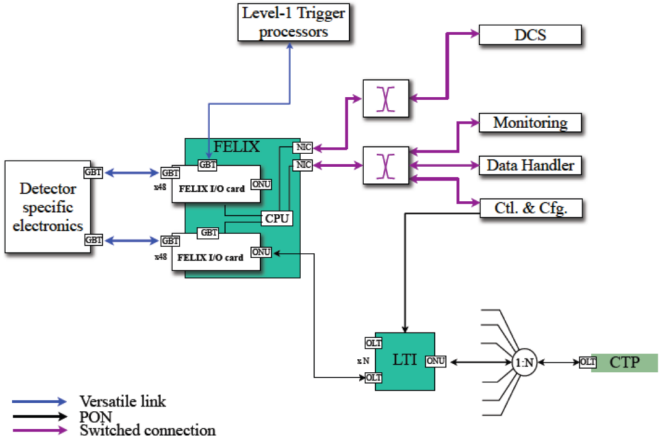
Interface to Phase-II TTC system via PON

Data Handler

Commodity PCs on network

- customized detector configuration, control and monitoring in backend software
- functionality currently in hardware

Enables flexible Event Building paradigms



Dataflow

Stores, transports, builds, aggregates and compresses event data

Raw event size ~5 MB, input rate 400 kHz in two hardware level system

Event Builder

Full event building at Level-1 rate

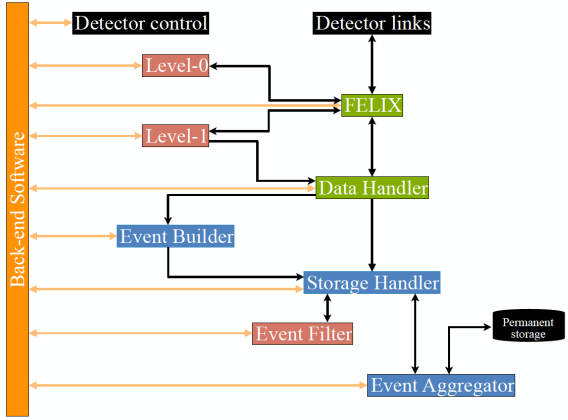
- physical or logical

Storage Handler

Decouples Dataflow and Event Filter

- stores data during LHC fill, Event Filter continues processing in inter-fill gap

Event Aggregator



Event aggregation, metadata bookkeeping, data compression at output rate of 10 kHz

Storage Handler the biggest challenge in single level system

Still a big challenge in two level system…

Issue is I/O rather than data volume

- sustained 5 TB/s for uncompressed write of 5 MB per event at 1 MHz
- today typically ~1 Gb/s sustained write performance per drive ⇒ *~50000 drives*

Event Filter

New framework from Phase-I taken further for Phase-II

Increase in farm size driven by

- input rate increasing from 100 to 400 kHz
- increase in execution times with pile-up
  – *reconstruction algorithms rely increasingly on tracking to mitigate pile-up*
- more offline-like selections to provide rejection (greater use of full-scan)

Partially mitigated by

- hardware-based full-event tracking used for selected triggers (~100 kHz) to identify primary vertices to suppress the effects of pile-up
- extensions and improvements in the software Framework introduced in Phase-I
  – *multi-threading, seamless integration of offline algorithms*
- speed up of algorithms, possibly exploiting accelerators
  – *General Purpose Graphics Processor Units (GPGPU) or FPGA*

Computing moving towards many-core and heterogeneous architectures

In single hardware level architecture requires accelerated regional track processing

EFTrack regional tracking along lines of L1Track

But software equivalent of L1Global – case for separate calorimeter hardware not clear

Hardware extensions to Event Filter

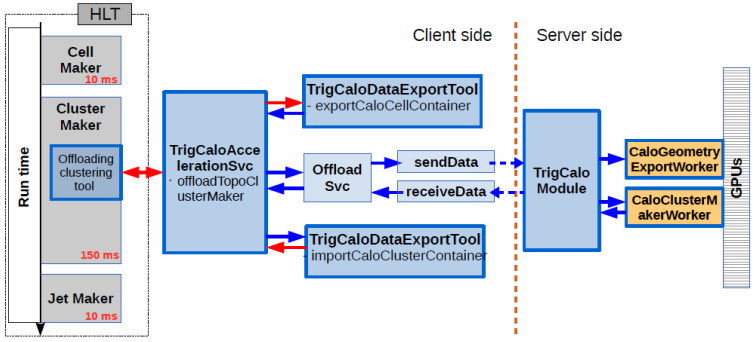
Rather than simply increasing Event Filter CPU size use specialised hardware

Particularly for self-contained tasks amenable to parallelisation

Exploit GPGPU or FPGA acceleration for tracking and calorimeter processing

Acceleration at point of use

- driven by trigger algorithms



Very strong case for separate hardware track finders

Offload time consuming computation onto specialised highly parallel hardware

- EFTrack giving $p_{\mathrm{T}} > 4\ \mathrm{GeV}$ "regional tracking" input to Event Filter at up to 1 MHz in single level architecture (primarily for electrons)
- FTK++ giving $p_{\mathrm{T}} > 1\ \mathrm{GeV}$ "full event tracking" at 100 kHz in both architectures

Tracks then refined in Event Filter to improve track-parameter resolution

- maximize efficiency and rejection power

Further study into optimisation of CPU and mix of hardware accelerators

Cost-benefit analysis of hardware acceleration on trigger decision

Summary

Higgs, BSM and SM physics all benefit from low thresholds

Run 1 thresholds for leptons are essential

Phase-I trigger provides basis for Phase-II system

In particular Phase-I hardware trigger core of Level-0

- but with significant improvements for muons
- *Level-0 trigger rate rises from 100 kHz to 1 MHz*

Track information from inner tracker crucial in subsequent levels

Factor 5 reduction in single lepton triggers, also vital for taus and pileup suppression

Regional tracking in either second hardware level or as coprocessor to Event Filter

Storage Handler decouples Event Filter from real-time data flow

Event Filter continues processing in gap between LHC fills

Event Filter a heterogeneous system

Mix of CPU, GPGPU/FPGA and fully custom tracking hardware

- FTK++ providing full tracking at 100 kHz
- regional tracking at 1 MHz in single hardware level system

Decision to be made between single and two level architectures this Summer

History of the two hardware architectures

Spring 2012

Two hardware level architecture first proposed

- Level-0 rate 500 kHz, Level-1 200 kHz into Event Filter
- *allows for legacy muon electronics*
- system described in Phase-II Upgrade Letter of Intent in December 2012

Spring 2014

Trigger rates updated to allow more bandwidth for taus and hadrons at Level-0

- Level-0 rate 1 MHz, Level-1 400 kHz into Event Filter
- *uncertain in case of legacy MDT electronics*

Autumn 2014

LHC raises target luminosity from $\mathcal{L} = 5{\times}10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ to $7.5{\times}10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$

- basis for trigger in Phase-II Upgrade Scoping Document, September 2015

Autumn 2015

ATLAS considers Level-0 only scheme

- all legacy muon electronics replaced, Level-0 rate 1 MHz into Event Filter

Hardware trigger parameter motivation

Level-0 latency

6 μs for trigger decision at trigger output allows extra information and computation

- MDT added to muon trigger, more time for processing in calorimeter trigger

10 μs at output to detectors basis for design of Phase-I ASICs

- *also not feasible to significantly increase this for inner tracker Phase-II ASICs*

Level-0 rate

Motivated by menu estimates

- included in Phase-I NSW and L1Calo design

Level-1 latency

30 μs trigger latency dictated by legacy electronics

- 60 μs total latency for new systems to give headroom

Level-1 rate

NSW readout targets 400 kHz as proposed for Phase-II reference design

- legacy MDT sets limit at 200 kHz