SMU

Fermilab

Versatile Link PLUS

Csaba SOOS
EP-ESE-BE

on behalf of the VL+ collaboration

Outline

- Versatile Link PLUS project introduction
  - Key differences between VL and VL+
- Link architecture
  - New front-end variants supporting e.g. multi-channel readout
- Link components
  - Back-end
  - Passives
  - Front-end module
    - Requirements, challenges
    - Optical components
    - ASICs
    - Packaging options
  - System
- Summary

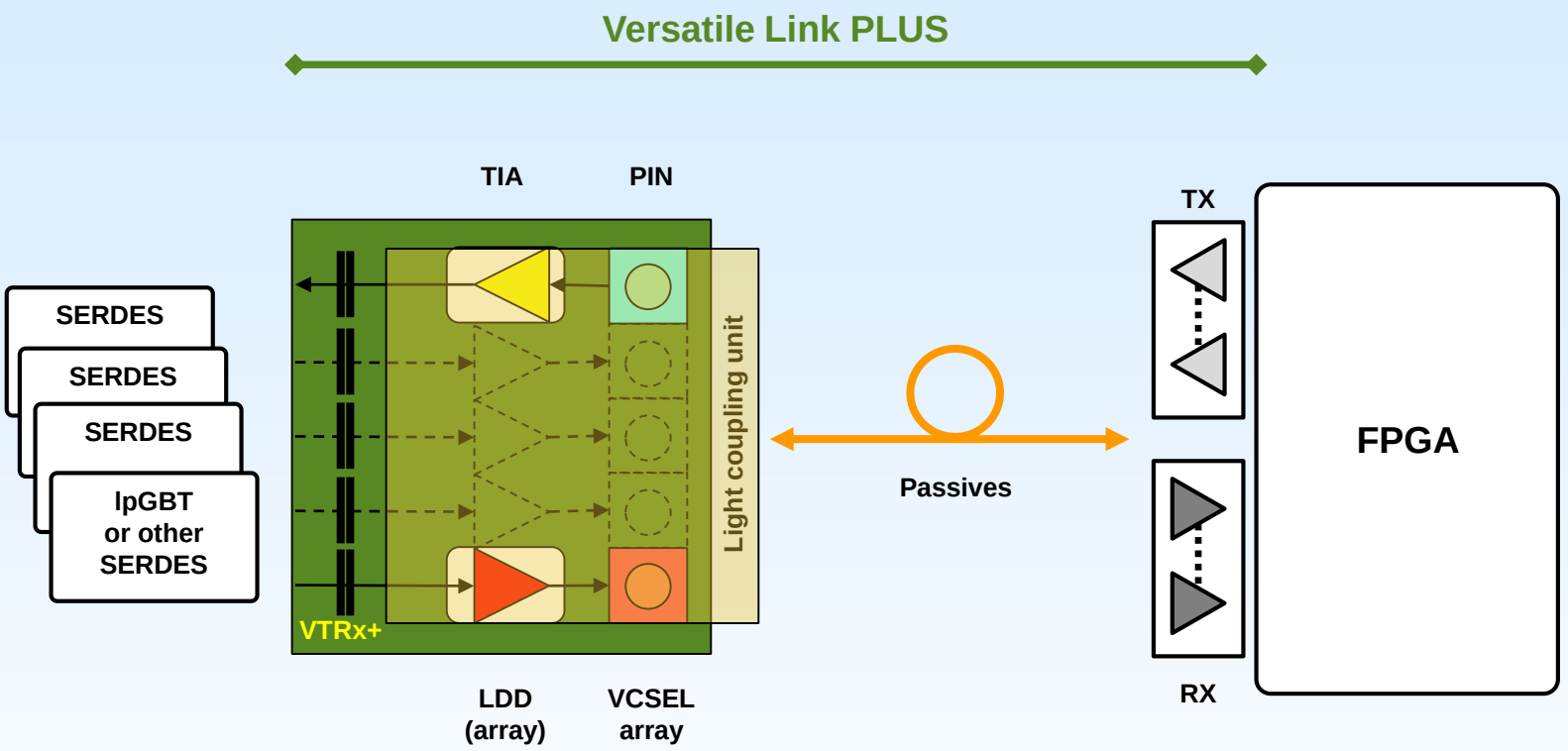
Introduction to Versatile Link PLUS

- The Versatile Link PLUS project (VL+) targets the phase II upgrades of the ATLAS and CMS experiments
- VL+ was officially announced at ACES 2014 and started on 1 Apr 2014. It is subdivided in three phases of 18 months each:
  - Phase 1: proof of concept (Apr 2014 – Oct 2015)
  - Phase 2: feasibility demonstration (Oct 2015 – Apr 2017)
  - Phase 3: pre-production readiness (Apr 2017 – Oct 2018)
- Collaboration between CERN, FNAL, Oxford, and SMU

	Versatile Link	Versatile Link PLUS
Optical mode	Single- and multi-mode	Multi-mode
Flavours	1Tx+1Rx, 2Tx	Configurable at build time up to nTx(+1Rx)
Radiation level	Calorimeter grade	Tracker grade
Form factor	SFP+	Custom miniature
Data rate	Tx/Rx: 5 Gb/s	Tx: 5/10 Gb/s, Rx: 2.5 Gb/s

Table : Key differences between VL and VL+

Versatile Link PLUS architecture

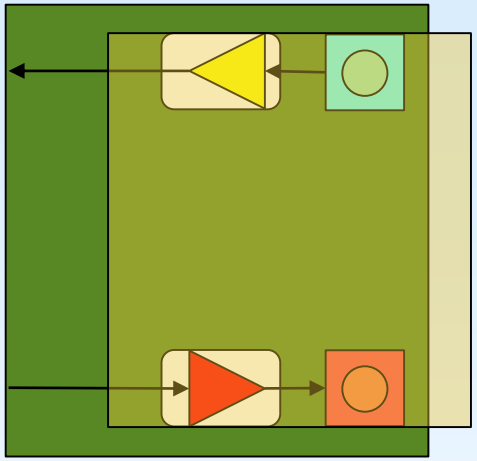


On-Detector
Custom Electronics & Packaging
Radiation Hard

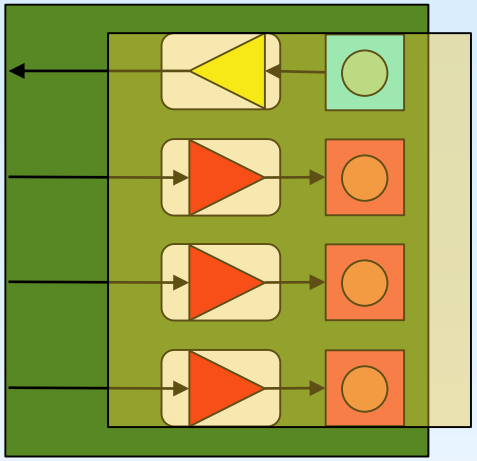
Off-Detector
Commercial Off-The-Shelf (COTS)
Custom Protocol

VL+ front-end module variants

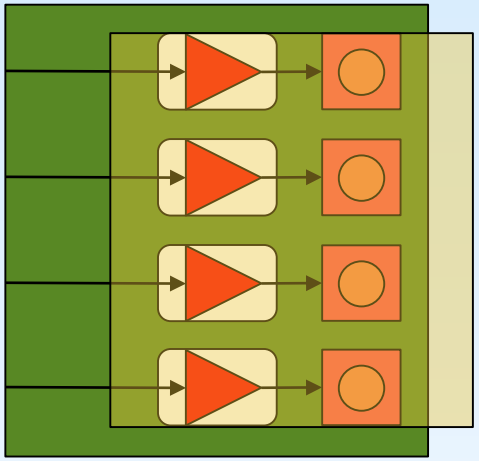
Discrete-based derived from:
- **Light peak**
- **USB-3**
- **Thunderbolt**



1 TX + 1 RX

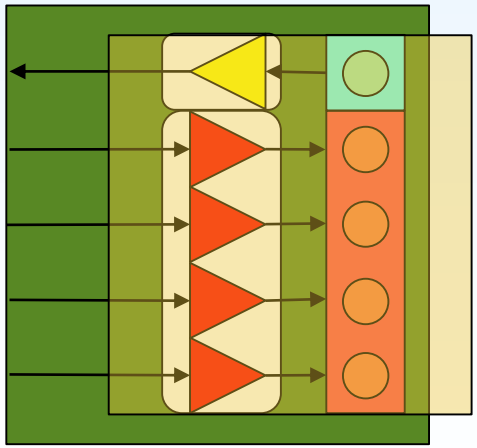


3 TX (single channel LDDs) + 1 RX

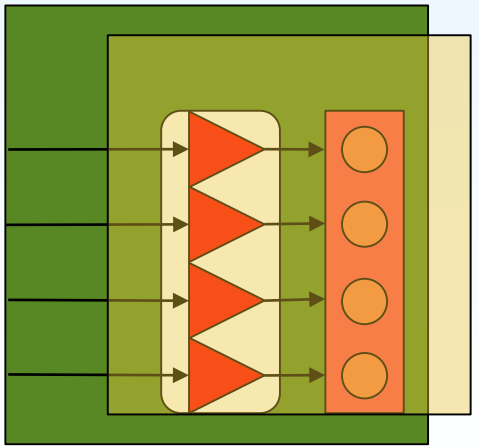


4 TX (single channel LDDs)

Array-based derived from:
- **QSFP+ engine**

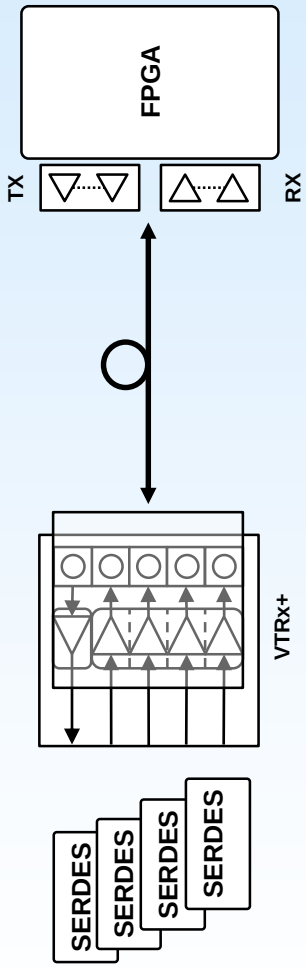


1/3/4 TX (using LDD array) + 1 RX



4/8 TX (using LDD arrays)

Link components



Back-end: FNAL

Passives: CERN

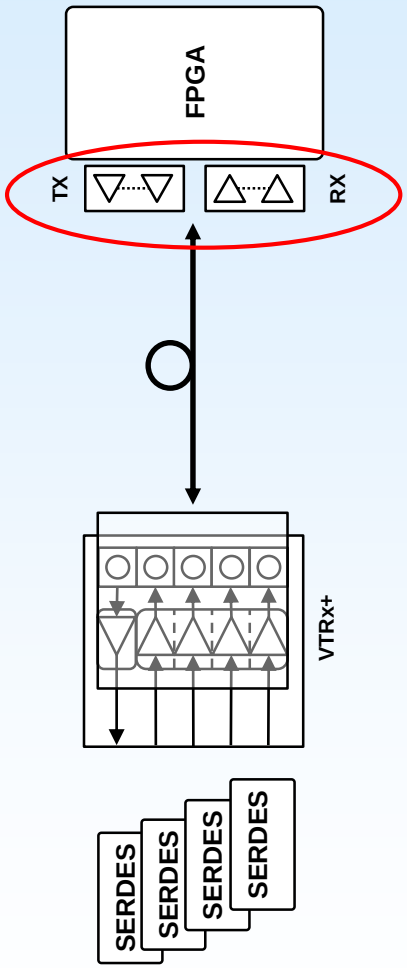
System: FNAL

Module & Components: CERN

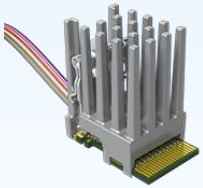
ASICs: SMU (EE & PHYS)

Reliability: Oxford

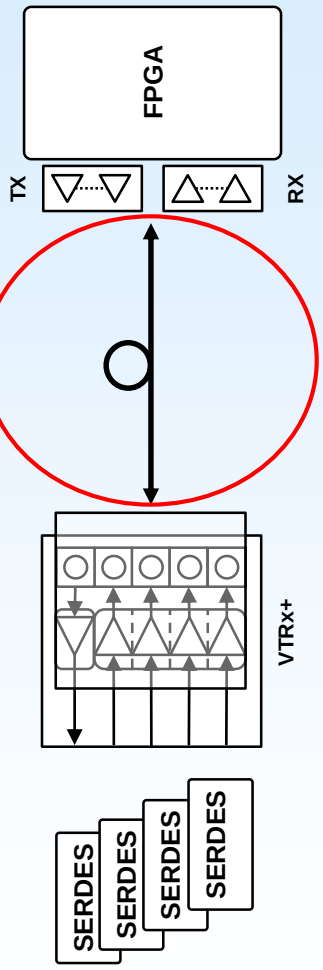
I. Back-end (FNAL)

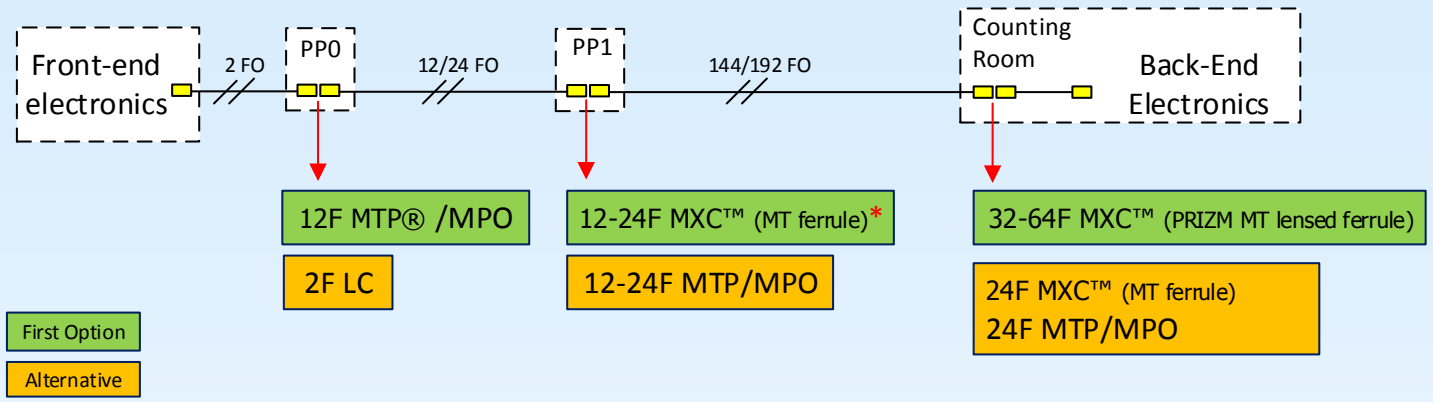


- Identify commercial back-end components compatible with the VL+ system
  - Continuous survey, selection and evaluation process
  - Recommend compatible parts to users
- Specifications for back-end Tx, Rx and TRx
- Shortlist components in two categories
  - Mid-board and board-edge
- Define test procedures and test benches
- Modules already tested
  - Samtec FireFly
  - Avago Mini/MicroPod
  - FCI Leap



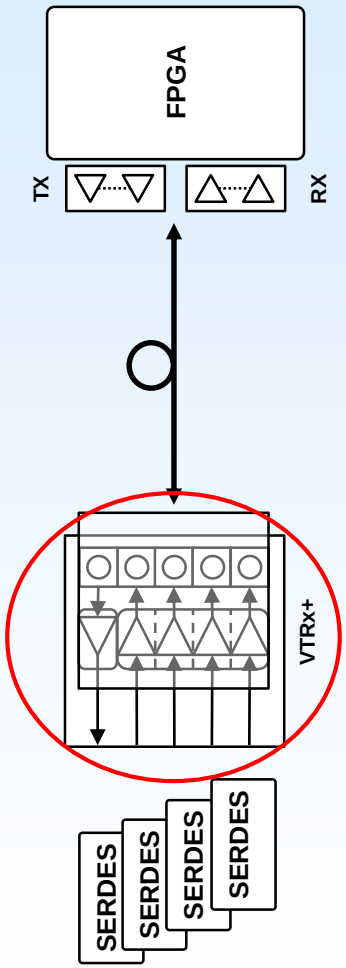
II. Passives (CERN)



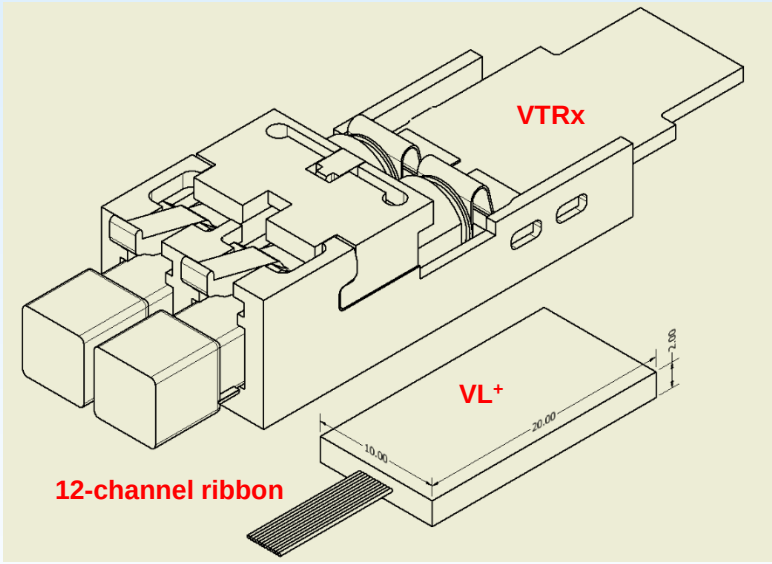


- Define cabling plant to meet specific HL-LHC requirements
  - High radiation dose over a short distance in a cold environment
- Investigate cabling *options* outside the sub-detectors
  - Trunk cabling: higher density and moderate ruggedness
  - Investigate connector solutions used in the industry (MTP, MXC, …)
- Calculate the impact of the radiation inside the detector
  - RIA, bandwidth, …
- Irradiation tests for front-end cabling plant
  - 1 MGy, room temperature and cold (-55C)

III. VL+ front-end module (CERN)

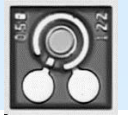


- Versatile
  - Up to 4Tx + up to 1 Rx, configurable at build time or by masking channels
  - 4Tx + 4Tx may become feasible (TBD)
- MM only
  - 850 nm VCSEL
  - InGaAs PIN (TBC)
- Miniaturized
  - Target dimensions 20 x 10 x 2 mm
- Pluggable
  - Either optical or electrical (or both) connector
- Data-rate:
  - Tx: up to 10 Gb/s
  - Rx: up to 5 Gb/s
- Environment
  - Temperature: -35 to + 60 °C
  - Radiation (based on Tracker requirements, TBD)
    - Total Dose: 1 MGy qualification (investigations up to 2 MGy)
    - Total Fluence: 2×10^{15} n/cm^2 and 1×10^{15} hadrons/cm^2



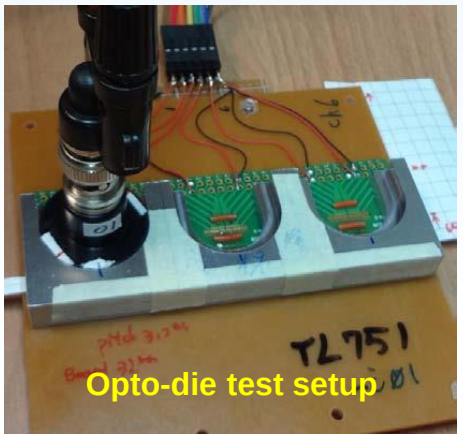
IV. Opto-die (CERN) and reliability (Oxford)

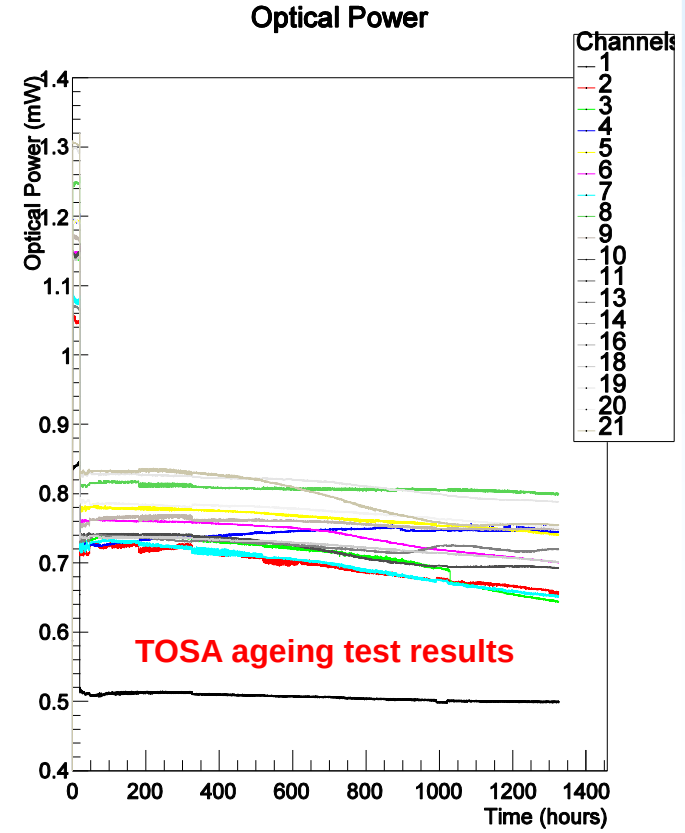
- Identify and test VCSEL and Photodiode chips (CERN)
  - Single PIN, single VCSEL, and VCSEL array
- Temperature tests (CERN)
  - VCSEL may have to be modified/optimized for cold
- Irradiation tests (CERN)
  - TID and total fluence
  - VCSELs, InGaAs and GaAs PIN diodes have been tested in Dec. 2015
- Reliability tests (Oxford and Academia Sinica)
  - 85C/85% RH
  - TOSA ageing tests
  - Opto-die testing



PIN

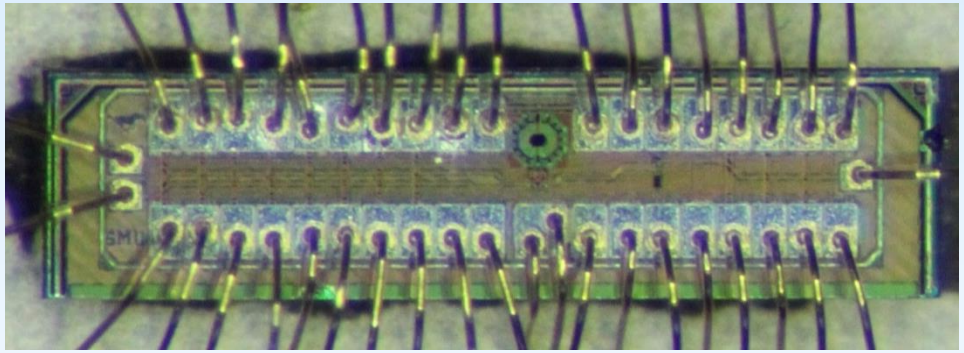
VCSEL array



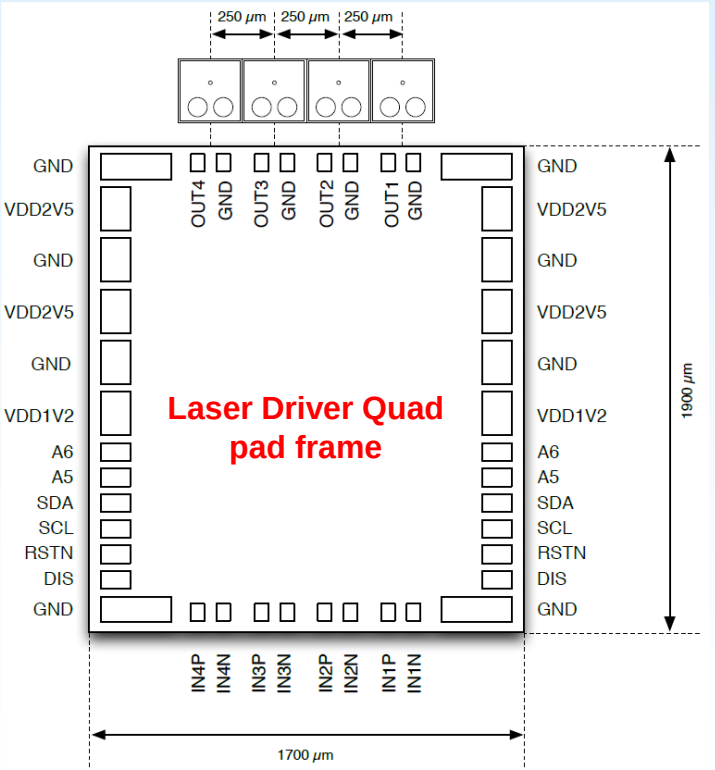


V. ASICs (SMU)

- Single-channel laser driver (see Paulo's talk)
  - Tested electrically at 10Gb/s



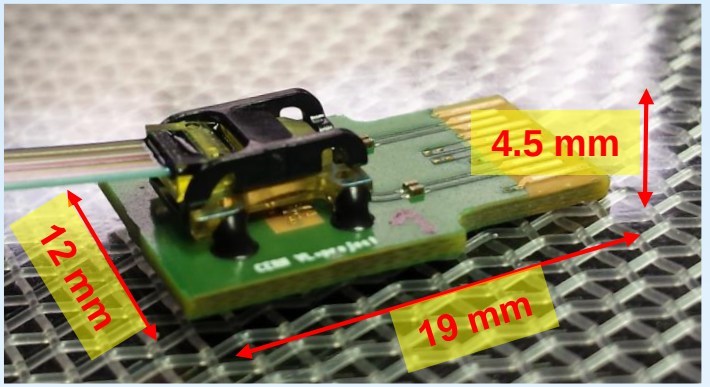
- 4-channel laser driver
  - 3 designs have been submitted
  - Expected in April-May

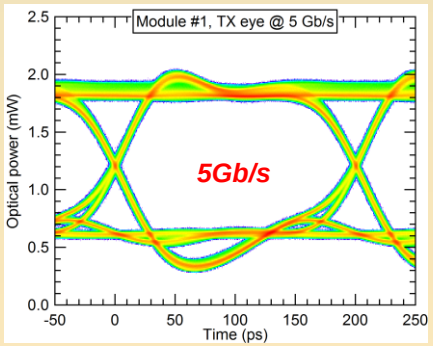


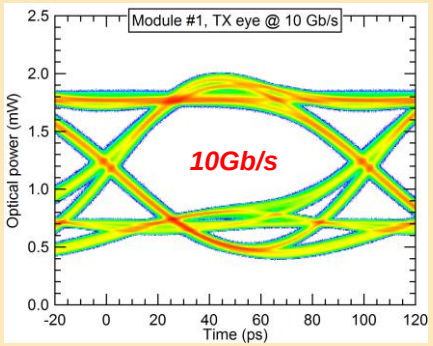
- Current GBTIA design meets the specs
  - Redesign is not planned for the time being

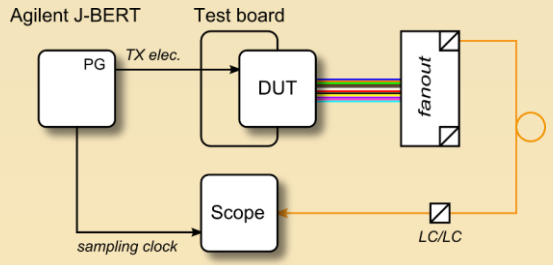
VI. Packaging (CERN) – Option 1

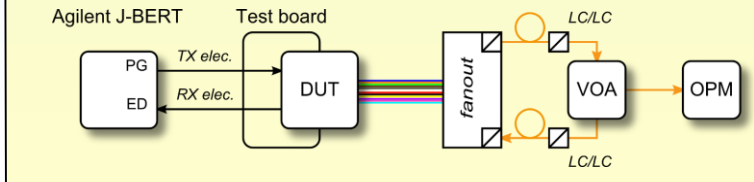
- In-house design and development of full custom module
- First iteration was successful with commercial ASIC
- New version with new ASICs and a low profile coupling block has been launched

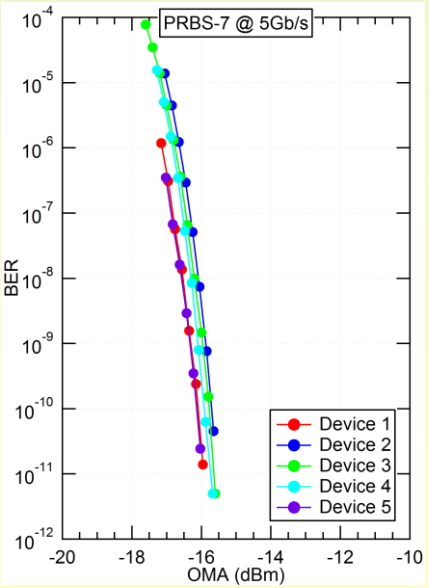












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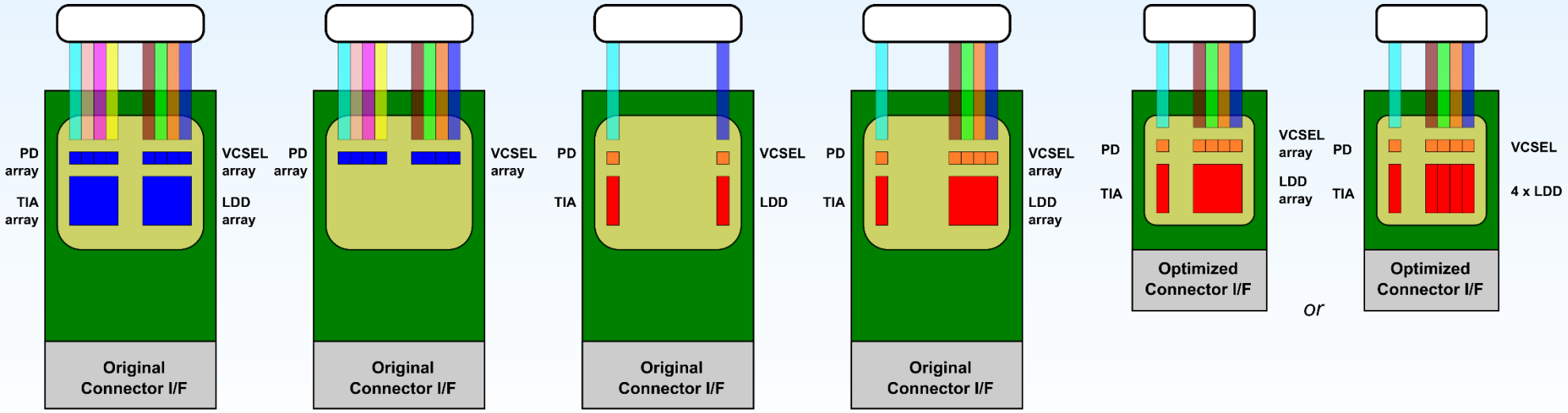
VI. Packaging (CERN) – Option 2

- Work with vendors on the customization of their existing commercial modules in a framework compatible with CERN purchasing rules
- Keep competition until late stage, but also allow some selection as development progresses
- First contact has been established, and market survey procedure is being launched



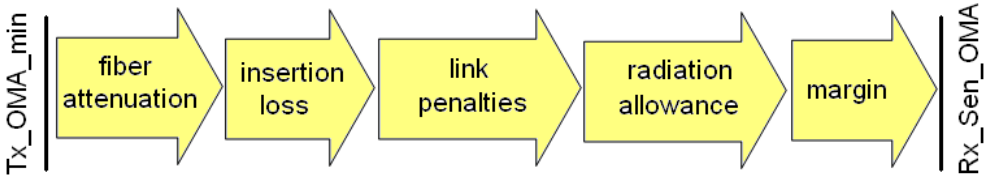
- *Original*
- *Commercial, qualified by CERN*
- *Custom, designed by CERN*

Proposed customizations steps

VII. System (FNAL)

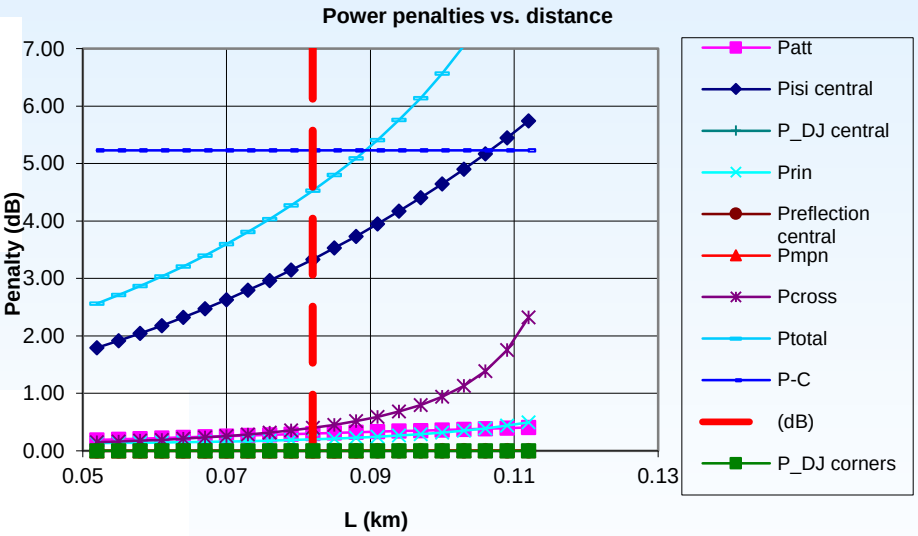
- Update system specifications
- Develop system test framework
- Verify VL+ links using system test stand demonstrator

Power budget based on aggregate effects and penalties



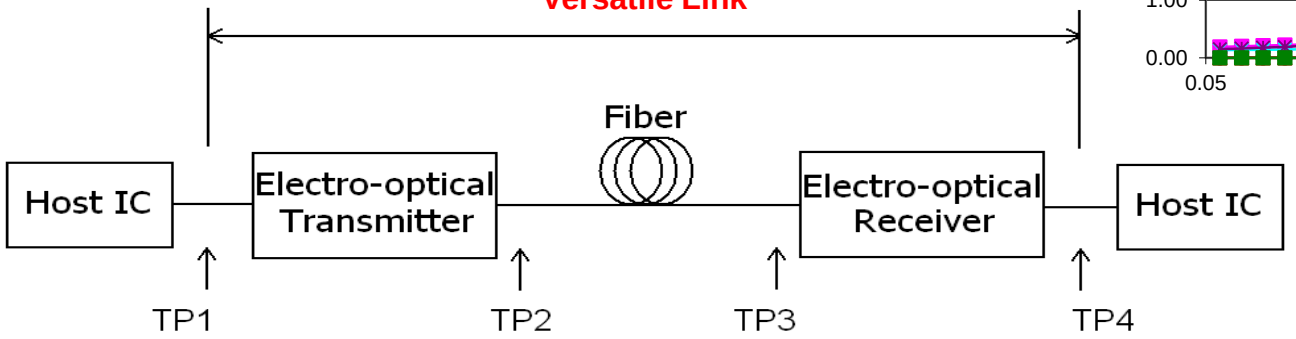
D. Gong, et. al "Link Model Simulation and Power Penalty Specification of the Versatile Link Systems",

Power budget modelling



IEEE P802.3ae 10Gb/s Ethernet Task Force power budget modelling spreadsheet

Versatile Link+



derived from the Versatile Link system specifications

Summary

- Versatile Link PLUS project successfully completed first project phase
  - We demonstrated concept of miniature, integrated, multi-channel fibre optic link for experiment readout and control
- Back-end
  - Candidate components are being tested
- Passives
  - Optical cable and connector candidates have been identified
  - Fibres have been irradiated in cold
- Front-end module
  - Sample VTRx+ made available to first user
  - Damp-heat testing of modules will start soon
  - Several ASICs are in the pipeline
  - Further developments are ongoing with commercial partners to benefit early from industrialization
  - Level of customization will be strongly influenced by final quantities
- Feasibility demo will take place by Q2/2017
- Target production starting in 2019