Phase-I ATLAS trigger upgrade

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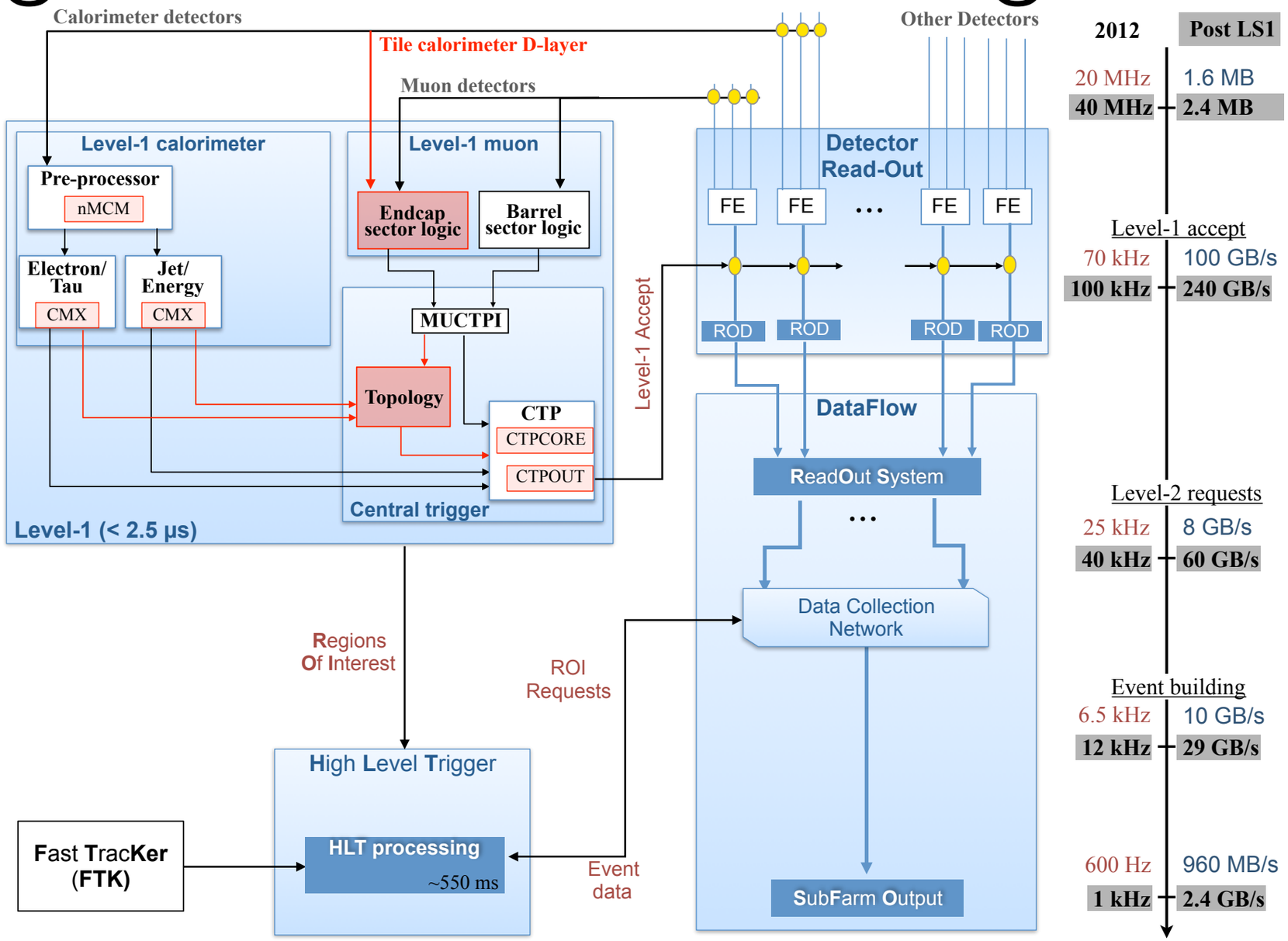
ATLAS Trigger and DAQ challenges

Run2 system:

- new L1CALO pre-processor and interface to Central trigger.
- new muon chambers and Tile calorimeter input to endcap L1MUON.
- Central Trigger with new Topology Trigger and Central Trigger Processor modules.
- initial deployment of Fast Tracker (FTK) in HLT

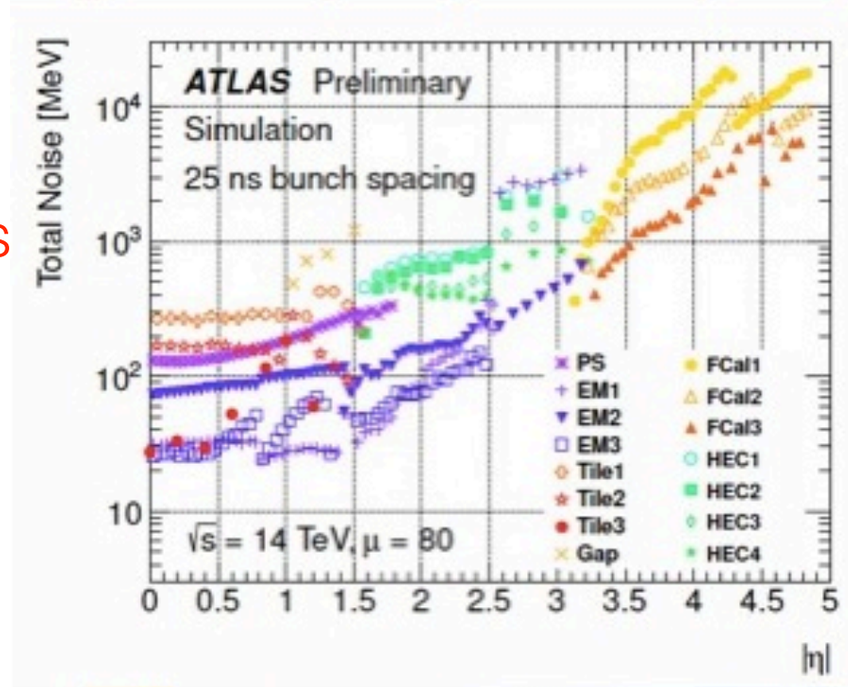


In Phase-I, ATLAS TDAQ system will face event rates and pile-up levels much higher than the original design values. Trigger will adapt to this new environment by:

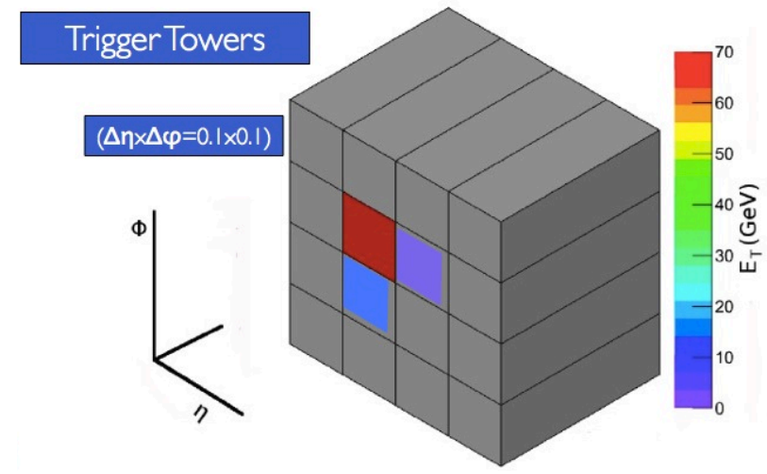
- having a powerful L1Calo using increased granularity to achieve better isolation
- keeping low energy thresholds, most useful to do physics with electro-weak scale particles;
- the Muon Endcap Trigger will suppress fake rate using New Small Wheel detectors;

LAr and L1Calo in Phase-I

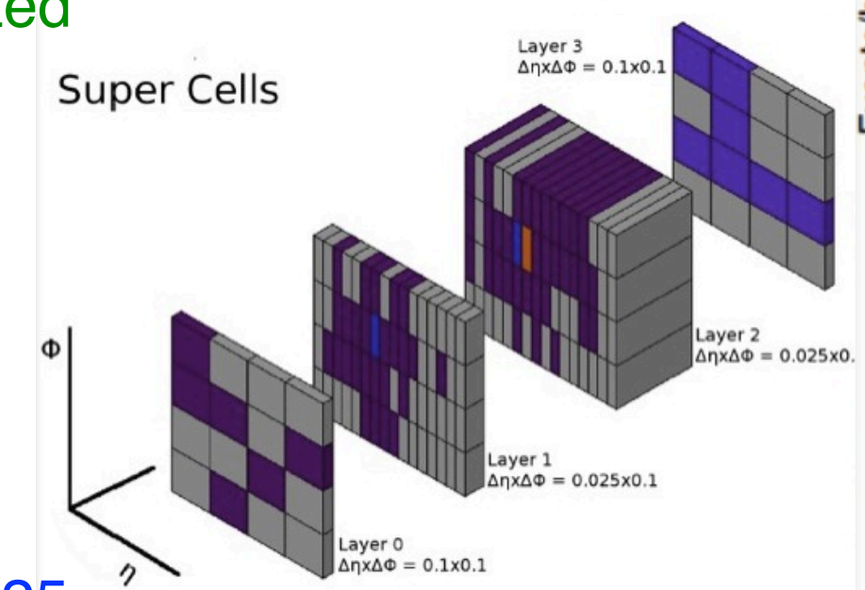
- Inclusive rates of current EM triggers expected to grow linearly with luminosity. Rates from di-EM increase due to accidentals from minimum bias events:
  - 270 KHz total (EM18VH, EM30, 2EM10)
- Clustering and isolation is degraded by large granularity in eta-phi (0.1X0.1) and limited resolution (E_T: 1GeV/count).
- Large improvements expected by:
  - higher granularity in eta 0.025
  - segmentation in depth
  - higher resolution (E_T: 0.125 GeV/count)



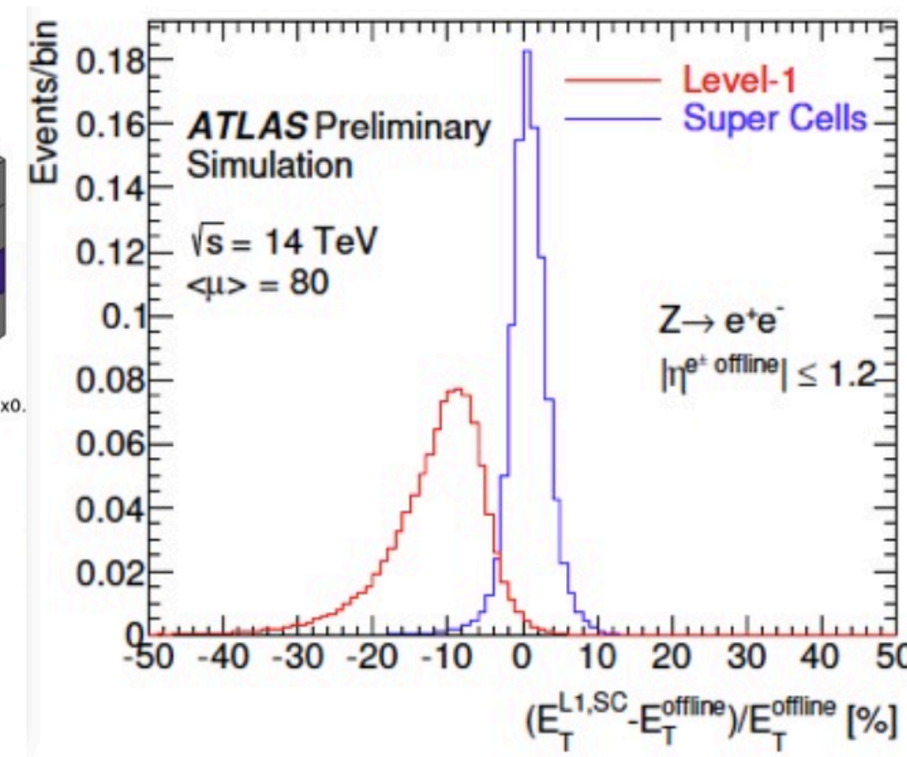
total noise on different calo cells, μ=80



Run2: LAr EM clusters and isolation regions



Phase-I: LAr Supercells

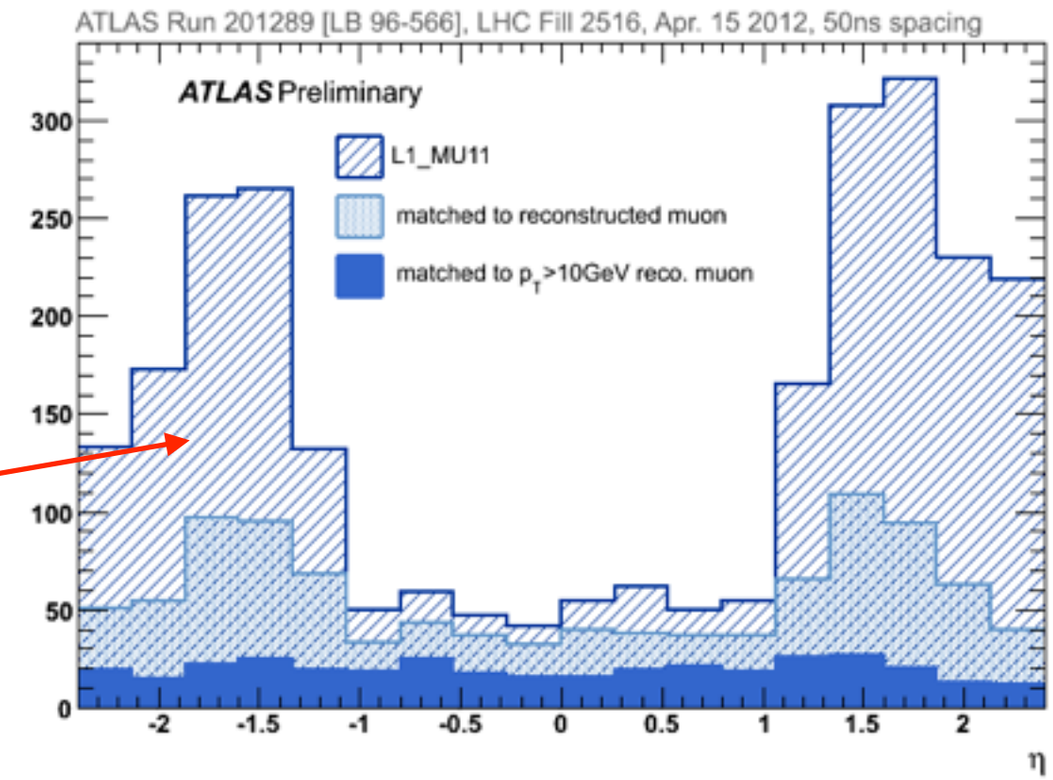


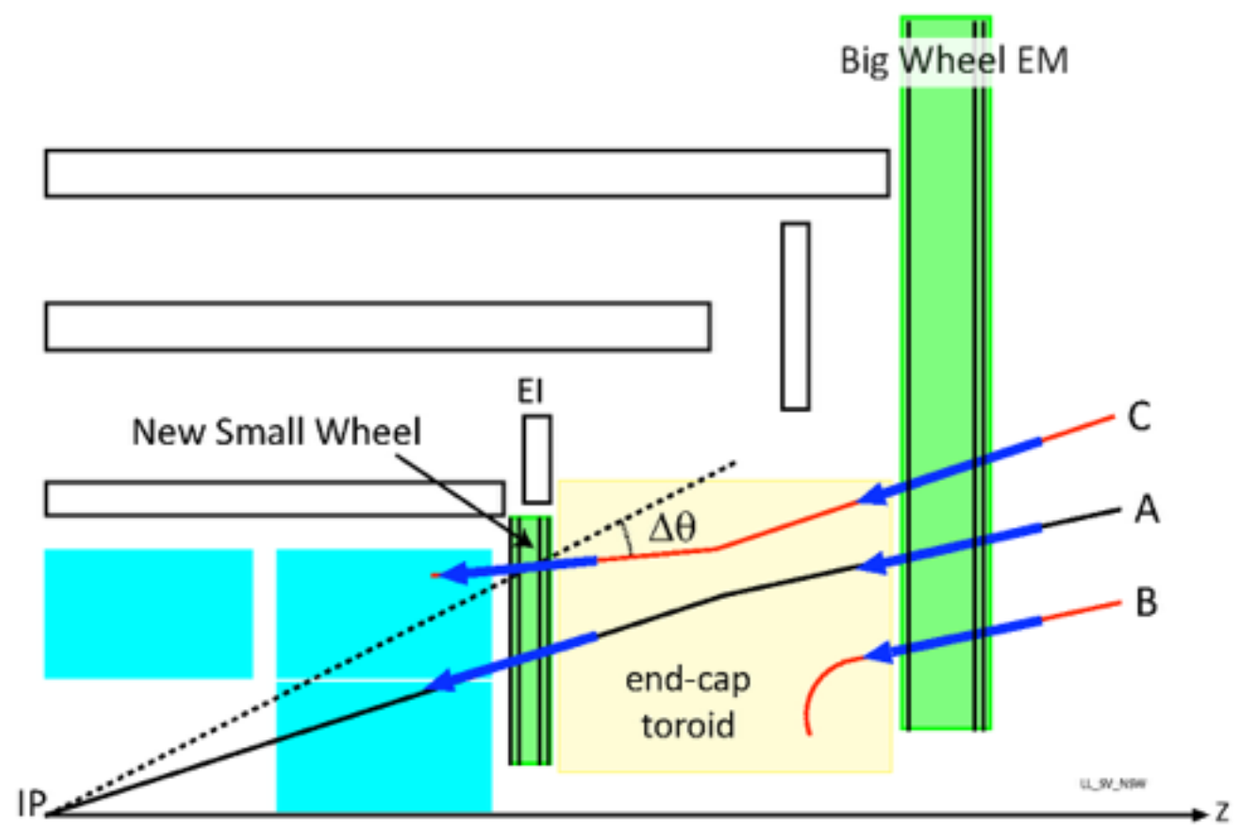
Expected Improvement respect to Run2 system, μ=80

New Small Wheels in Phase-I

(see J. Zhu presentation, "*ATLAS New Small Wheels*")

- Fake L1 muon trigger rate
  - In the present Muon System, triggering on high-pt muons relies on information of the Big Wheels.
  - **Endcap Muon Fake rate is almost 90%**
  - As a consequence muon pt-threshold would have to be increased drastically above 1-2·10^{34} to keep trigger rate under control and within availability budget (~ 20 KHz)
- **NSW principle**
  - **Rejection of tracks not from the IP:**
    - B: creation within the toroid
    - C: multiple scattering
  - **Matching of angle θ between BW and NSW tracks**
  - Angular resolution of 1 mrad (trigger)
    - after phase-2 BW upgrade
    - Until LS3: NSW confirmation of BW tracks, angular cut of +- 7 mrad

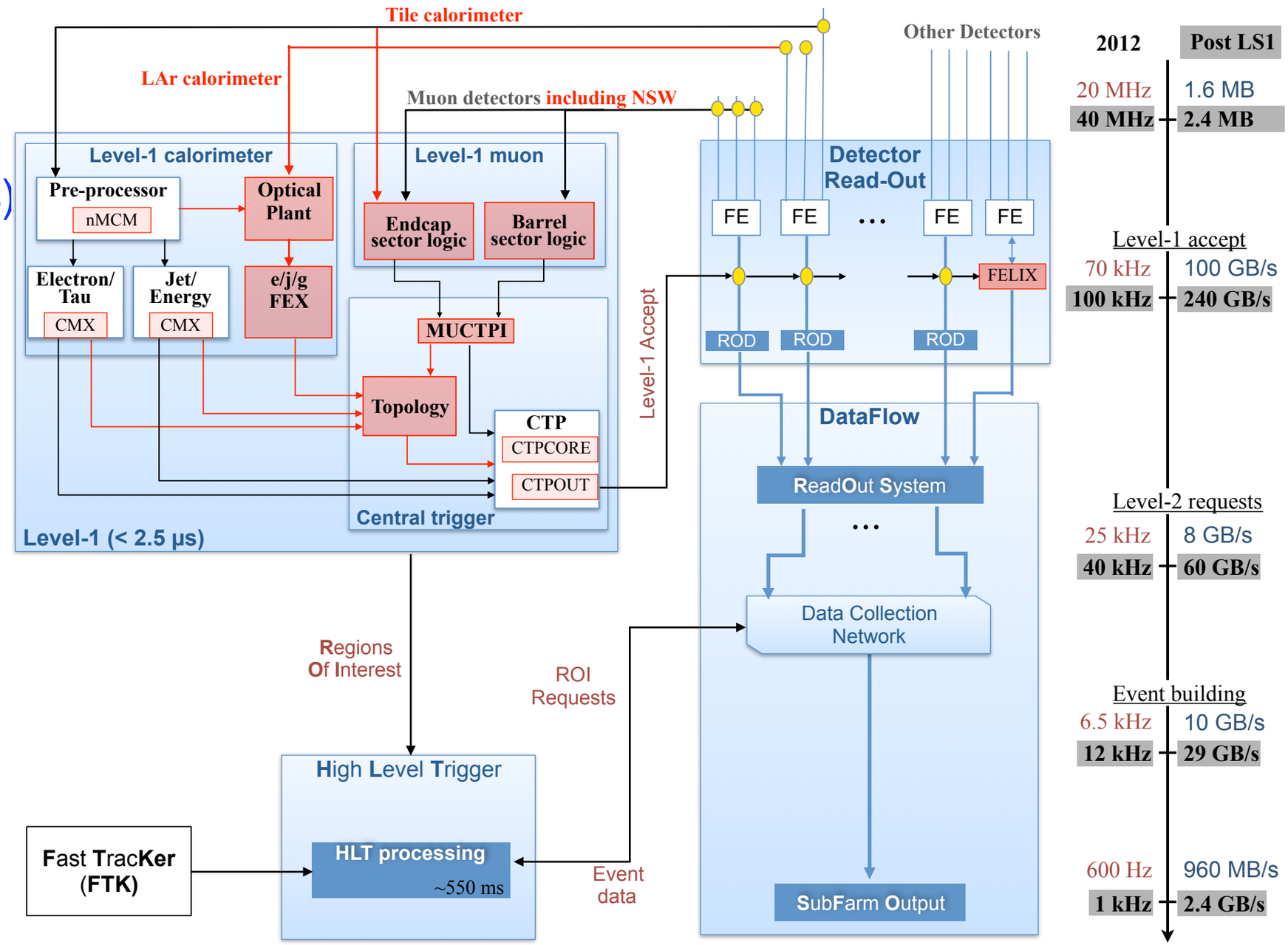




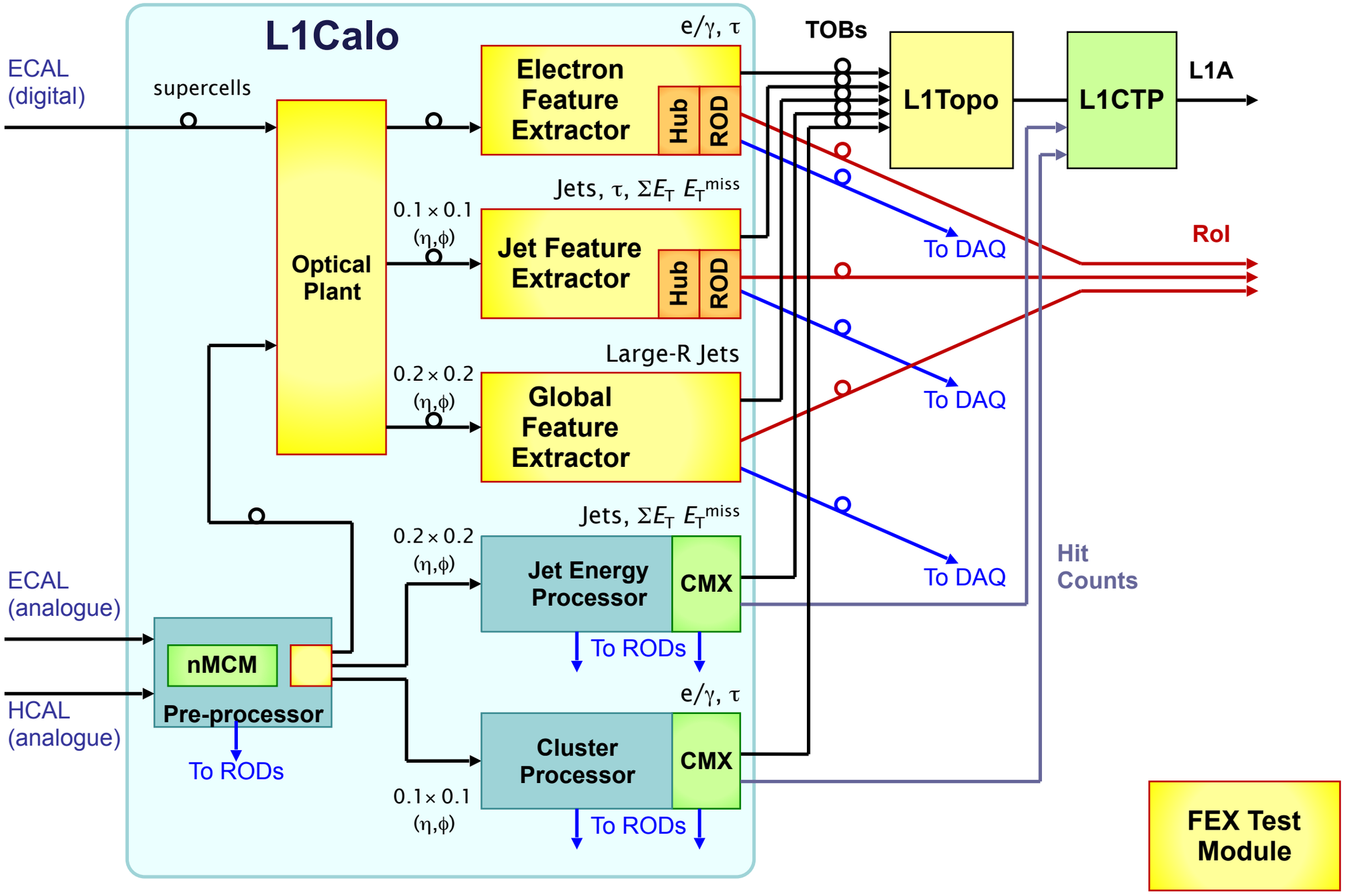
ATLAS Trigger and DAQ after Phase-I upgrade

Triggering in Phase-I will be achieved with an upgraded L1Trigger: a real-time, low latency path using:

- Multi-Gbps (6.4-12.8 Gbps) optical IOs
- Algorithms implemented in large FPGAs
- ATCA (VME) boards hosting multiple interconnected FPGAs using Multi-Gbps links.
- Example: jFEX (see later):
  - ATCA board, 5 FPGAs
  - 240 x 11.2 (6.4) Gbps inputs,
  - 48 x 11.2 (6.4) Gbps Outputs,
  - 120 x 11.2 (6.4) Gbps inter-FPGA connections.



L1Calo Phase-I Upgrade



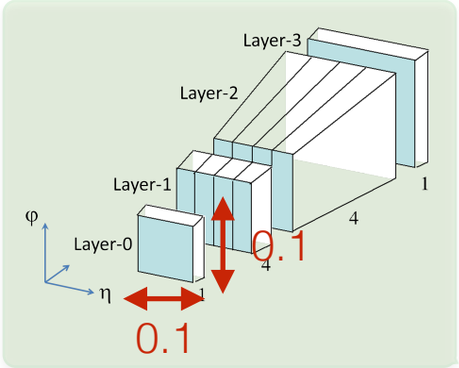
(see F. Carrio Argos presentation on calorimeters backend)

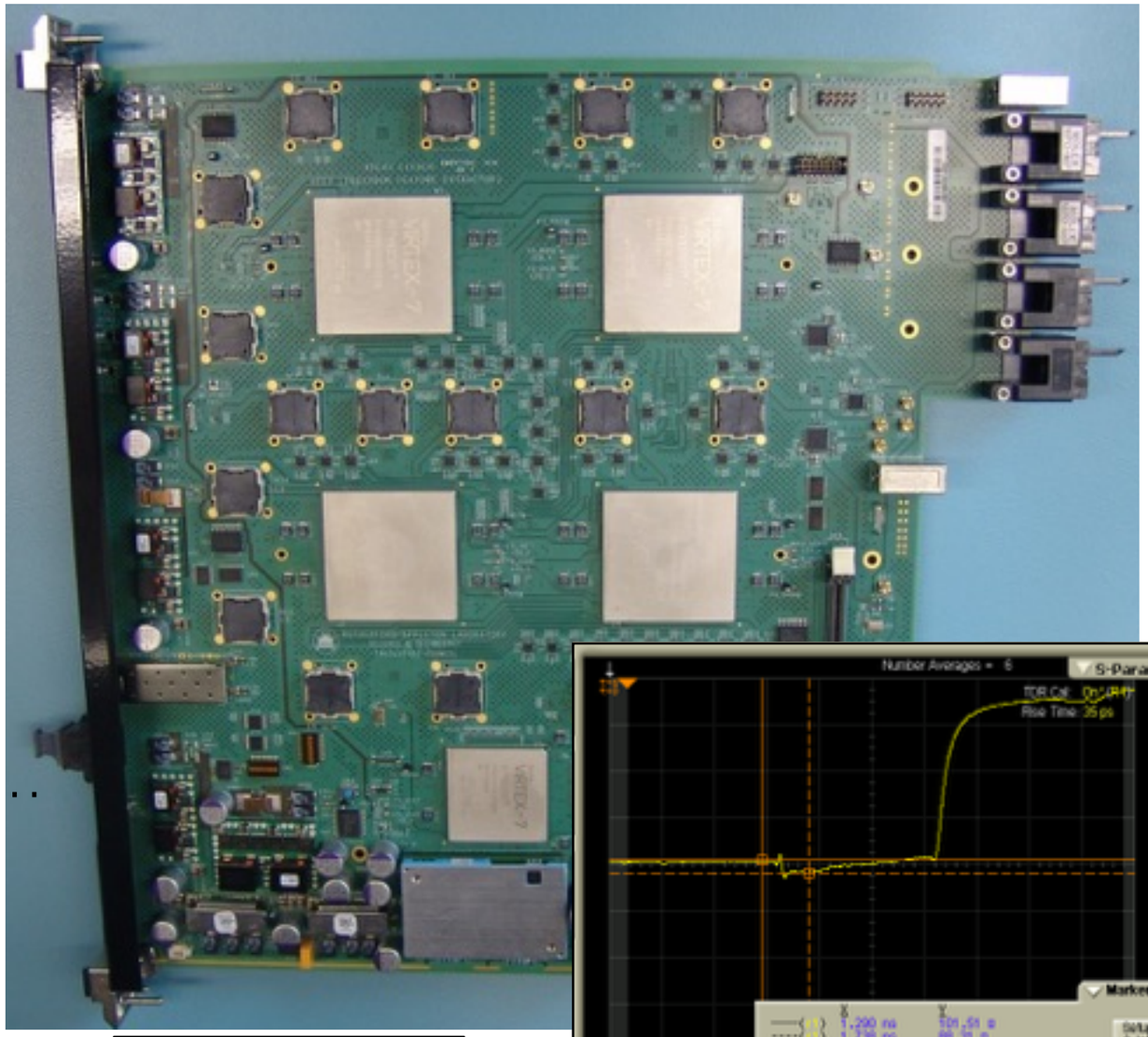
eFEX

- Identifies isolated e/γ and τ candidates (higher granularity and segmentation in depth)
  - 24 ATCA modules
- Order to manufacture placed July '15
  - 2 PCB batches failed
    - oven failure + plating voids
  - PCB Batch 3 succeeded
- First assembled module received
    - Testing underway
- Firmware
  - Basic Control firmware complete
    - IPBus, Configuration, Monitoring…
    - Tested on dev boards
  - Test engines for link-speed tests complete

Processing FPGAs, XC7VX550T (Virtex 7)

Control FPGA, XC7VX330T (Virtex 7)



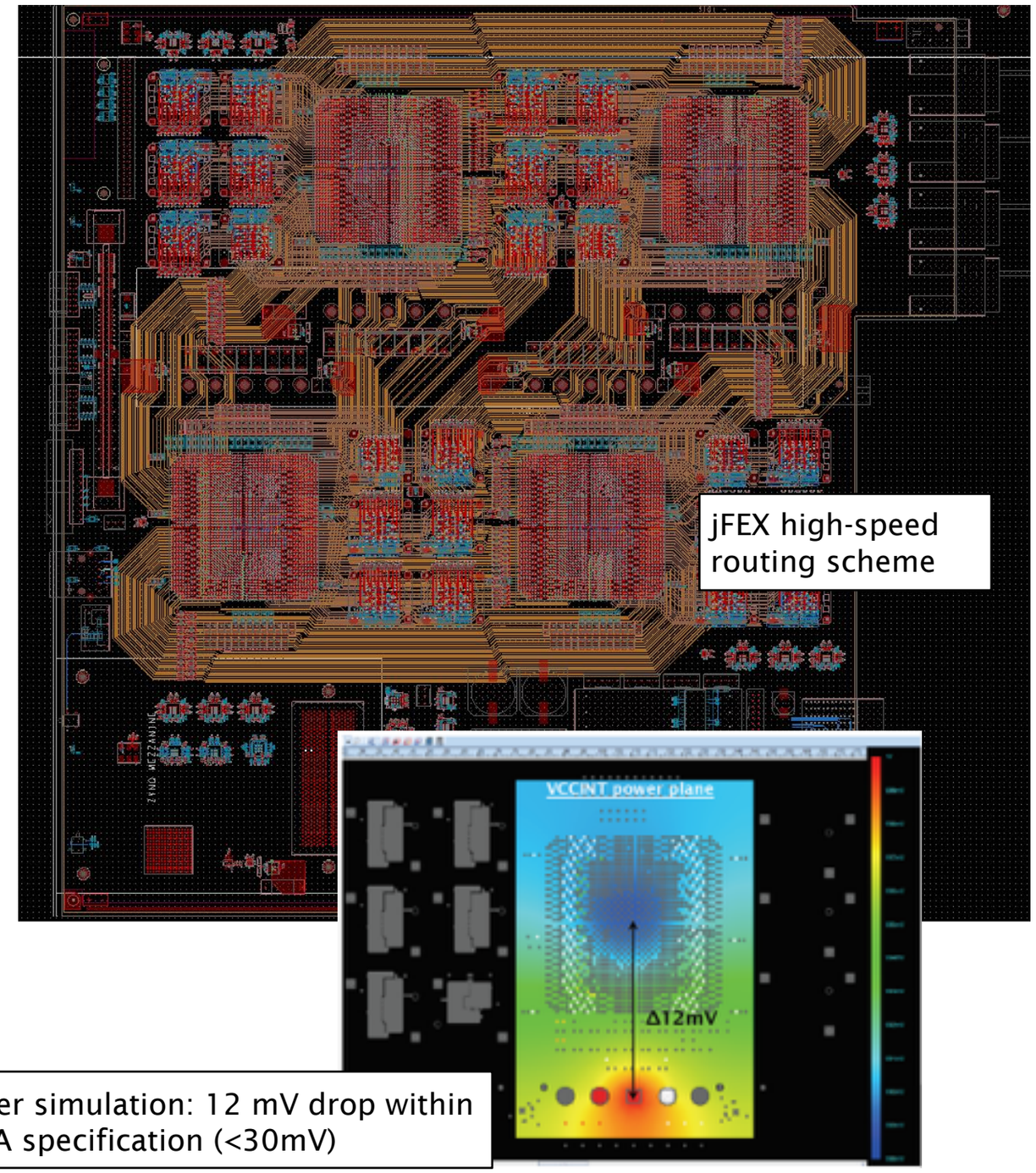


eFEX Prototype

TDR results of bare-PBC track

jFEX

- Identifies jets (large τ), ΣE_T, E_T^{miss} (improved performance for high-pileup and overlapping jets, e.g. gaussian jets Event-by-event pile-up corrections)
  - (7–10 modules)
- Design being routed
  - **Routing of High Speed Links completed**
  - Completed several iterations of simulation for power-plane optimisation
    - Challenge: FPGA under full load: current >60A
  - Completed design of the heat sink based on a careful evaluation of power dissipation and cooling scheme
- Firmware:
  - Control & monitoring FW exists
  - MGT FW well developed



jFEX high-speed routing scheme

Power simulation: 12 mV drop within FPGA specification (<30mV)

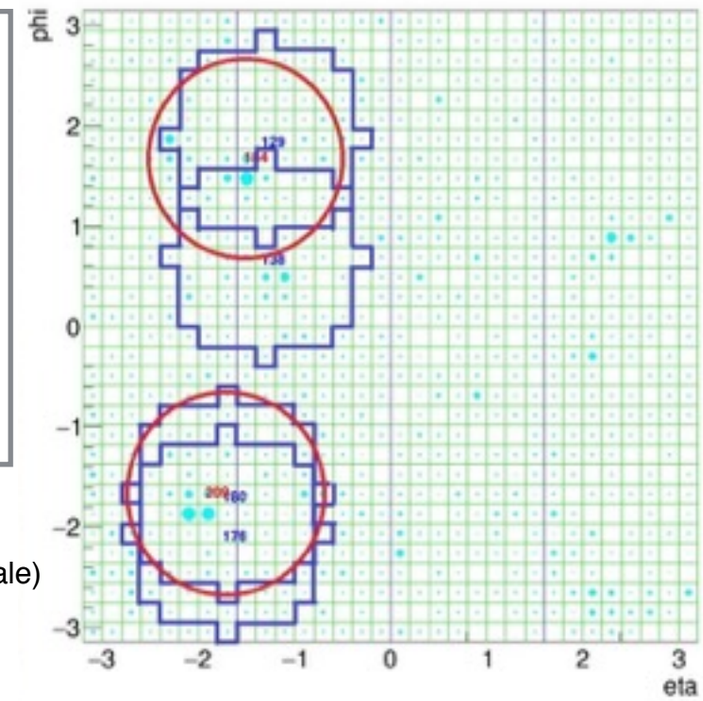
Processing FPGAs XCVU190 (Ultrascale)

Control SOC Zync 7

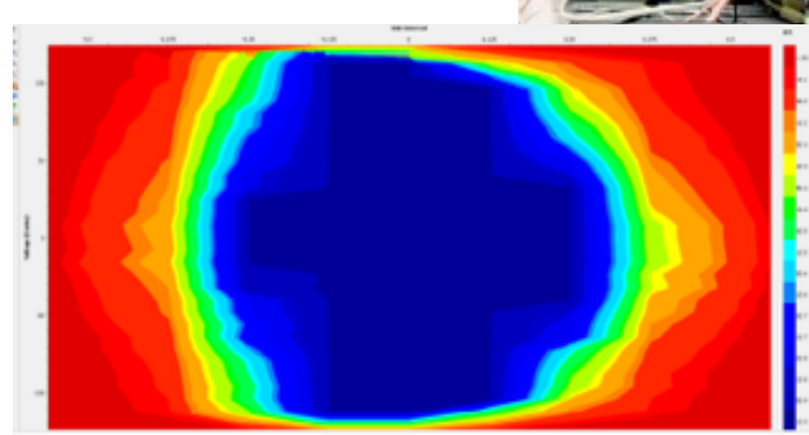
gFEX

- Identifies large-R jets, E_T^{miss}, centrality.
  - Single module
- Prototype v2 being routed
- Recent progress
  - Prototype v1 (single processor FPGA)
    - **80 MGTs tested with BER<10^{-15} @ 11.2 Gb/s**
    - Integrated with data flow and timing distribution system (FELIX/TTC)
  - Firmware v1 complete
    - Large-R jets, jets-without-jets
    - IPBus operational
    - Zynq running SLC5 Linux
  - **Used successfully in LAr–L1Calo link-speed tests (see later)**

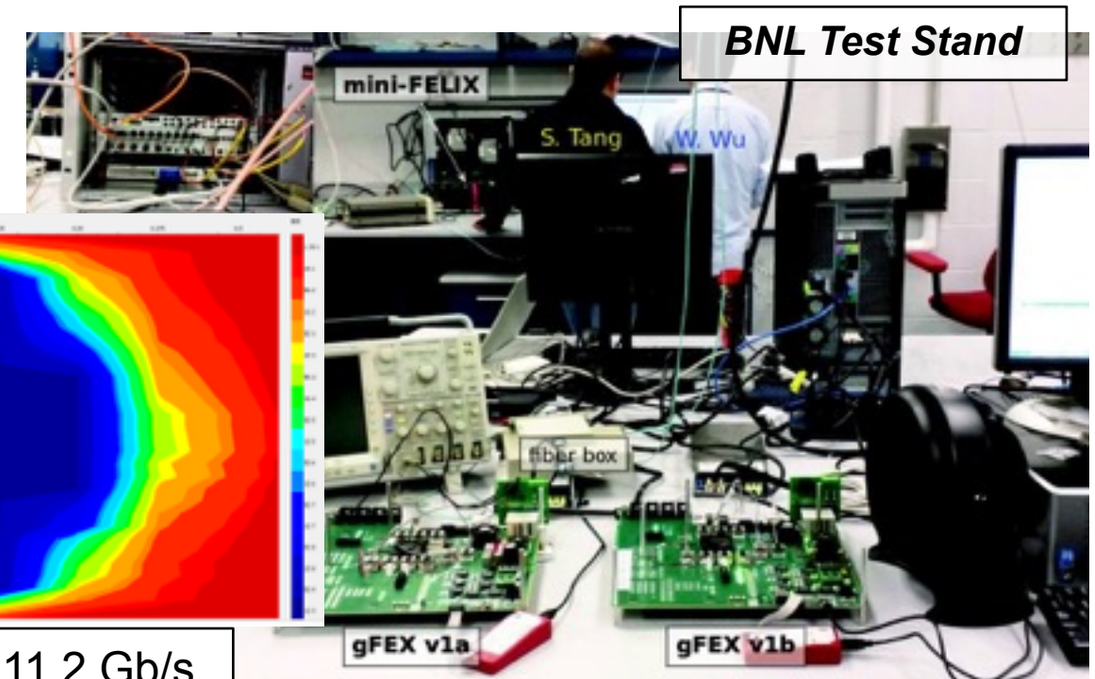
Algorithms Firmware v1 (simulation)
red: offline anti-kT R=1.0 jets
blue: gFEX R=1.0 jets



Processing FPGAs	XCVU160	(Ultrascale)
Control SOC	Zync 7	



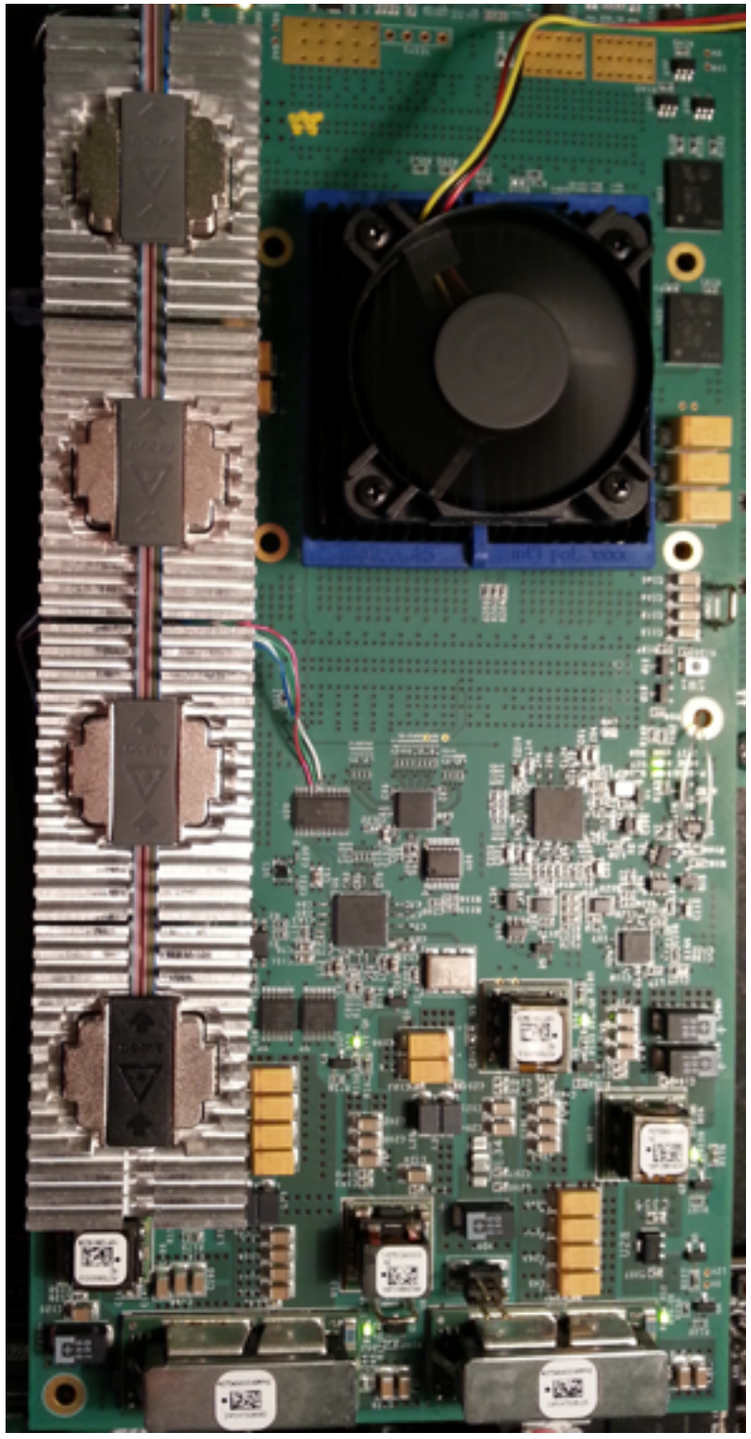
Eye Diagram at 11.2 Gb/s
LAr-FOX-gFEX & FELIX



2.4 ROD

- collects & buffer readout data across eFEX & jFEX shelf; transmits to ATLAS Dataflow (FELIX)
- **Prototype under test**
  - Tested successfully Power & clocks, Configuration logic (single image)
  - Optical links (20)
    - Felix 10.26Gbps BER < 10^{-14} (PRBS31)
    - S-Link 4.0Gbps BER < 10^{-14} (PRBS31)
  - 12/24 possible FEX Inputs tested
    - 10.26Gbps BER < 10^{-14} (PRBS7)
    - Limited by availability of other modules
  - Ethernet PHY
- Test will be completed when host board (Hub) becomes available.
- Firmware
  - FW to test all HW interfaces exists
  - IPBus FW + SW in development

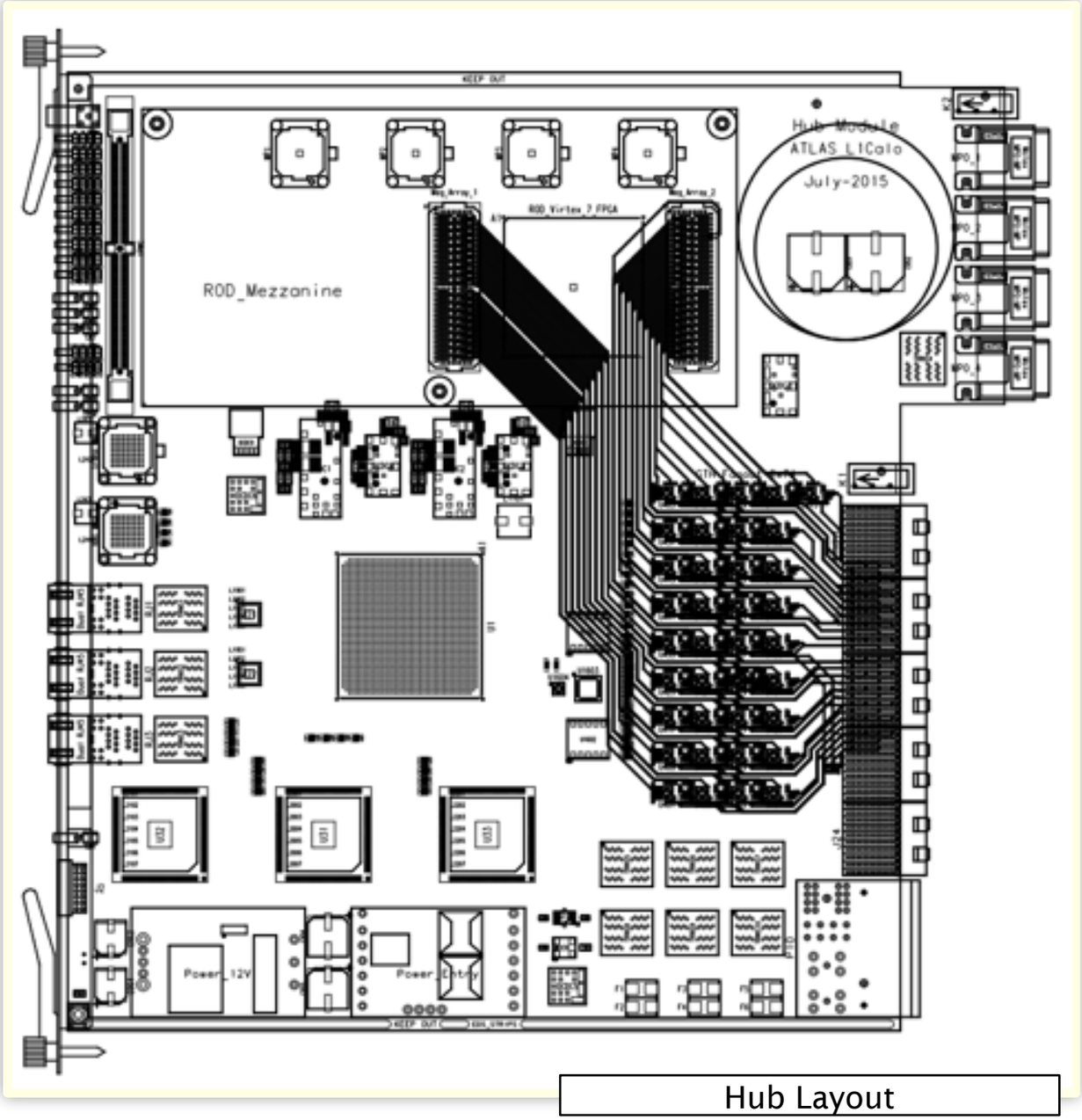
ROD: XC7VX550T (Virtex 7)



Hub

- control & clock hub; houses ROD
- Recent Progress
  - First iteration of layout & routing complete
  - But constraint on use of Ultrascale MGTs discovered (channel-bonding across device tiles)
    - Necessitates re-routing of high-speed signals
  - **Design being re-routed**
- Firmware
  - Development ongoing on V-7 and V-Ultrascale dev boards.
  - Version-0 of GBT and GbE interfaces exist
  - Firmware studies of Hub MGT configurations ongoing
  - Collecting best-practices for SSI chip firmware design

XCVU125 (Ultrascale) (was XC7VX550T)

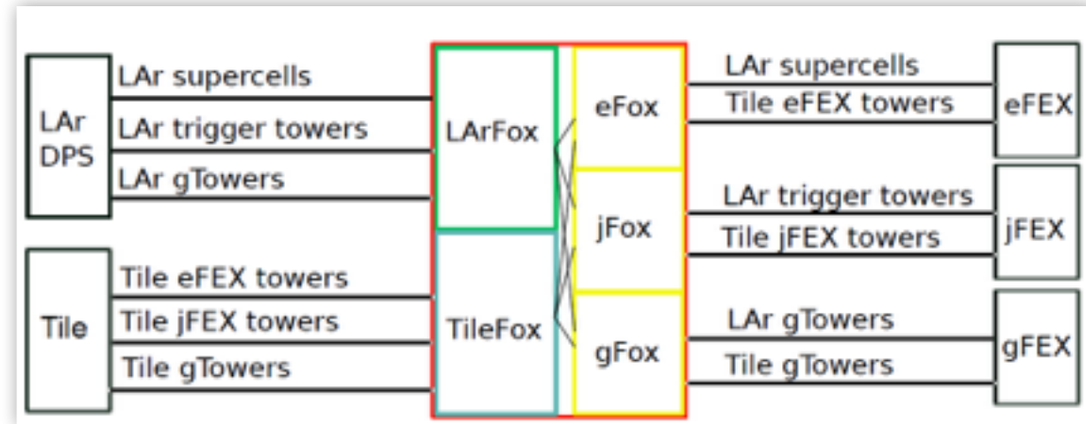


Hub Layout

FOX

- **Fibre-Optic Exchange: Re-maps & fans out input signals to FEXs**
- Design and production of demonstrator complete:
  - LAr/TileFOX & e/j/gFOX Demonstrators with
    - MTP & LC connectors
    - Fanout cables
    - Splitters
- Recent progress
  - Studies of attenuation conducted
  - **Used successfully in LAr–L1Calo link-speed tests**
  - Calorimeter-FEX mapping done for three link speeds (6.4, 9.6 and 11.2 Gbps). Compatible with Phase-II by updating Tile Fox.

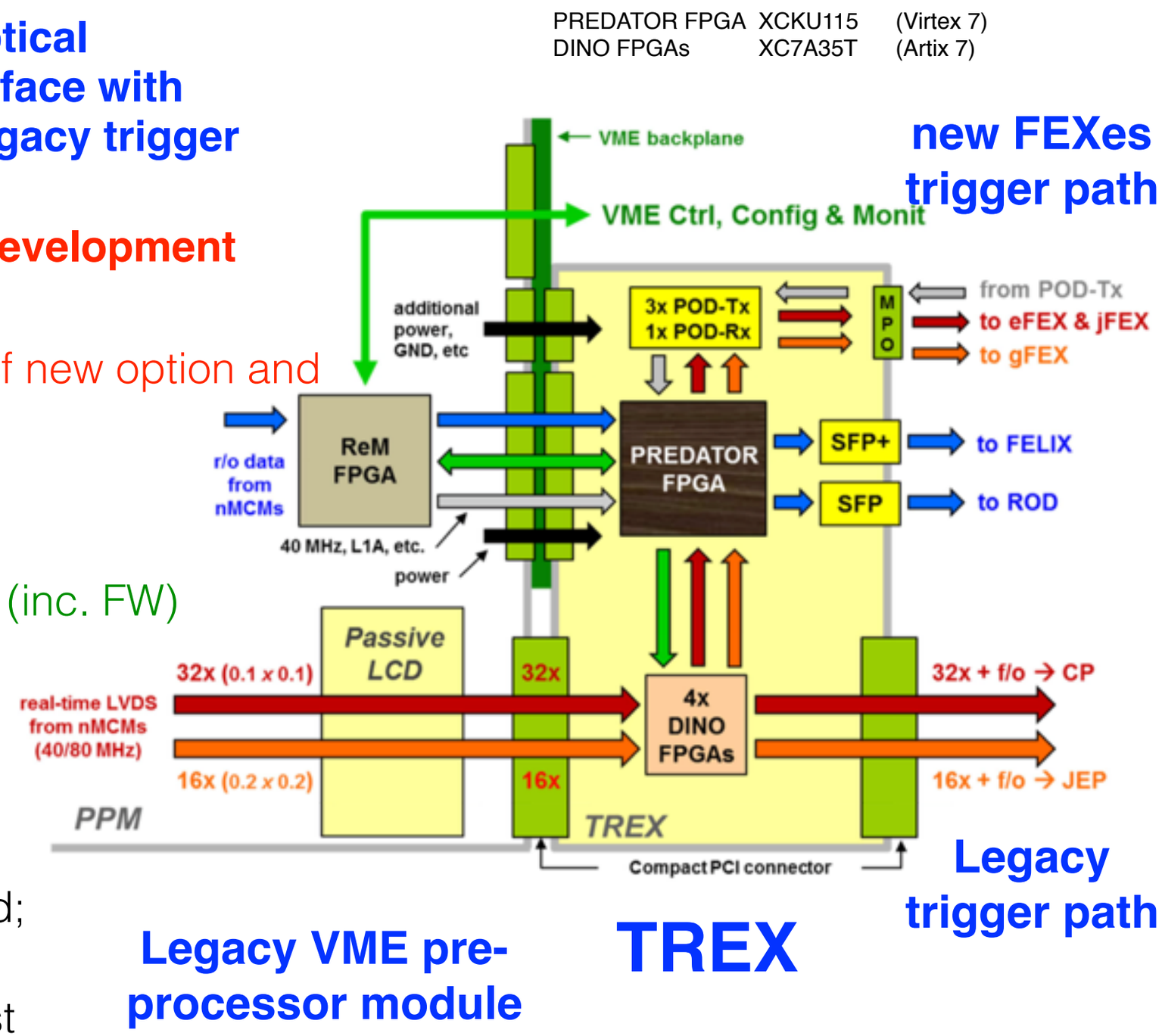
FOX, block diagram



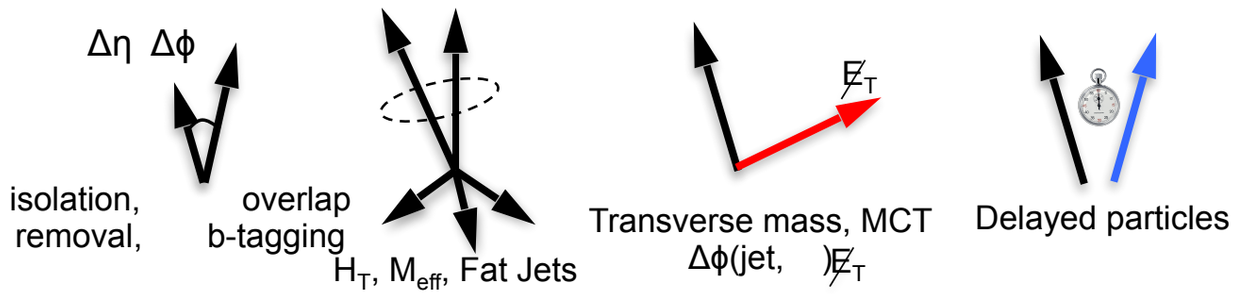
FOX Demonstrator Module

TREX

- **Tile Rear Extension: electrical–optical conversion of Tile signals to interface with Feature Extractors keeping the legacy trigger path.**
- **Schematics, layout firmware in development**
  - Necessarily in parallel
  - Delays incurred due adoption of new option and to effort shortage, now solved
- Recent Progress
  - Functionality blocks defined
  - Design of Legacy path finished (inc. FW)
  - Currently working on:
    - Power & clock distribution
    - Optical output
- Firmware developed using dev kit
  - 2 x 11.2 Gb/s links implemented; now extending
  - Provides experience & early test
  - To be used as test board for TREX



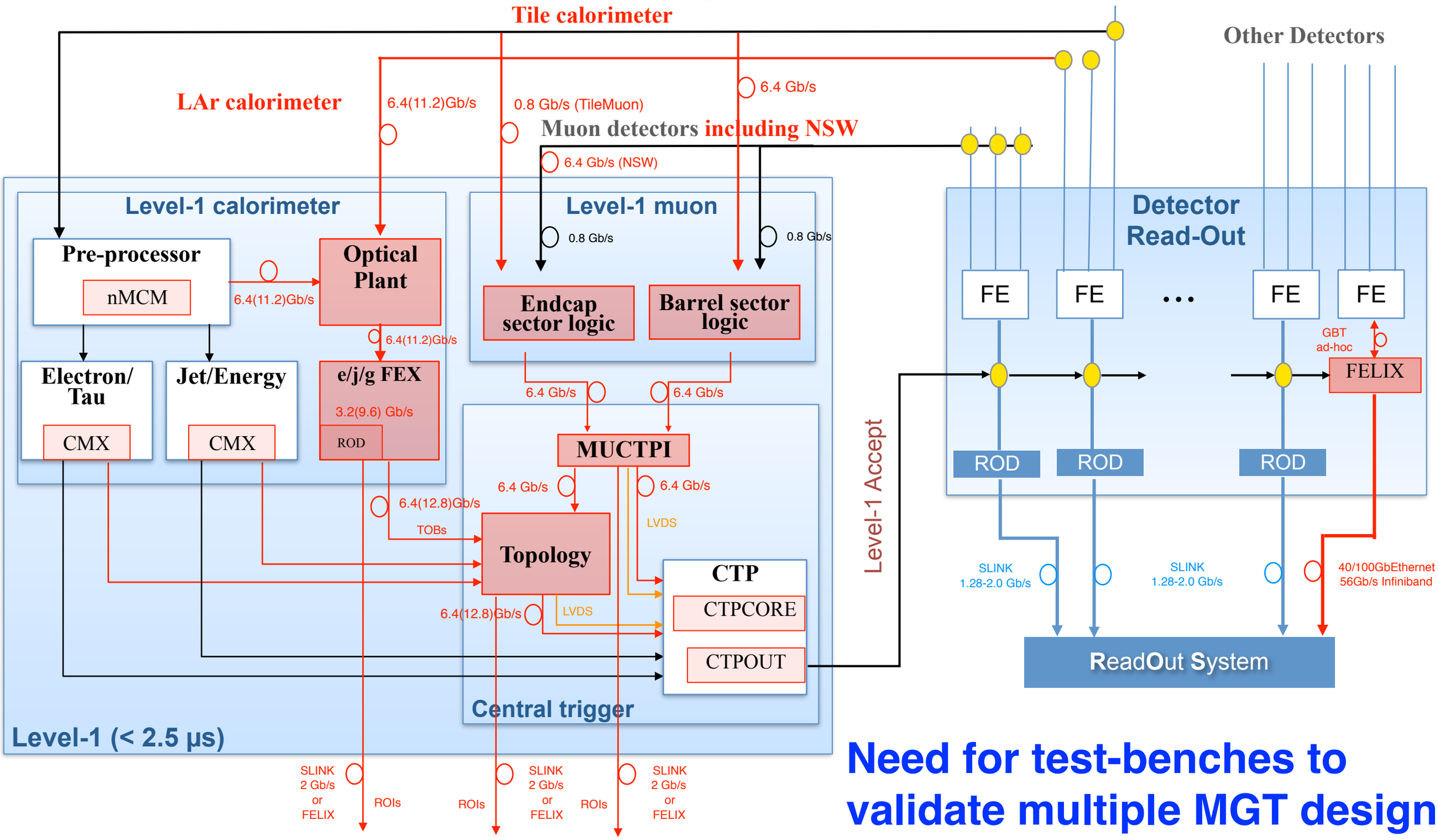
L1Topo



- **Event selection based on event topology**
- Current L1Topo can be considered a prototype for Phase-I. Expect only minor changes:
- But aim to implement Phase-II requirements at Phase-I
- To review
  - (Phase-I) Physics requirements
    - (Input from simulation & trigger community)
  - Impact of additional L1Topo modules on FEXes and L1Muon (additional fibres required)
  - Implications of Phase-II architecture

Run-2 L1Topo

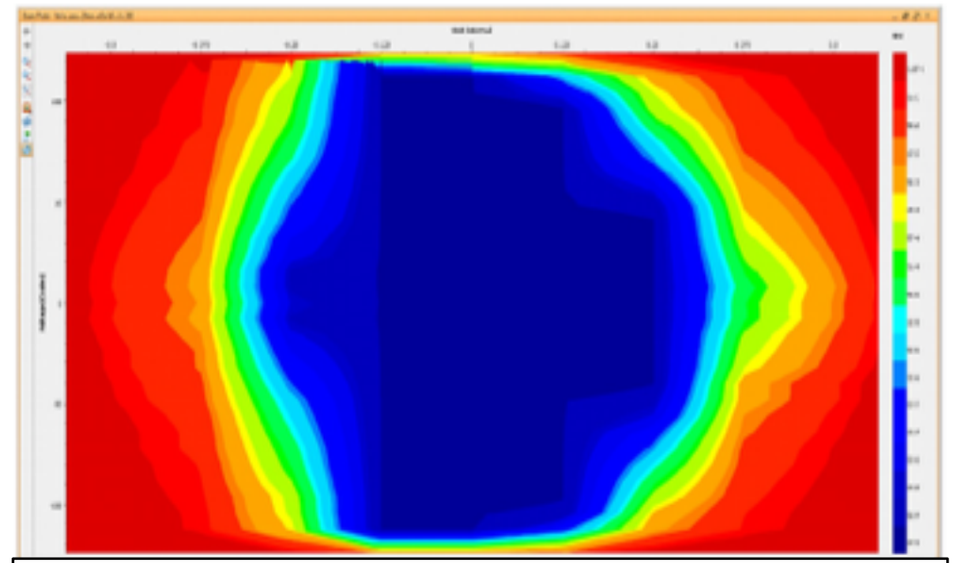
TDAQ Optical zoo



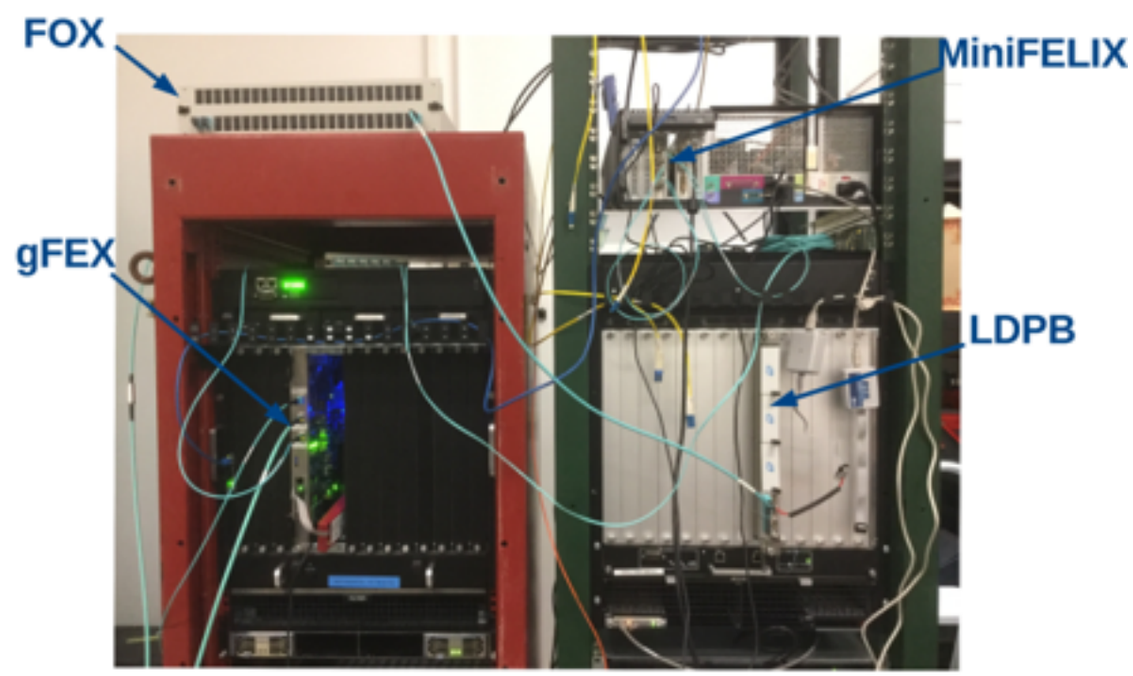
Need for test-benches to validate multiple MGT design working at various link speeds.

LAr–L1Calo Link-Speed Tests

- **Verified LAr (LATOME) – gFEX links at 6.4 Gb/s, 9.6 Gb/s & 11.2 Gb/s**
  - **BER < 10^{-14}**
- Validated technology of FOX demonstrator
  - No. connections foreseen for final system + passive splitters
- LAr + gFEX driven from common TTC clock via MiniFELIX (ATLAS data flow prototype)
  - Optimisation of MiniFELIX necessary for links at 11.2 Gb/s
- gFEX–L1Topo link demonstrated at 12.8 Gb/s
- First step towards LAr–L1Calo link-speed decision (May 2016).
  - LAr—eFEX results crucial for decision
- First step in integration with LAr
- Test rig to form basis of L1Calo system (+ LAr) test facility



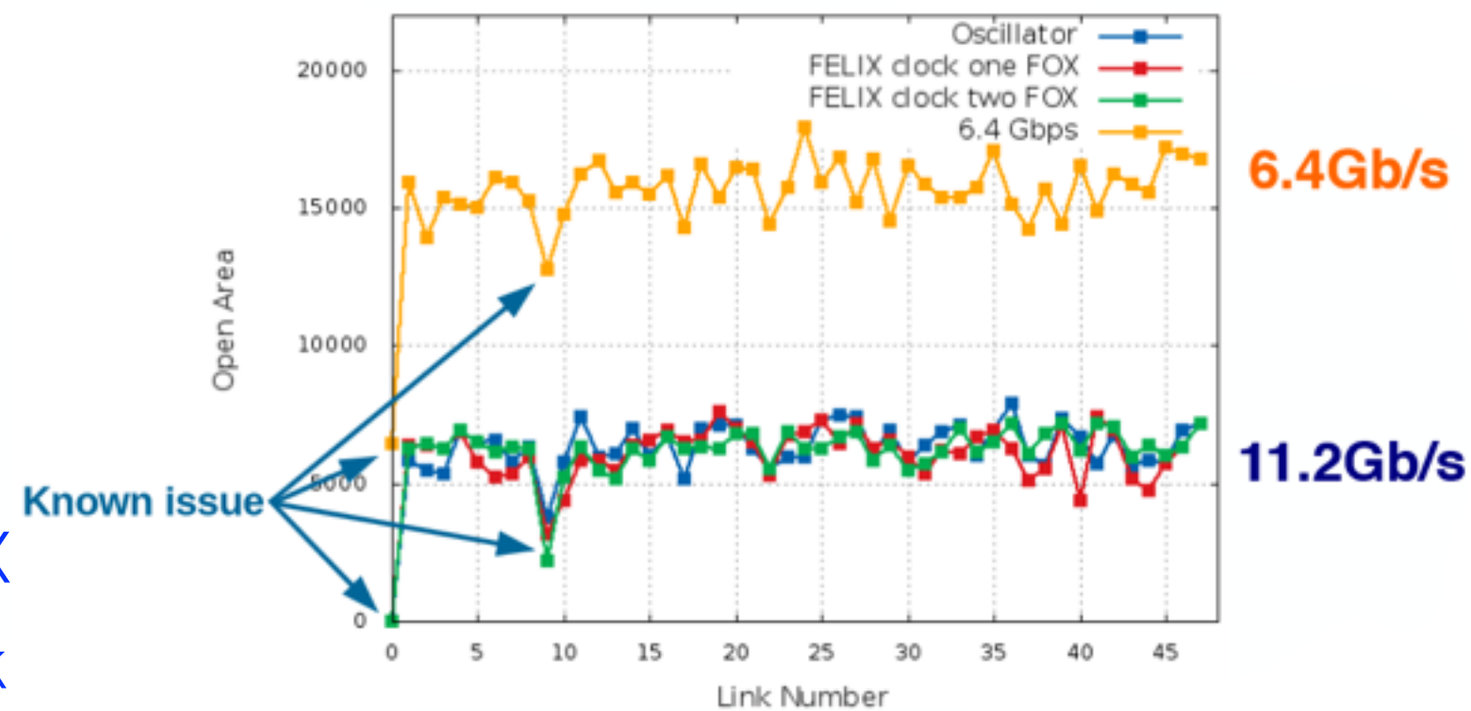
Eye Pattern From IBERT, 11.2 Gb/s
LATOME ➔ gFEX: two stages of FOX ➔ gFEX
Clock = FELIX oscillator



LAr–L1Calo Link-Speed Tests (2)

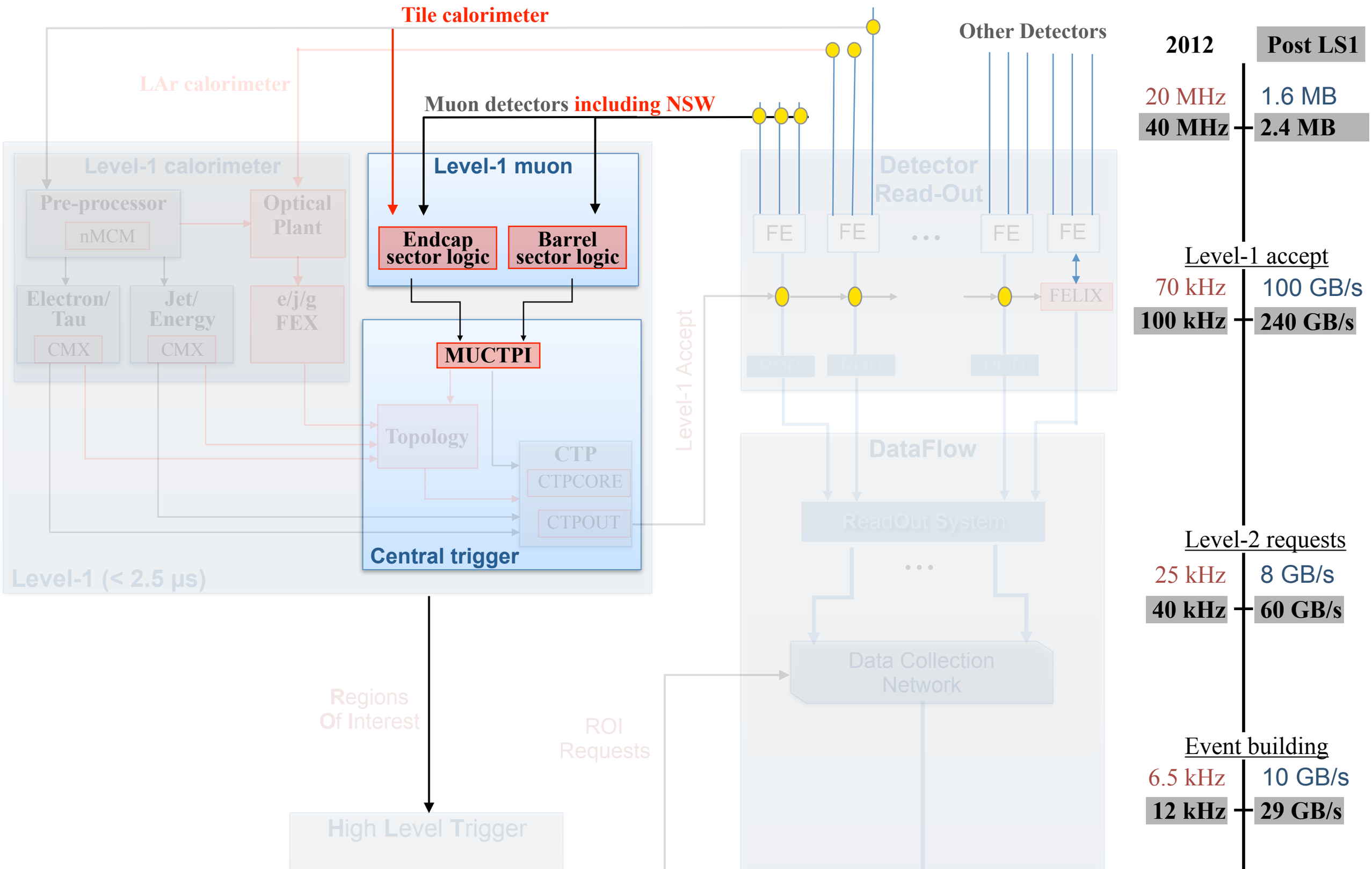
- **48 links run simultaneously**
  - (inc. 2 links on LATOME with known problems)
- Clock architecture
  - local oscillator
  - recovered clock from FELIX
  - FELIX using oscillator clock
  - TTC clock (TTCex, TTCvx)
- FOX Setup
  - One stage
  - Two stage
  - with and without splitters

Open area of eye diagrams in LDPB-gFEX



Link speed	Clock Source	FOX stage	BER	average open area
11.2Gb/s	Oscillator	1	2×10^{-14}	6408
	FELIX oscillator	1	2×10^{-14}	6191
	FELIX oscillator	2	6×10^{-15}	6340
6.4Gb/s	FELIX oscillator	2	7×10^{-15}	15766

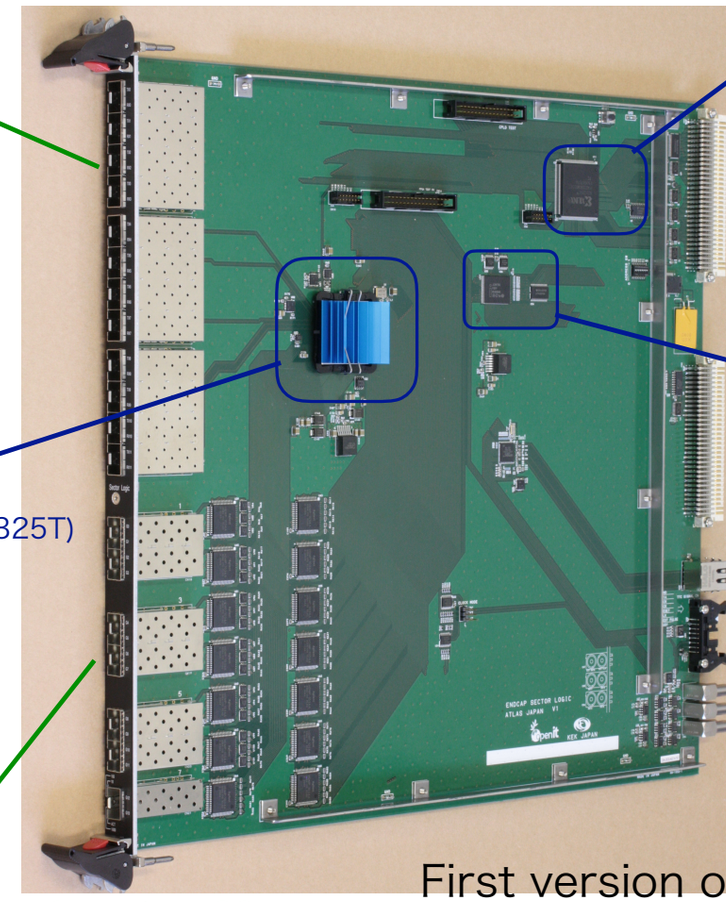
Muon Trigger



Off-detector part of Muon Endcap trigger (72 modules)

3.1 Muon Endcap New Sector Logic

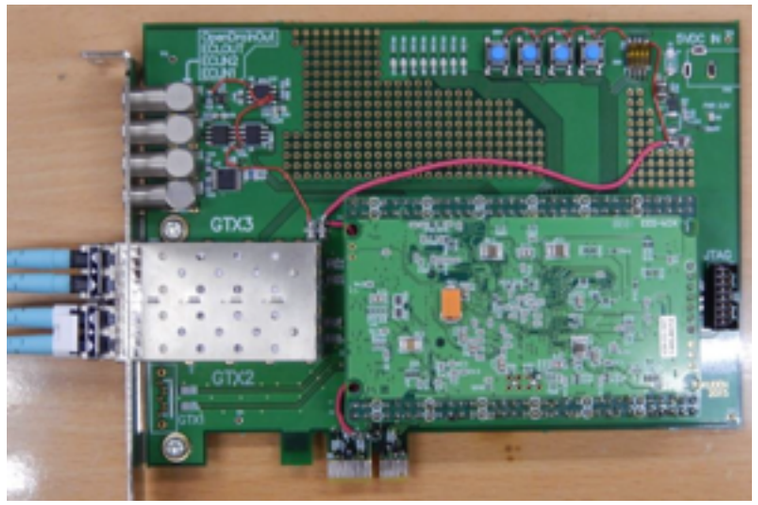
- **Prototype module has been successfully tested in 2015.**
  - **GTX's has been operated up to 10.24 Gbps (6.4 Gbps required).**
- Module-0 has been submitted end Dec. Five assembled modules to be delivered early March.
  - Hardware functional tests (all I/O's) end March.
- Firmware development ready in April.
  - IO parts simulating real data protocol/format
    - GTX : 6.4 Gbps , G-Link : 800 Mbps
  - Readout path
    - L1B -> de-rad. -> zero-suppress -> output buffer -> SiTCP
  - Trigger path
    - Trigger algorithm
    - Latency measurement



First version of prototype boards came in October.

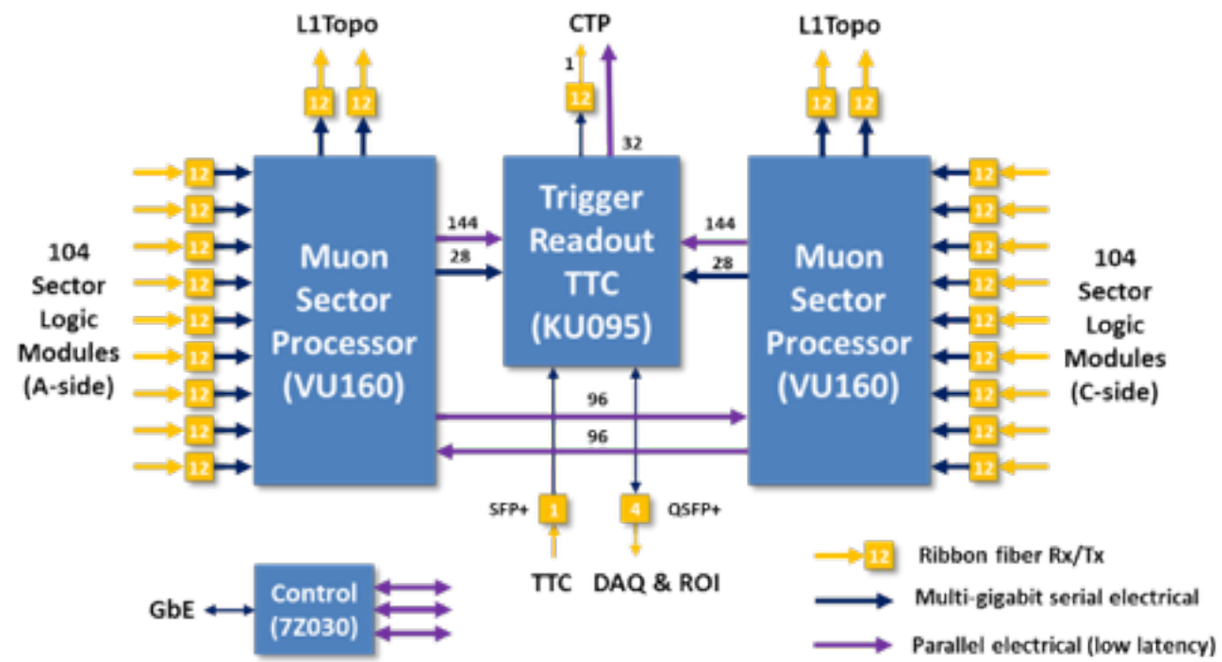
Slink/Busy board

- Slink/Busy prototype available, tests successful.
- TTC fanout and readout board PCB design started. First prototype board expected in May



MUCTPI

- Interface between Muon Barrel and Endcap triggers and Central Trigger Processor (provide full granularity Muon ROI to L1Topo)
  - single module
- PDR done on 9th December 2015
  - First prototype expected end of 2016.
- current status
  - FPGA development and custom mezzanine boards are being used to make early firmware development and integration tests with new sector logic interfaces.
  - custom mezzanine submitted to manufacturing.
- System lifetime: Phase-II

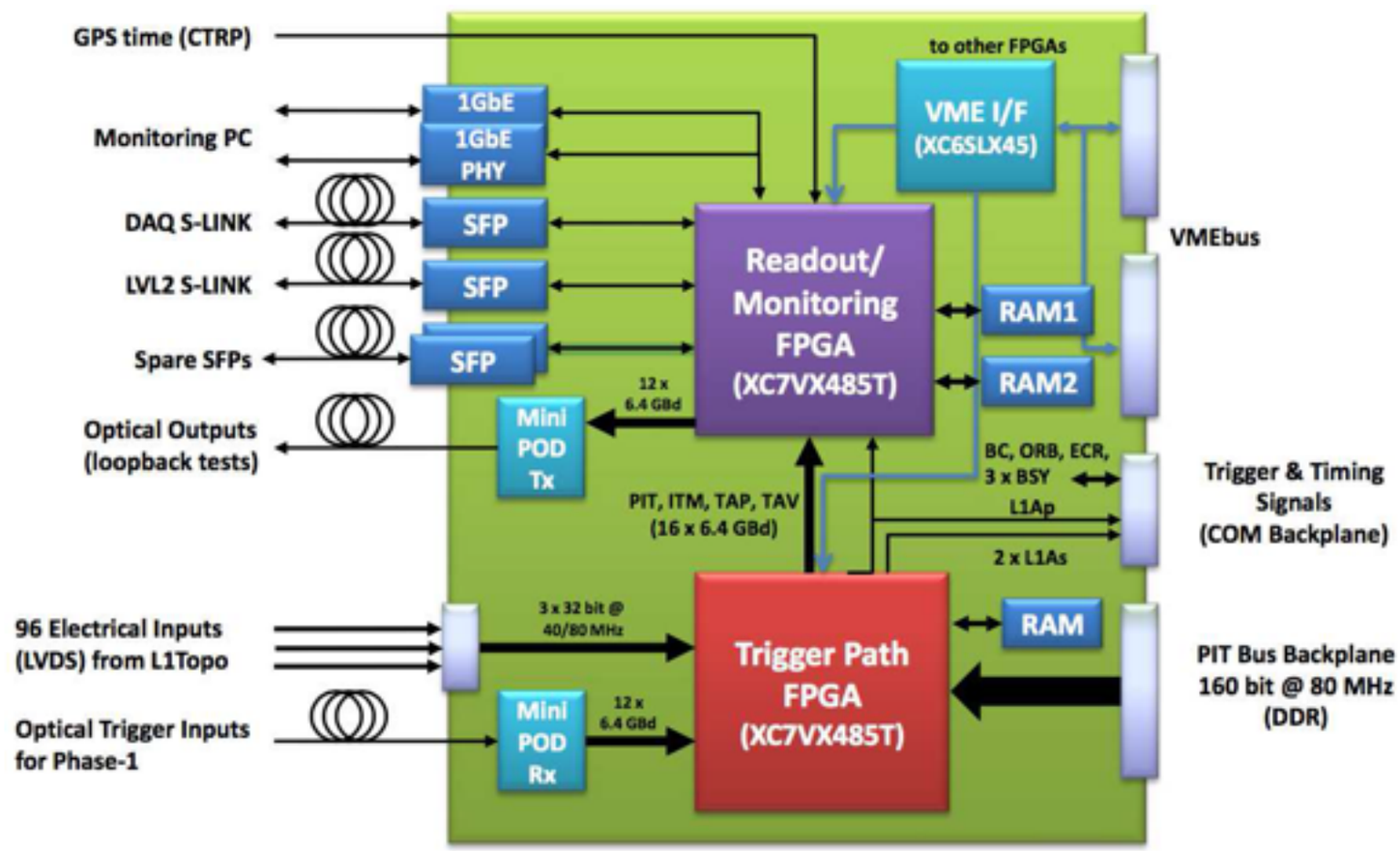


ATLAS Trigger Phase-I timeline

- Phase-I trigger projects have completed all Preliminary Design Reviews:
  - Full-functional prototypes are being built and tested (main focus of this presentation). First system tests started (optical interconnection tests).
- Aim to complete:
  - Pre-production Design Reviews by Q3-2017.
  - Complete production by Q3-2018.

Latency, optical vs electrical interconnections

- Phase-I latency is a concern, due to constraints from existing TDAQ systems:
  - need to integrate legacy systems with additional processing elements along trigger path on both Calorimeter and Muon Trigger.
  - aim to maintain Run2 latency below about 2 μs.
- High-speed serialisers-deserialisers are not latency-friendly, need to resort to electrical connections on critical paths.
- Phase-II latency is not a concern:
  - Specifications: latency below 10 μs.



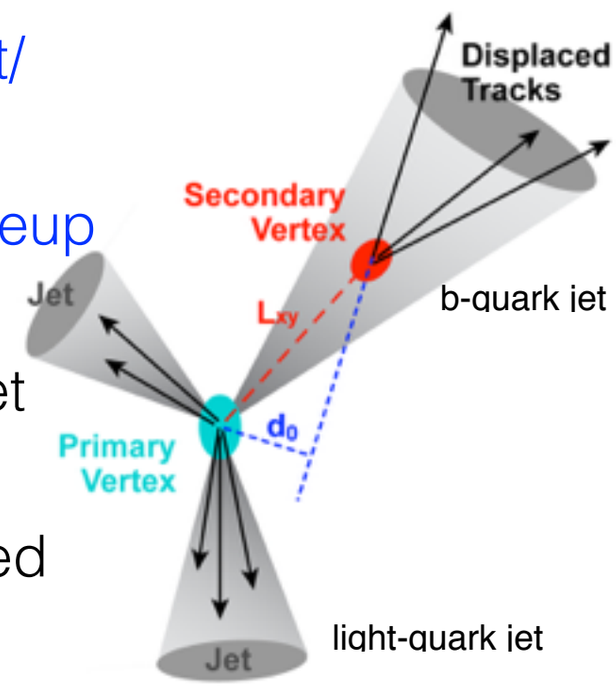
Central Trigger Processor module

Phase-I High-level Triggers

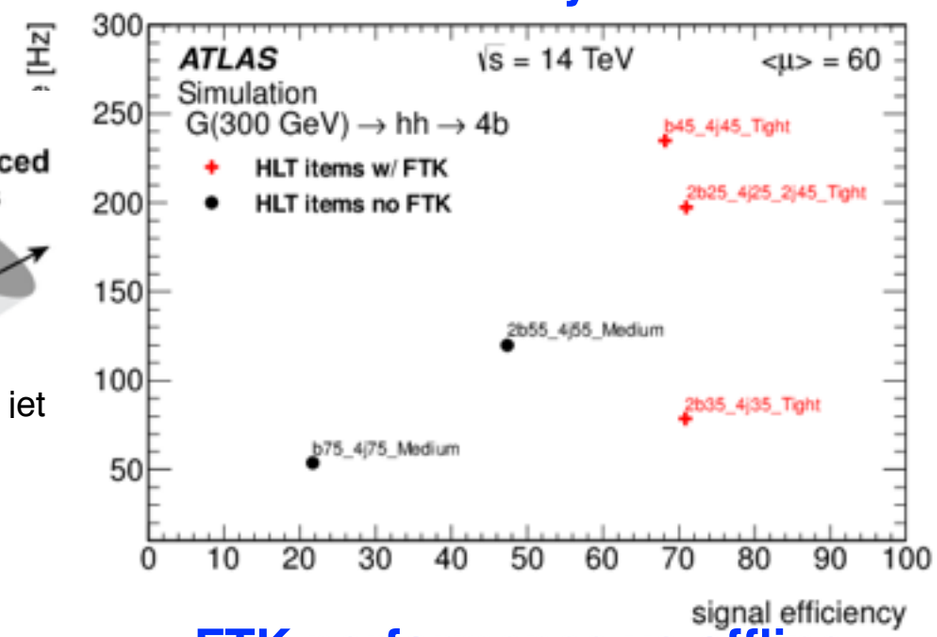
- Phase-I Hardware upgrade of High Level Triggers foresees the deployment of a Fast-Track Trigger:
  - Early Installation starting in 2016 (see M. Beretta *Current ATLAS FTK* talk, 8th March).
- Other upgrades foreseen to exploit:
  - the technology evolution.
  - availability of specialised hardware.
    - Goals of testing online at the end of Run 2 & deploying the full system in Run-3.

FTK Physics motivation and architecture

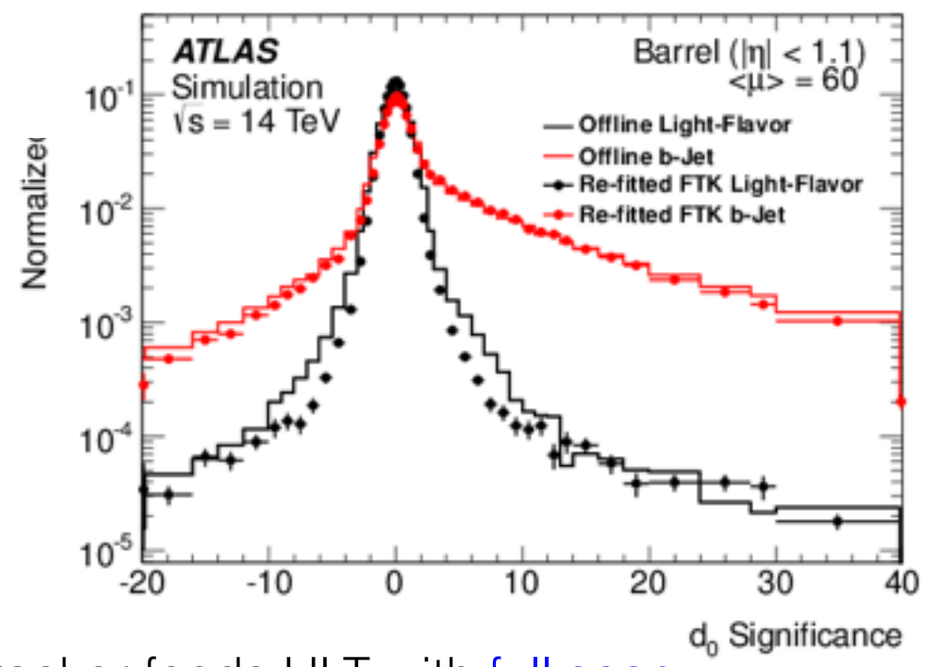
- (see M. Beretta presentation)
- Exploit full-scan FTK tracking in HLT
- Tau identification, b-tagging and Jet/MET pileup correction
- Primary vertex reconstruction for pileup resilient algorithms
- Can improve efficiency for multi-b jet signals
  - 3x efficiency improvements for ~fixed rate

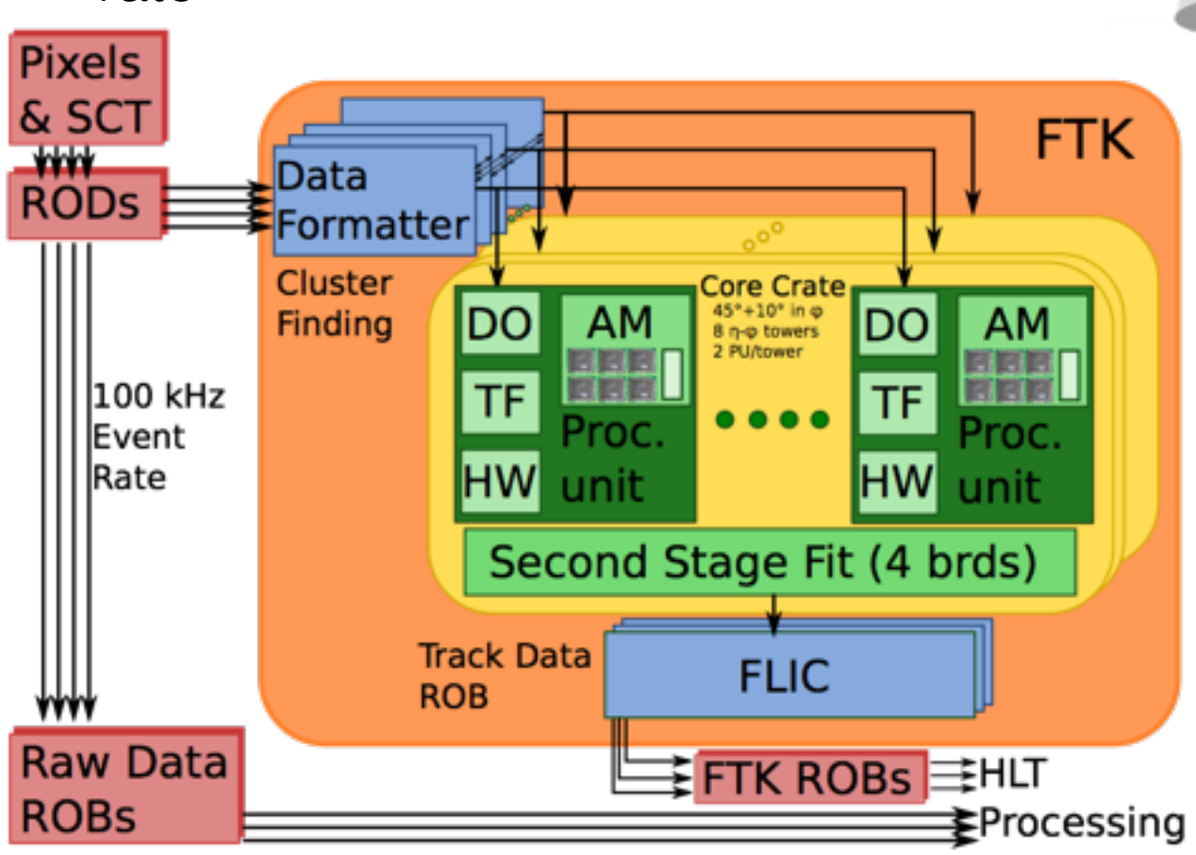


Full-scan efficiency with w/o FTK



FTK performance vs offline

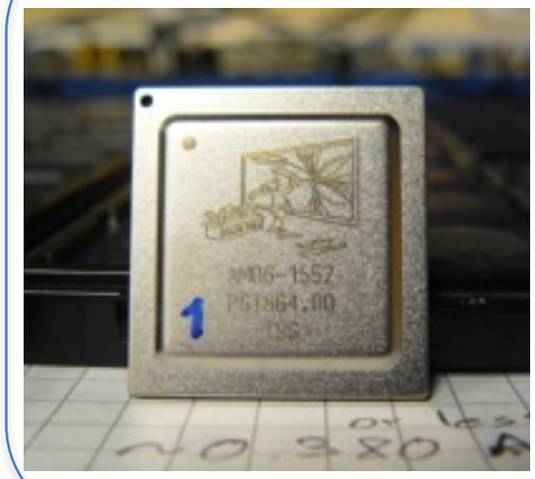




- The Fast Tracker feeds HLT with full scan tracking at 100 kHz $p_T > 1$ GeV
- Combination of ATCA and VME cards
- 8192 ASICs (65nm): 1 billion patterns on ~2000 FPGAs. Thousands of I/O links up to 10 Gb/s

FTK HW arriving at CERN

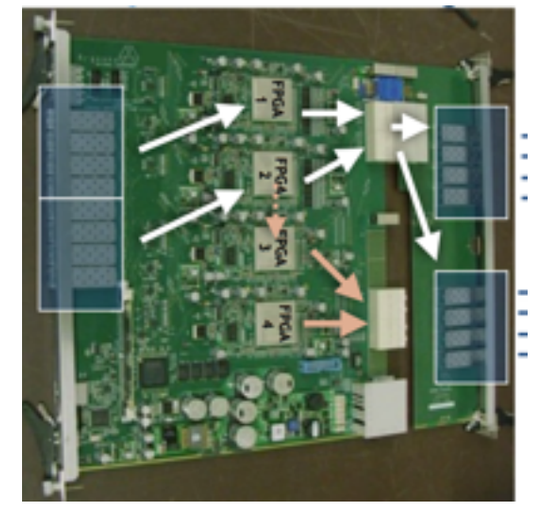
FTK full scan tracking at 100 kHz.
Reconstruct up to O(30M) track/s
2016 goal: commission barrel only system



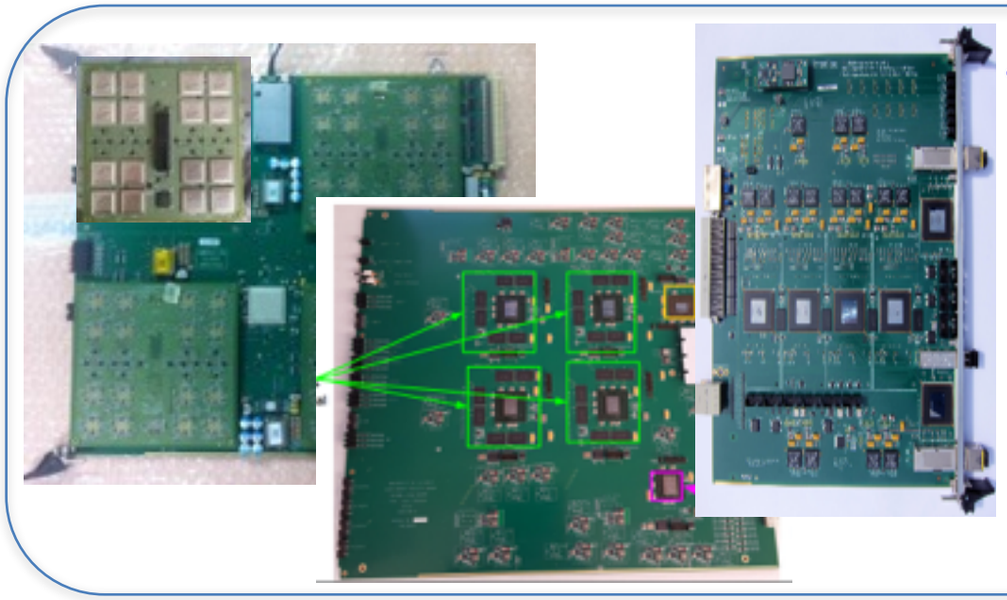
AM06: 65nm ~160mm^2
Working at 100 MHz
(nominal speed)

- Now: package more for this summer
- July: produce more AM06 for next year

FTK Input and Output cards fully produced
Now: being installed and commissioned

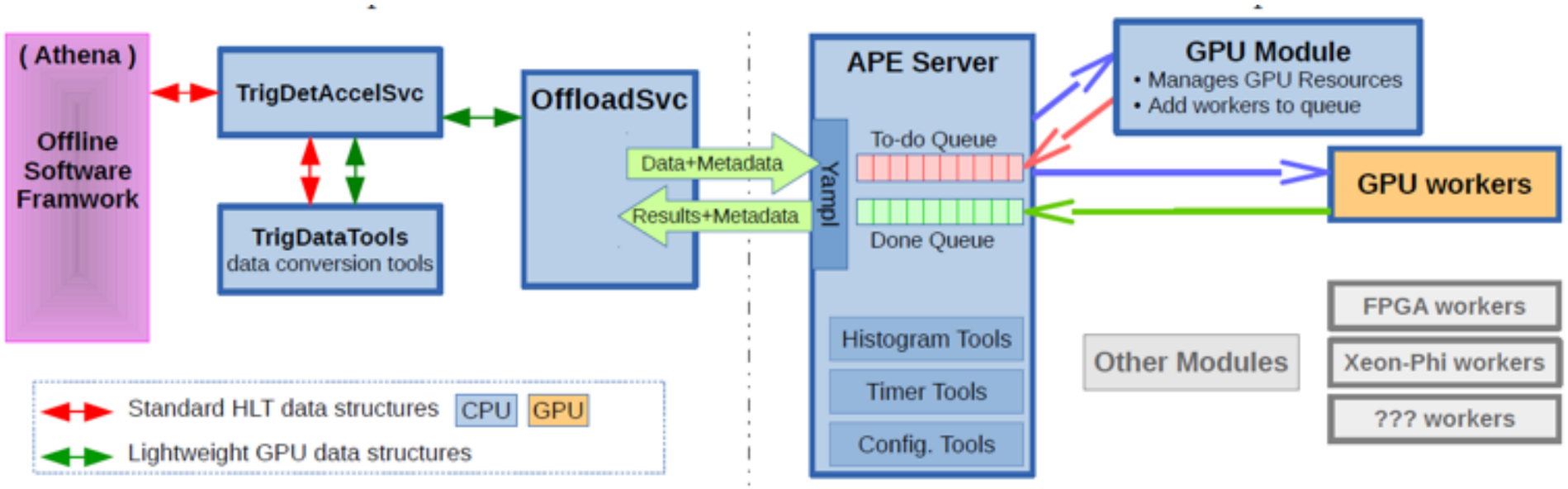


10/32 modules already installed and operated in 2015



- Core processing cards produced or in production soon
  - July 2016: 12.5% processing power installed
    - Barrel only system
  - April 2017: 25% processing power installed
    - Full coverage
  - 2018: full system installed
    - Full coverage & full processing power

HLT Accelerator prototype



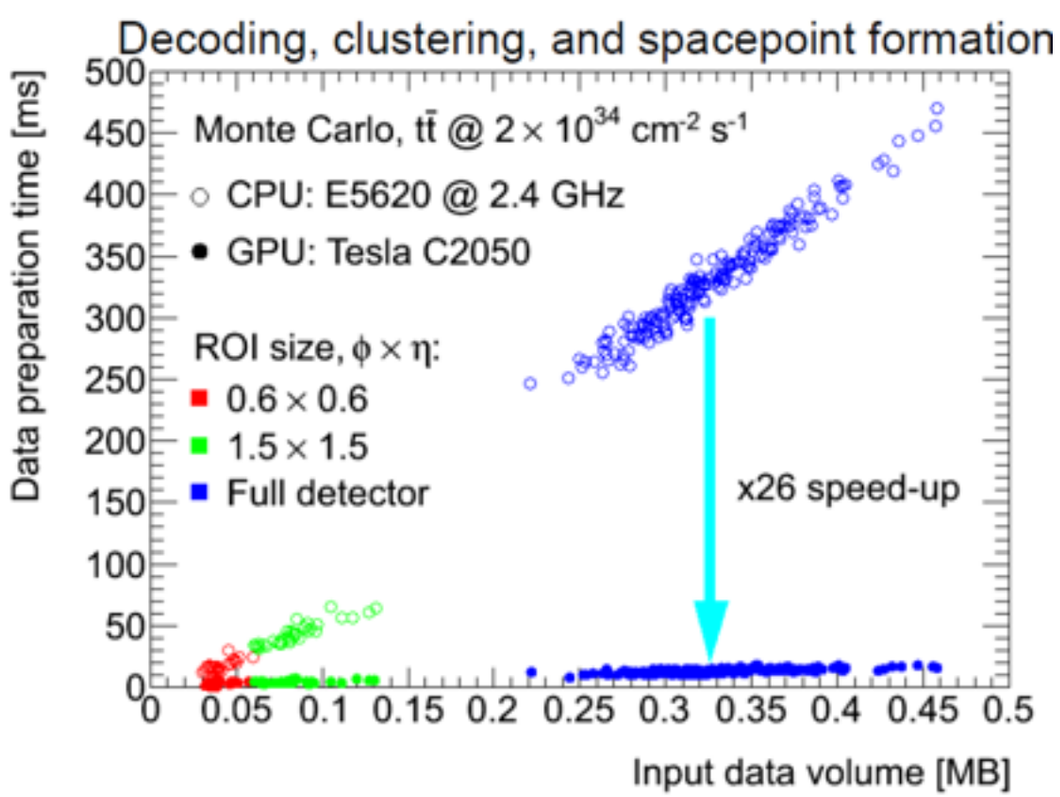
First prototype

Hardware: GPU server at RAL –
- dual quad-core Westmere 2.4 GHz, Nvidia Tesla C2050 GPU (448 cores @ 1.15 GHz, 3GB on-card memory, PCIe 2.0)

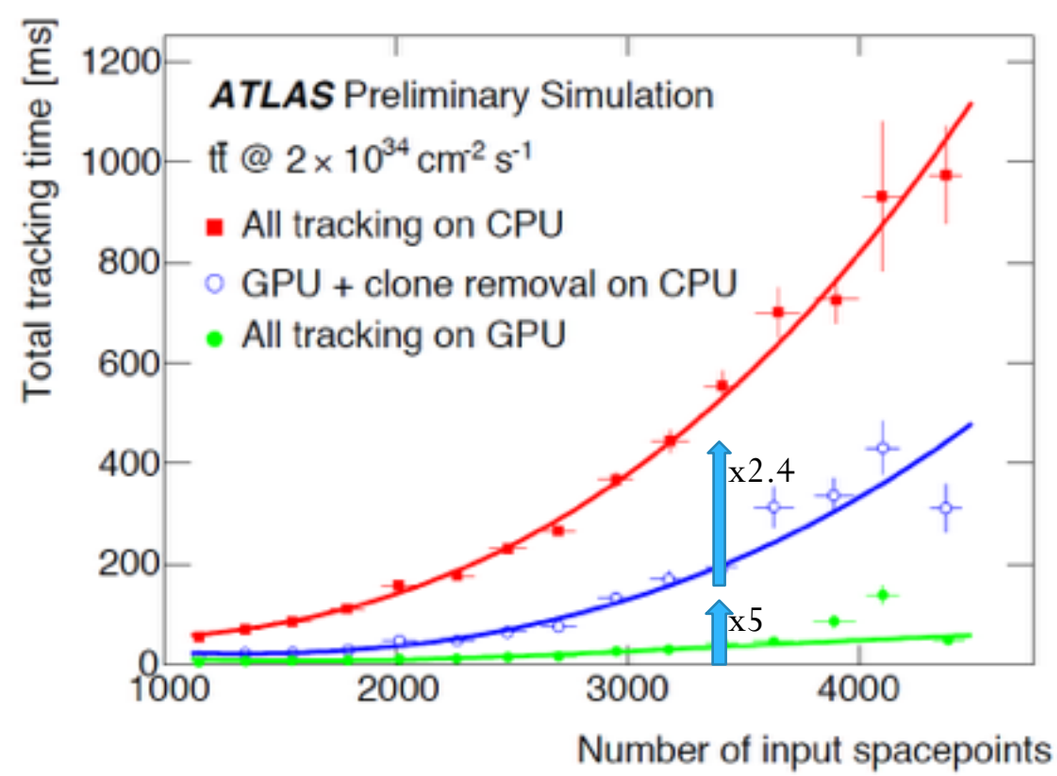
Software:
- Nvidia CUDA 4.0 for GPU programming
- SLC5 + Linux GPU driver from NVidia, AtlasHLT, 17.1.0, opt, 32

GPU-based or FPGA-based modules foreseen as co-processors. First prototype evaluated speed-up of max 26 and overall 12 for clustering and track-finding algorithms.

Pixel clustering on GPU



Combinatorial Track finding on GPUs



Summary

- Calorimeter trigger upgrades foresee new Feature Extractor Processors implementing new algorithms and exploiting a finer granularity LAr information.
- Muon trigger upgrade will use New Small Wheel Detector and information from outer Tile Calorimeter cells to reduce fakes in the endcap region.
- ATLAS Phase-I Level-1 Trigger foresees the deployment of ATCA (and VME) modules, hosting many FPGAs interconnected using a large number of high-speed (6.4-12.8 Gbps) optical links.
  - Phase-I trigger projects have completed all Preliminary Design Reviews. Full-functional Prototypes are currently under design or test phases.
  - Aim to complete Pre-production Design Reviews by Q3-2017.
- High-Level Triggers will exploit Full-scan tracking from a Fast Tracker System. Successive upgrades of of High-Level trigger will see the introduction of new hardware like GPGPUs , FPGAs, used as co-processors for specialised tasks.