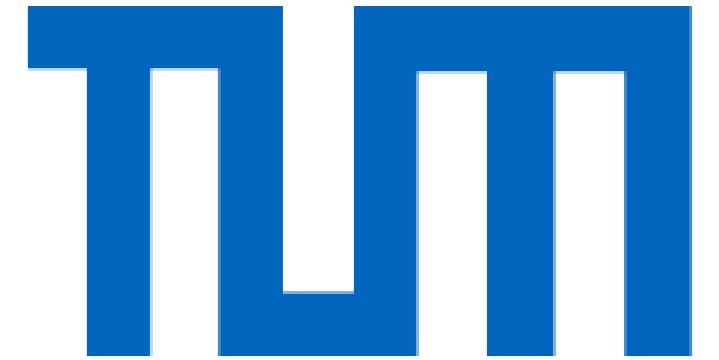




# The intelligent, FPGA-based event builder and Data Acquisition System (iFDAQ) of COMPASS

– an exemplary system for the future?

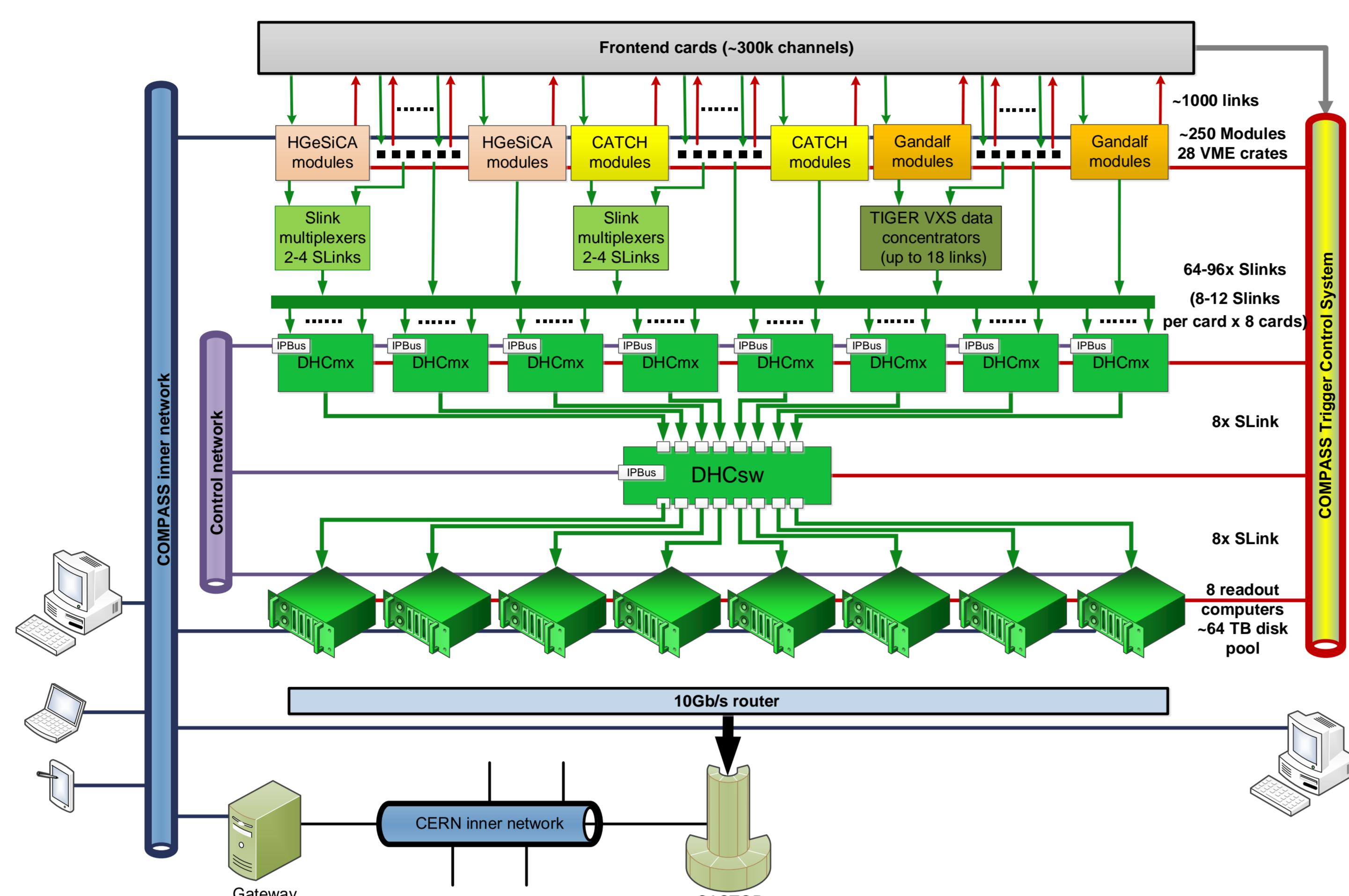


D. Steffen<sup>a</sup>, I. Konorov<sup>b</sup>, J. Novy<sup>c</sup>, O. Subrt<sup>a</sup>, M. Bodlak<sup>d</sup>, Y. Bai<sup>b</sup>, V. Frolov<sup>e</sup>,  
V. Jary<sup>c</sup>, S. Huber<sup>b</sup>, D. Levit<sup>b</sup>, M. Virius<sup>c</sup>

(a) CERN, Genève, Switzerland, (b) Technische Universität München, Germany  
(c) Czech Technical University, Czech Republic, (d) Charles University, Czech Republic  
(e) Joint Inst. For Nuclear Research, Russia

**TIME**

## iFDAQ and Hardware Event Builder



present status

## Data Handling Card (DHC)

**form factor:**  $\mu$ TCA / AMC standard  
6U VME carrier card

**FPGA:** Xilinx Virtex6

**memory:** 4GB DDR3 SDRAM

- DHCmx (12:1 multiplexer)
- DHCsw (8x8 switch)
- DHCsb (PCIe spillbuffer)



DHC on VME carrier Card as used for DHCmx and DHCsw

- TCS (Trigger Control System)
- 1 Gb Ethernet control network (IPbus)
- 16 serial data links (SLINK)
- PCIe (for spillbuffer)



**throughput:** 3 GB/s as DHCsw

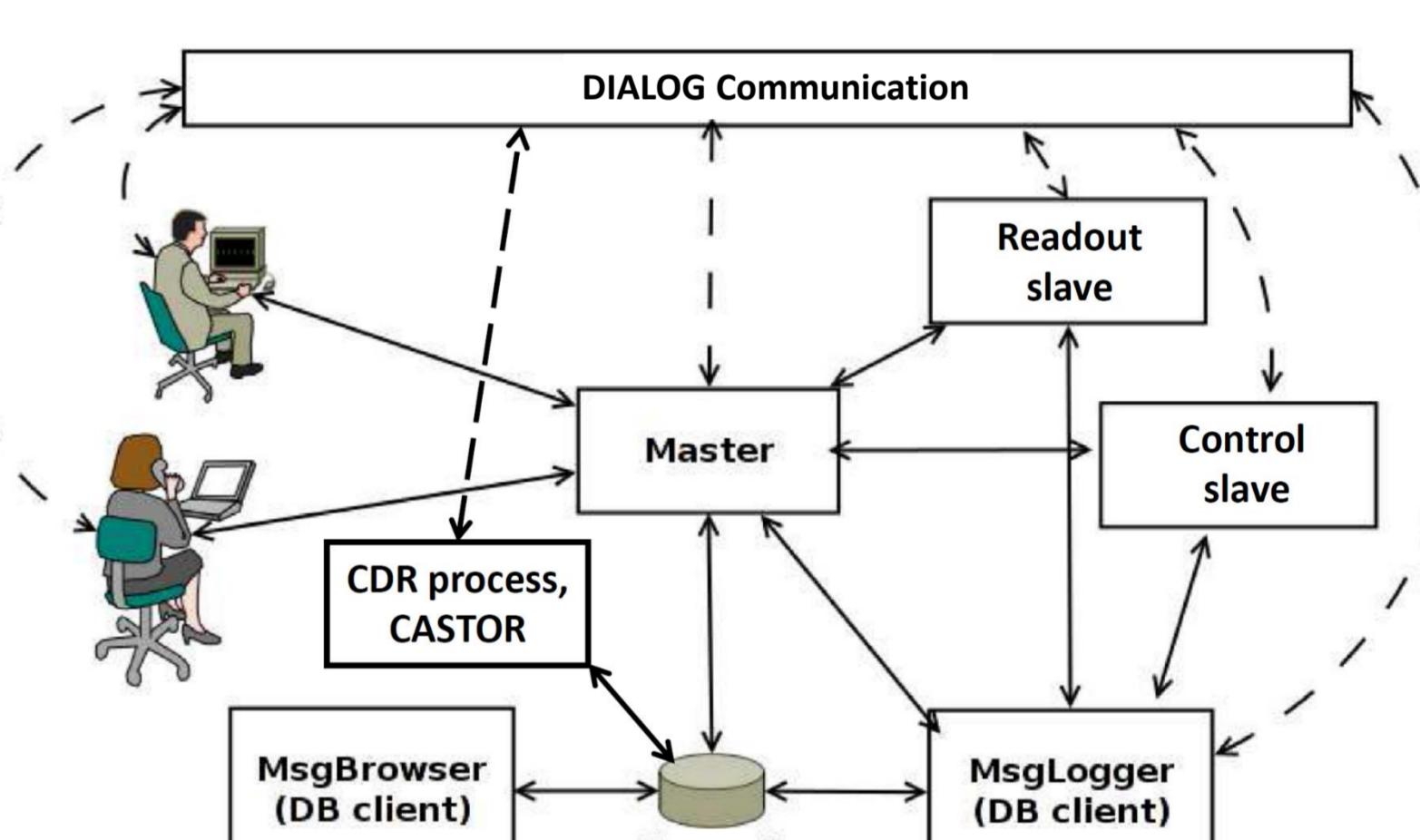
## iFDAQ - Properties

- On-spill data rate: 1.5 GB/s
- Buffering on all levels of event building  
↳ 500 MB/s sustained rate
- 3 independent interfaces:
  - Time distribution (TCS)
  - Data flow (SLINK)
  - Slow control (IPbus)

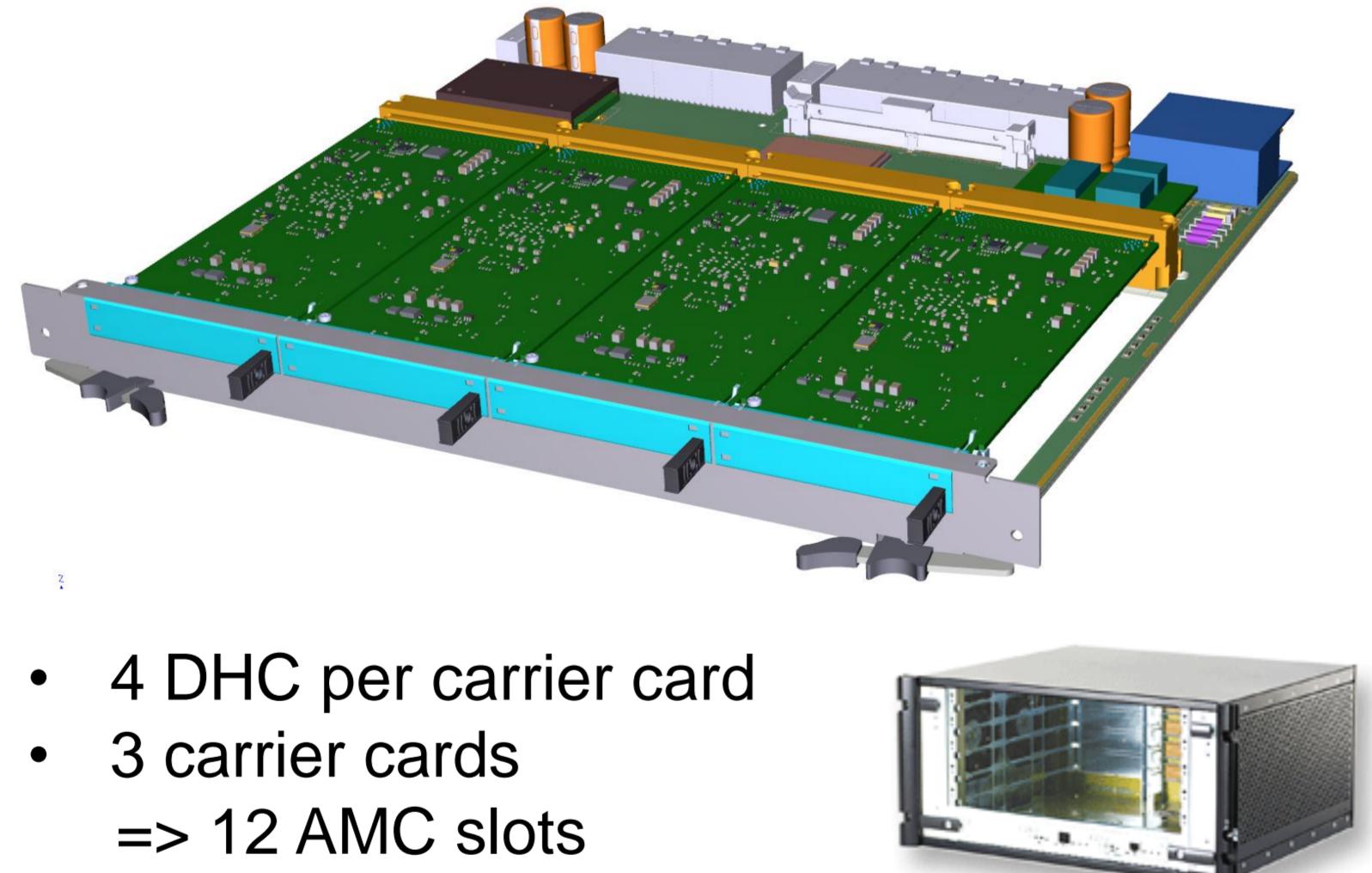
- Initial intelligence:**
- Automatic resynchronization of FE modules
  - Data check/FE-error handling
    - Data throttling
    - Replacing missing/defective frames by empty frames
  - Self-synchronized event building data flow

- Control of DAQ configuration through web and C++ GUI
- Multithreaded event processing and error detection
- DAQ status monitoring and system overview

## RCCAR-Software functionality



## ATCA standard



near future

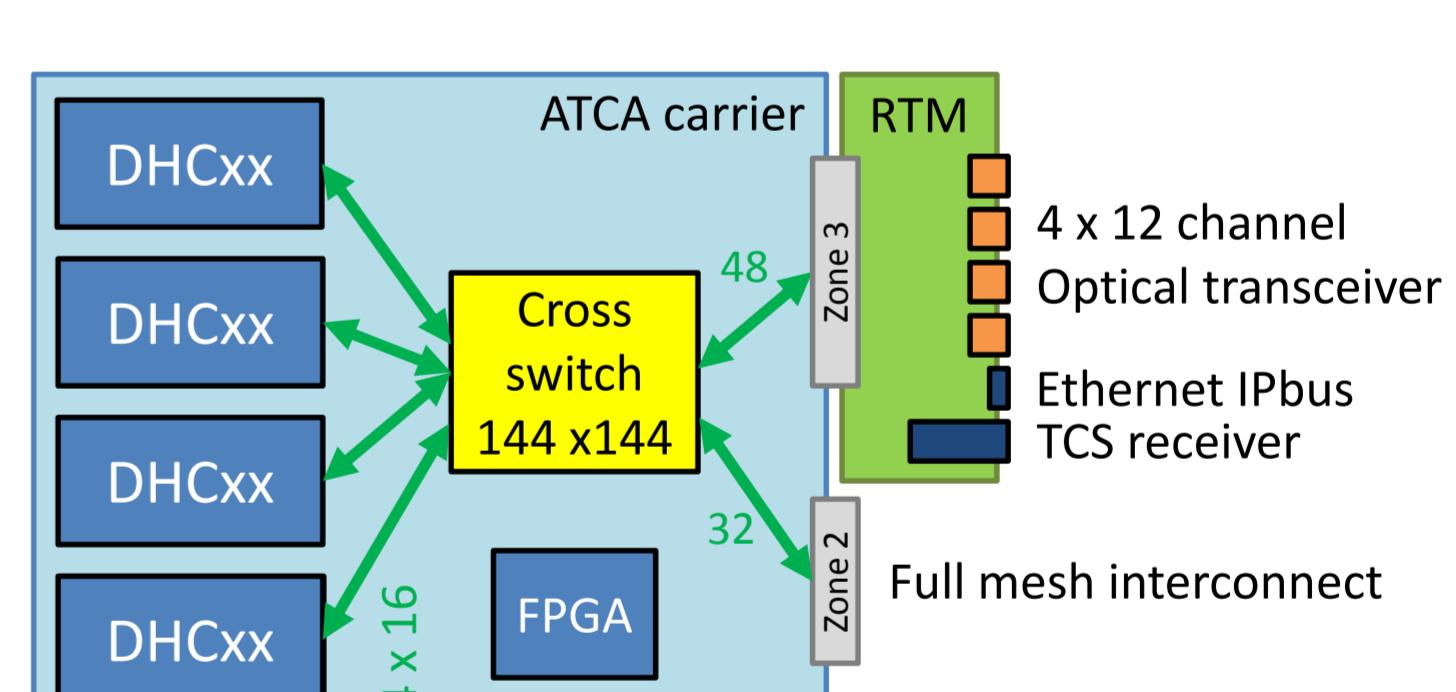
## Upgrade Time Distribution System

- Bidirectional PON (Passive Optical Network)  
16x16 topology
- UCF protocol (Universal Communication Framework)
  - Receiving node status information
  - Synchronous node configuration (topology reconfiguration)
  - IPbus protocol for Slow Control

### Extended intelligence:

- Automatic recognition and compensation for hardware failure
- Automatic load balancing
- Continuously running DAQ

## Crosspoint Switch

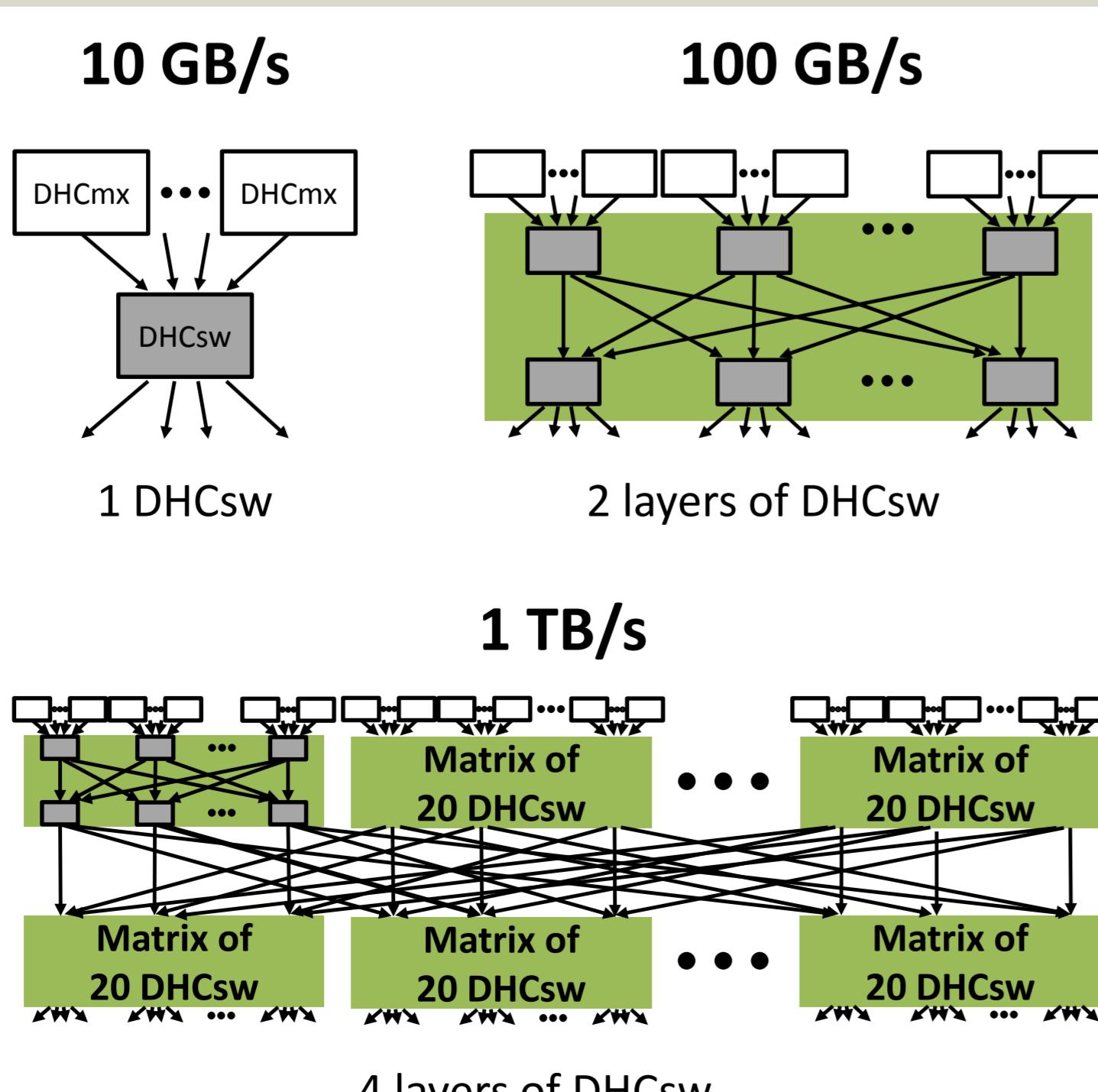


- crosspoint switch:** Vitesse – VSC3144-02  
**FPGA:** Xilinx Artix-7
- fully programmable
  - cross switch control and monitoring
  - Hub to AMC modules

End of COMPASS Scale

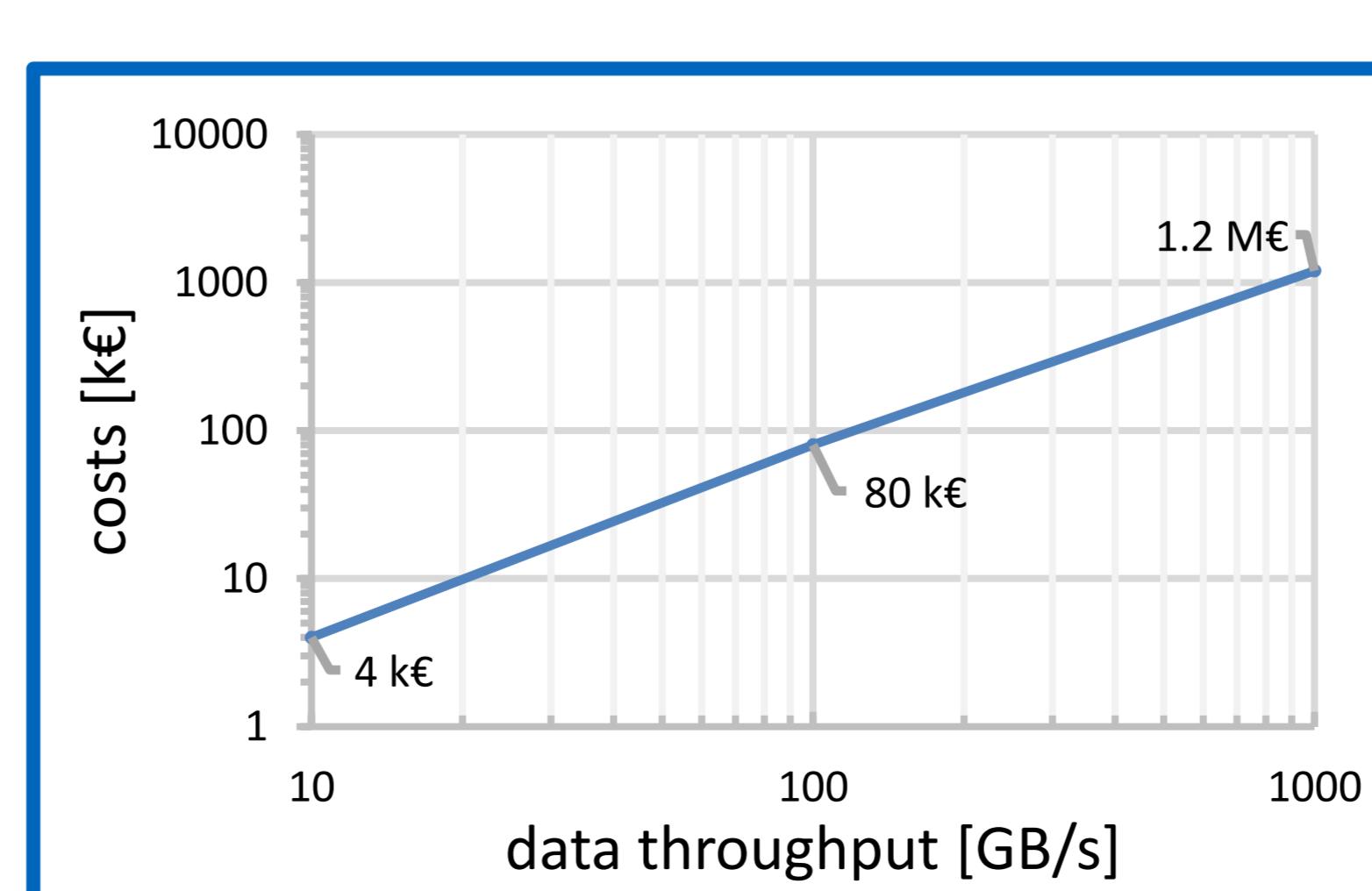
far future

## Scaling Possibility



### Scenario for:

- Xilinx 7-series FPGA
- SLINK interfaces replaced by Aurora



## Software

- Example event for automatic evaluation of DAQ topology and configuration
- Machine learning algorithm for data quality monitoring

## Supported by

