Preliminary Experimental Results of A 14-bit Split-SAR ADC for ATLAS LAr Phase-II Upgrade

Hongda Xu¹, Yongda Cai¹, Ling Du², Datao Gong², and Yun Chiu¹
1 Department of Electrical Engineering, University of Texas at Dallas, Richardson, TX, USA
2 Department of Physics, Southern Methodist University, Dallas, TX, USA

Background and Motivations

ADC Specs for Phase-II LAr Readout

- High resolution: 12-14 bits
- High speed: 40-80 MS/s
- Low power, low area
- Radiation-tolerant
- Pipelined ADC: High-gain residue amplifier hard to scale w/ process
- SAR ADC: low-power, low-area is a strong candidate for Phase-II

Previous TID Results (TWEP®14)

- 12-bit, 160 MS/s ADC in 40-nm CMOS
- Total radiation dose up to 1 Mrad
- No significant degradation on SNDR, SFDR

Split SAR Architecture

- Split ADC and architectural redundancy
- From best case to worst case: 9 bits vs. 16 bits
- If ΔD is large, choose the output of the ADC that is not hit
- A 3-dB SNR gain with normal operation (i.e., no hit)
- Two-step pipelined structure
- Fewer number of bits in first stage
- Amplifier removed from SAR Loop

Single-Event-Effect (SEE) Protection

- Summing-Node Hit Detection
- 2nd Stage SAR Error Detection
- Data-Latch Error Detection

- SEE detector is formed by a pair of resistors, a “substrate-current amplifier”, and some digital logics.

Example

For C_{ox} = 100 fF and C_{T2D} = 2 pF, V_{H} = 50 mV !

Preliminary Electrical Measurement Results

- Super-radix-2 issue

Due to a layout error, the SAR capacitor array in the first stage suffered a large mismatch error, resulting in a super-binary weight for the most significant bit (MSB).

- FIB Surgery

Focused ion beam (FIB) surgery is performed to reduce the MSB capacitor size by cutting the MOM capacitor fingers.

- Single Channel Measured Performances

- Over 97-dB SFDR and 74.5-dB SNDR (ENOB = 12.1 bits) are measured after FIB at 10 MHz input for a sample rate of 40 MSPS.

- Region 1: At low input frequency, it is likely limited by the input network on the PCB (balun etc.)
- Region 2: At high input frequency, it is likely limited by clock jitter.