# xTCA Developments at Technical University of Lodz

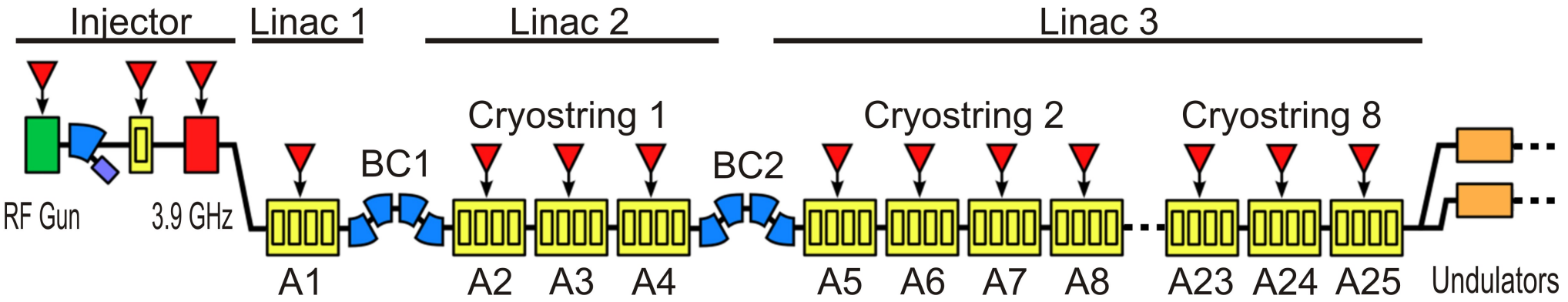
**Dariusz Makowski**

10th meeting of the xTCA interest group
10 March 2016, CERN

# Agenda

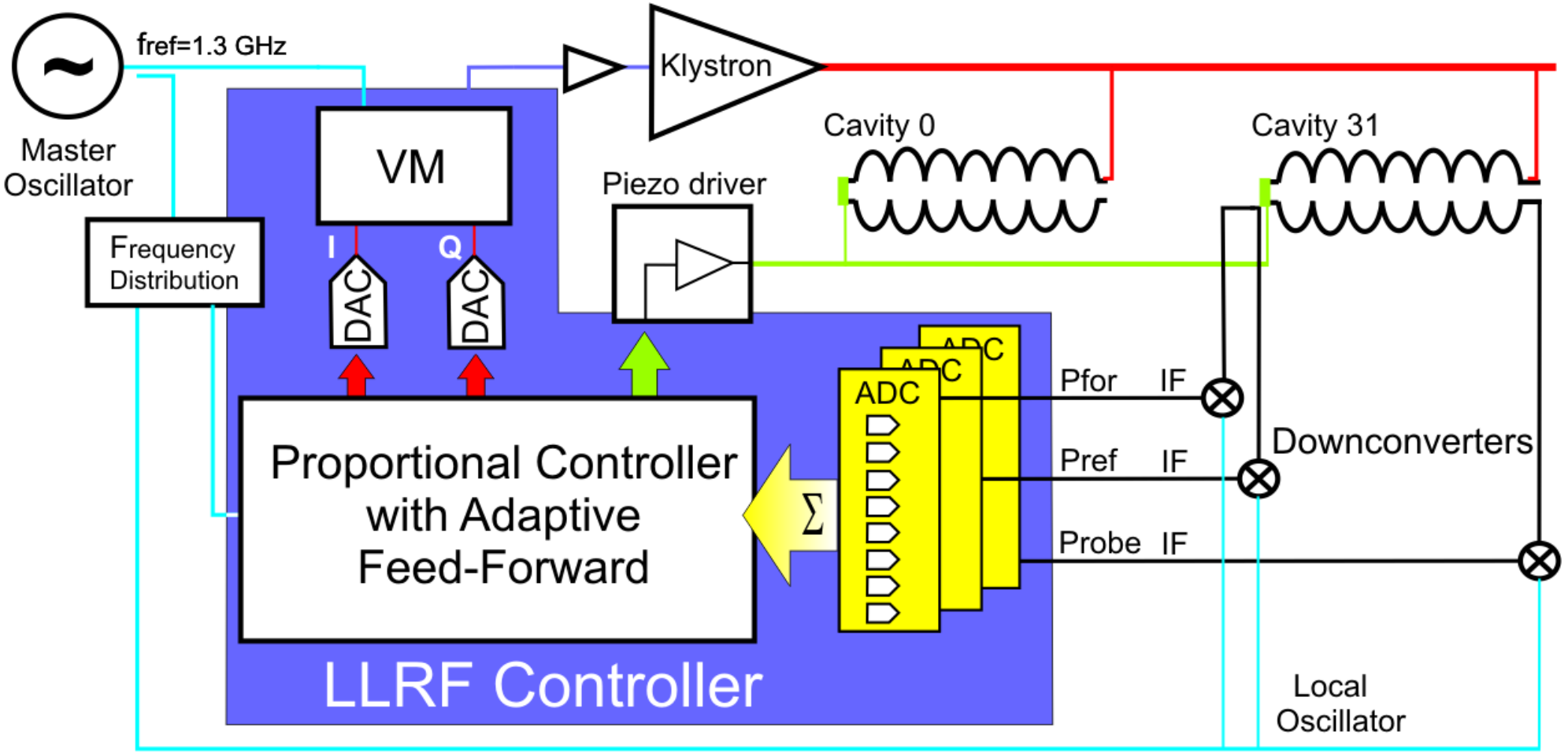
- European XFEL and LLRF System
- First Approach
- New Standard – New Possibilities
- MTCA.4-based LLRF Control System
- Image Acquisition System

# European X-ray Free Electron Laser at DESY



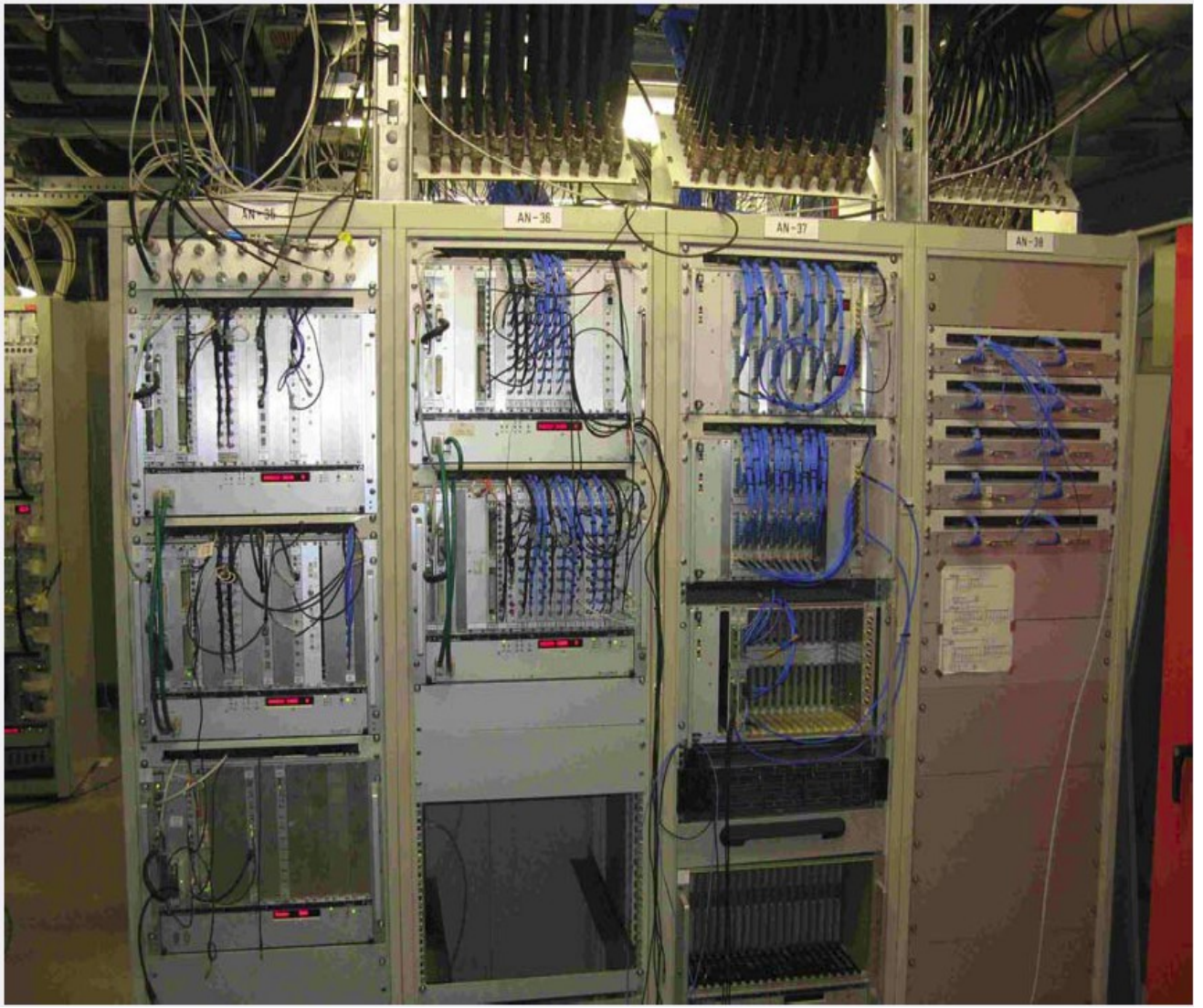

- EXFEL is composed of 800 super-conducting cavities
- Installed in 100 cryo-modules
- LLRF system is controlled by 25 RF stations (A1-A25)
- Requirements for stability:
  - <0.01% amplitude
  - <0.01° phase at 1.3 GHz
- Requires high availability
  - Looking for a new standard for LLRF system

# LLRF System for EXFEL Accelerator



# LLRF at DESY

- VME standard:
  - Old standard ('81)
  - Control 8 cavites
  - Lack of diagnostics and and management
  - Expensive CPU
  - Limited resources
  - Limited connectivity
  - ...




Courtesy of S. Simrock

# Comparison of Selected Standards

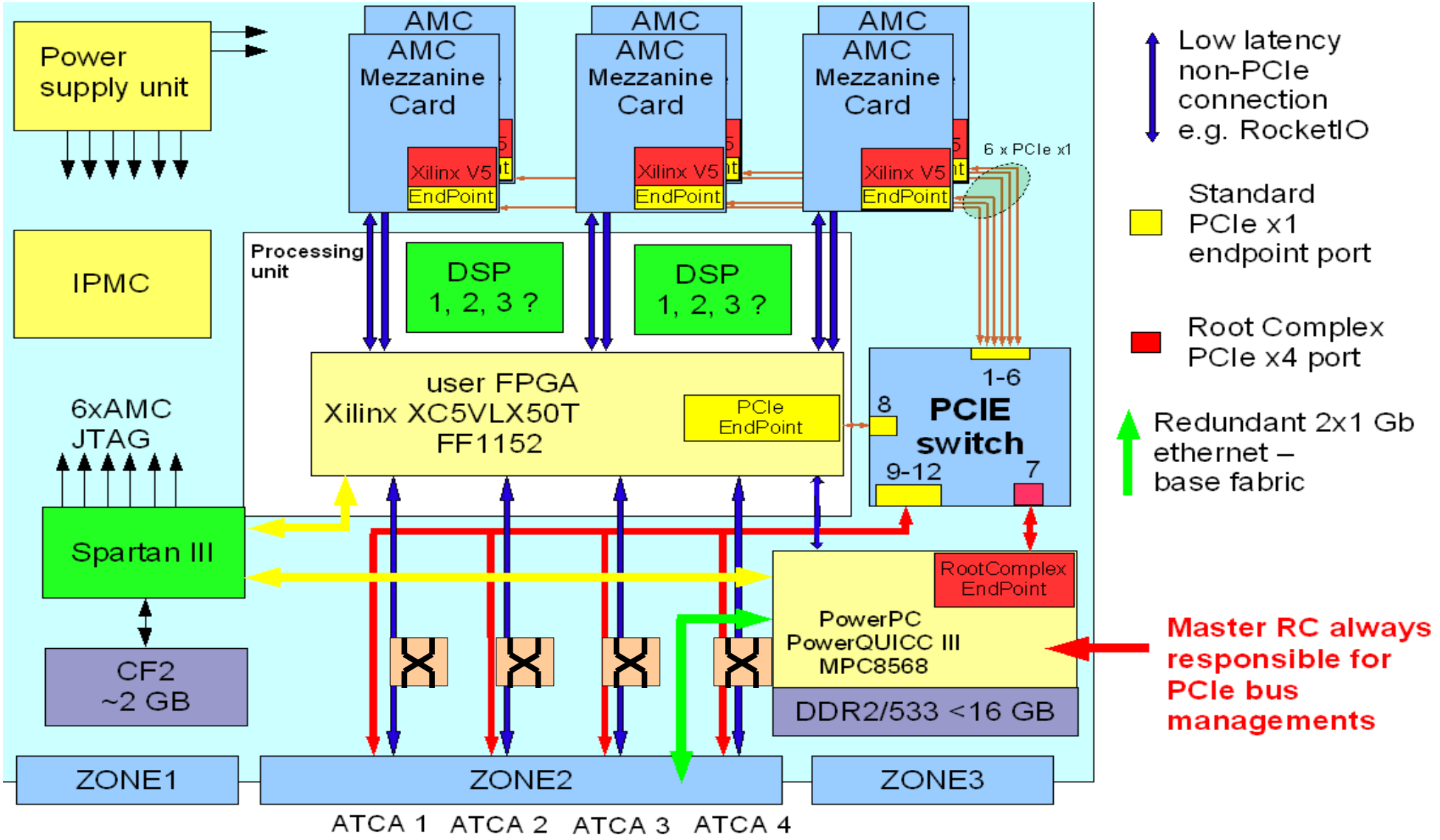
VME chassis

ATCA chassis

MTCA chassis

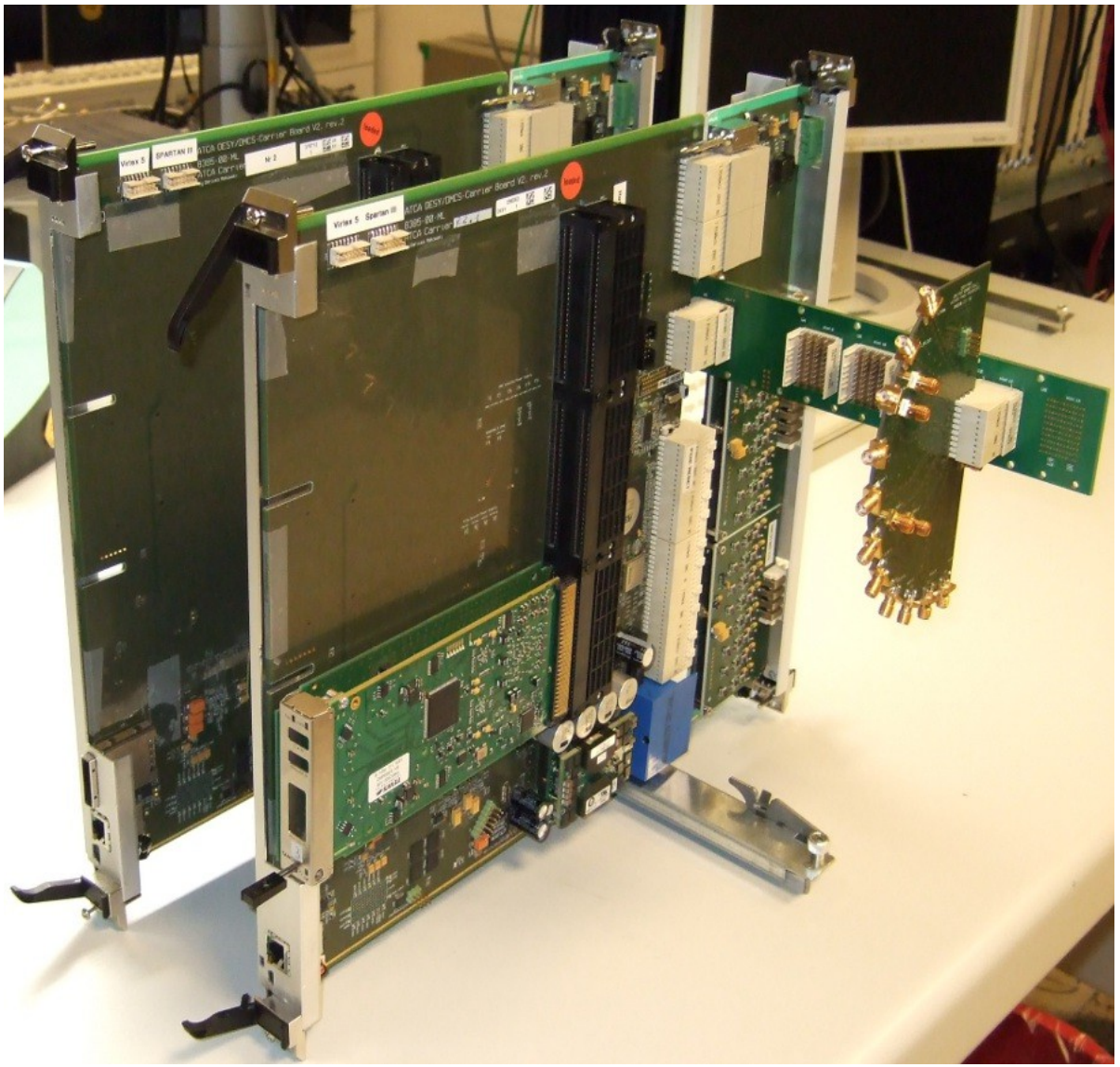
Need more info
– see our lab

# Carrier Board for LLRF System



# ...and Final Product

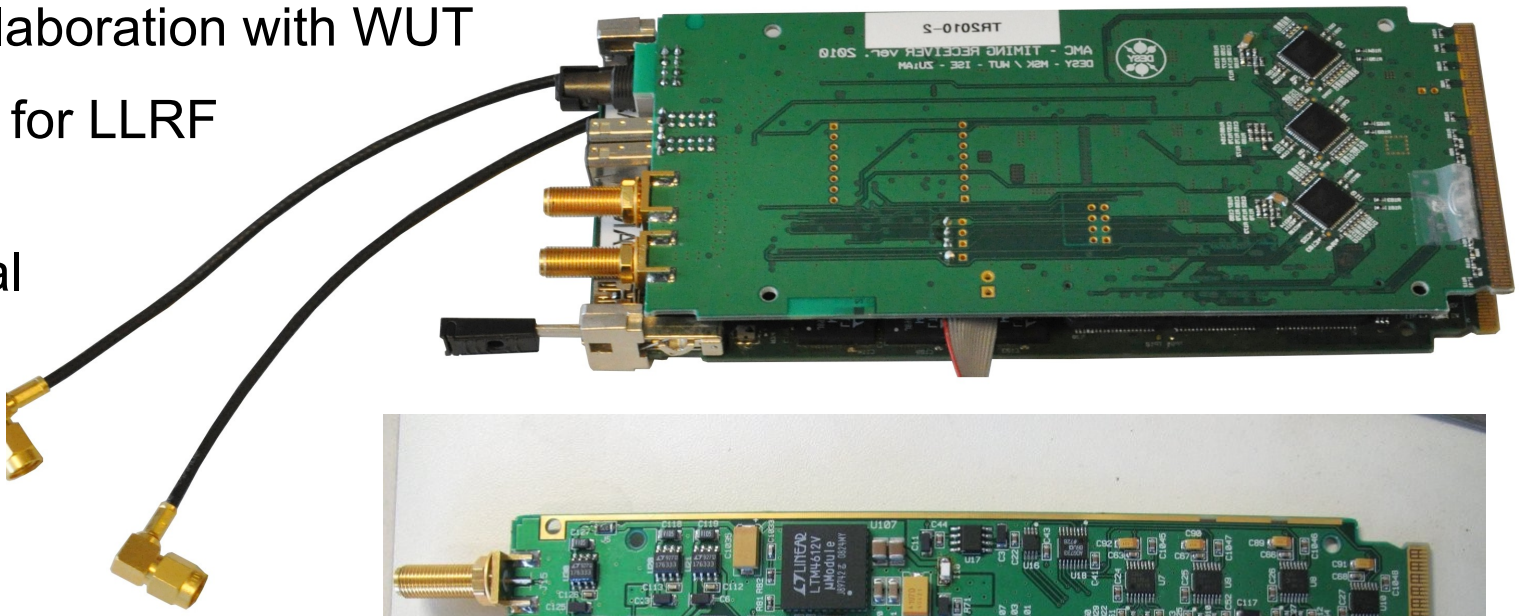
- Provides processing power for LLRF algorithms
- Provides accommodation for LLRF components
  - Down converters
  - Digitizers
  - Vector Modulator
  - Timing, synchronisation
  - Protection (interlocks)
- Only 3 AMC slots
- PCIe switch, Virtex 5 FPGA, TigerShark DSP, RAM
- Management - IPMC
- All connectivity on backplane
- Very poor quality of RF signals



# Vector Modulator and Timing Module

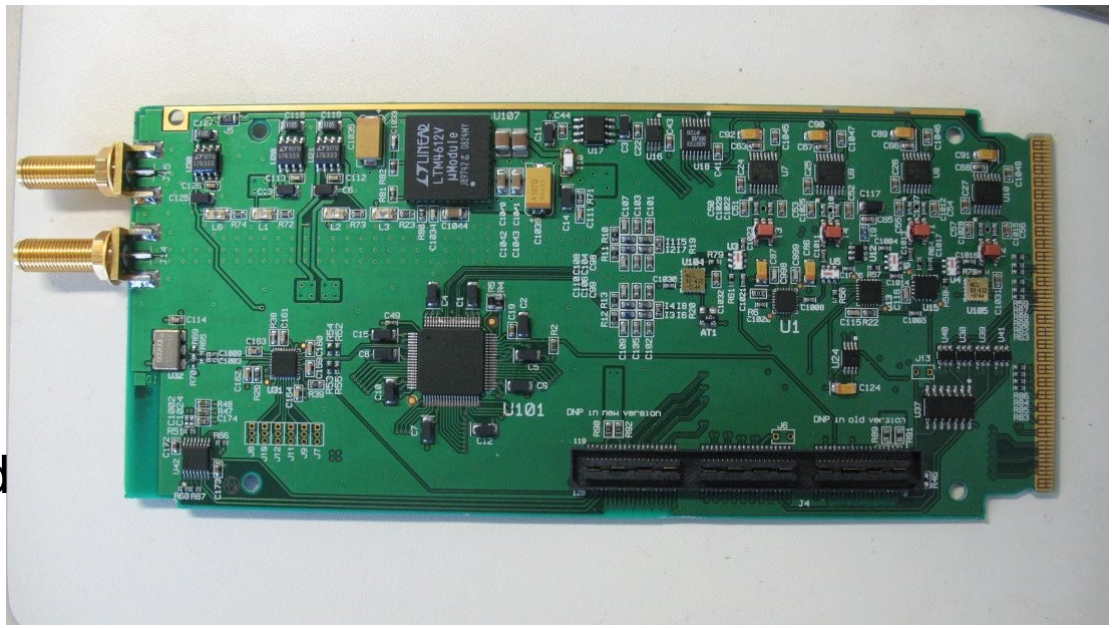
## Timing module

- Designed with collaboration with WUT
- Provide reference for LLRF hardware
- Receive MO signal and generate 3 frequencies



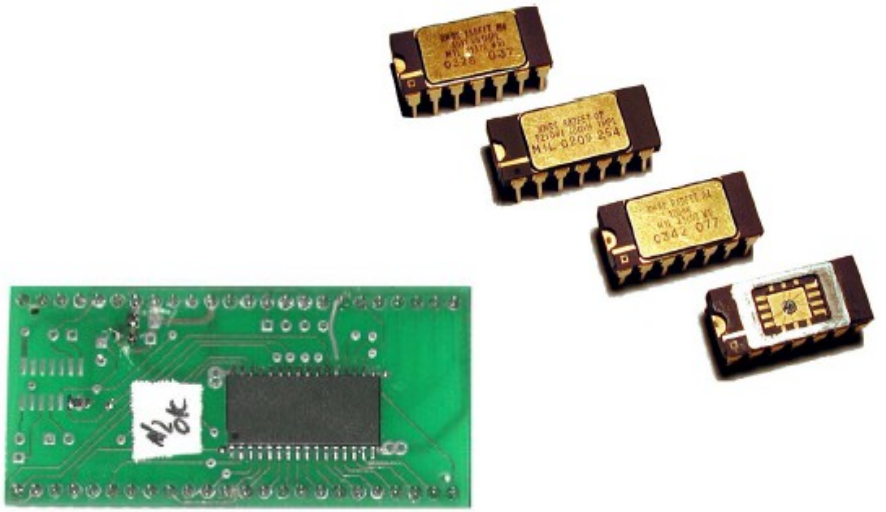
## Vector Modulator

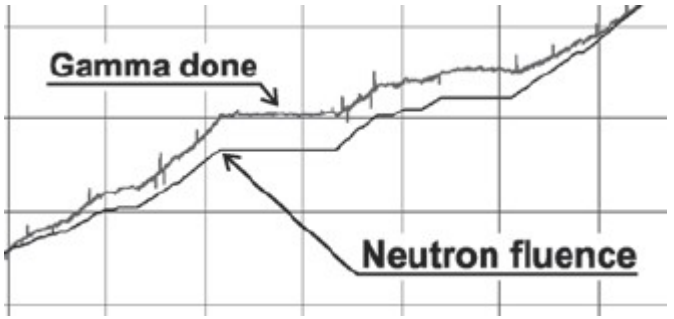
- Designed with collaboration with WUT
- Modulates RF signal from MO and generates signal for klystron
- Single RF channel



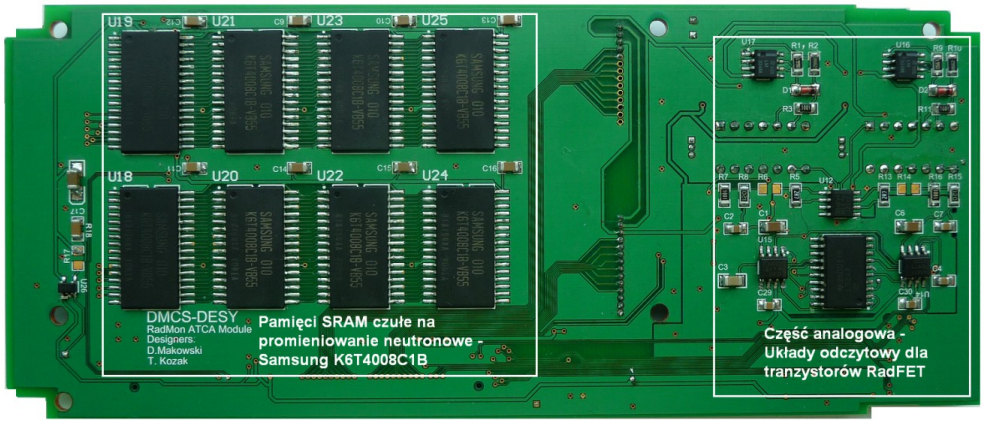
# Radiation Monitoring Module

- Measures neutron fluence and gamma dose
- SRAM-based sensor for neutron fluence
- RadFET (Tyndall) dosimeter for gamma dose measurement






| Calibration factor | SRAM | RadFET |
|---|---|---|
| Neutron fluence | $1.85 \times 10^4$ n cm$^{-2}$/SEU | – |
| Silicon kerma | $1.17 \times 10^{-3}$ Gy(Si)/SEU | – |
| Gamma dose | – | 46.3 mV/ Gy($SiO_2$) |



# New Standard – New Possibilities

MicroTCA™

PICMG® Specification MTCA.4
R 1.0 Draft 0.9xi

## MicroTCA Enhancements for Rear I/O and Precision Timing

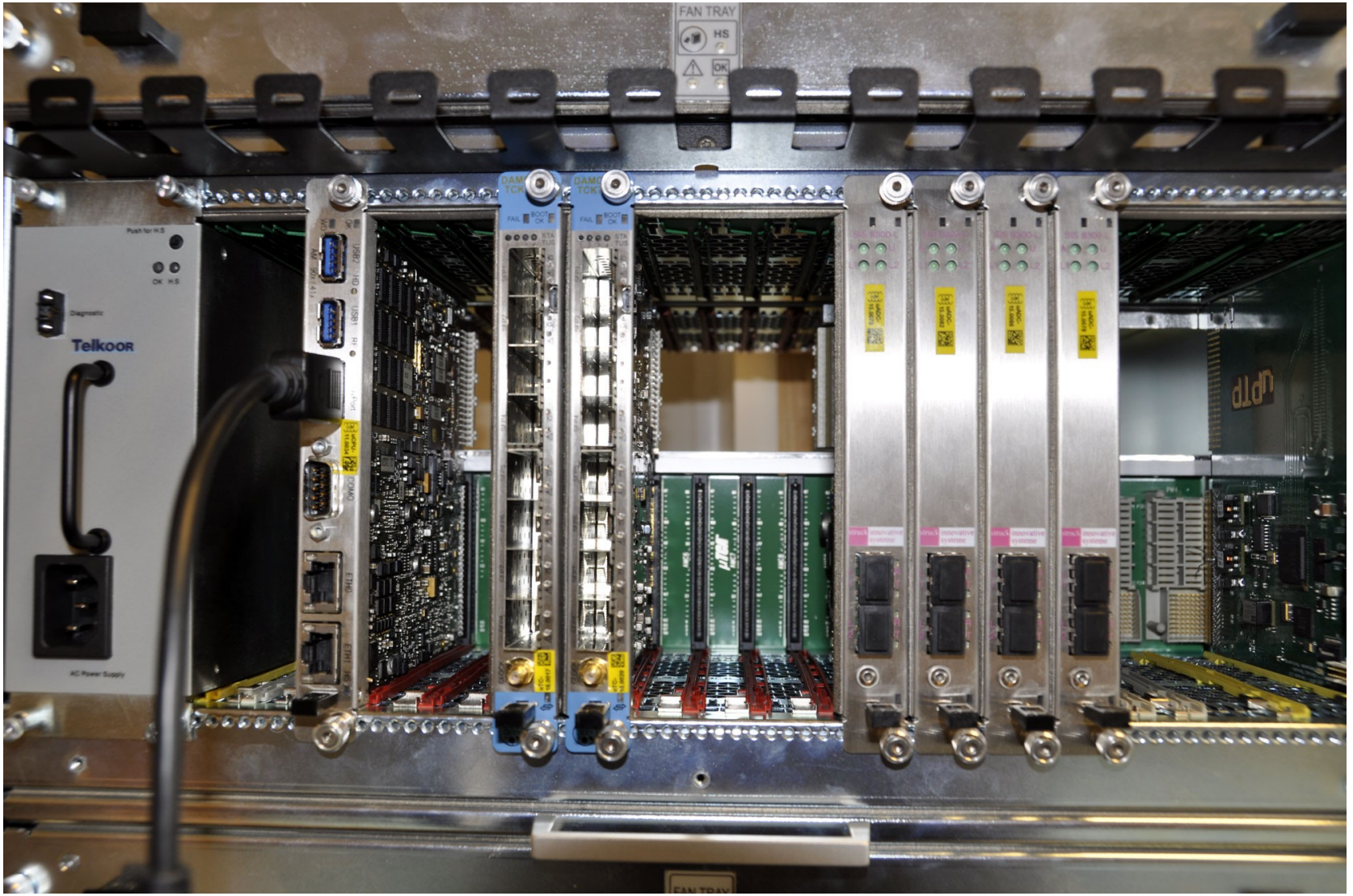
18 July 2011

For Member Review Only - Do Not Claim Compliance To or Distribute This Draft Specification

PICMG®
Open Modular Computing Specifications

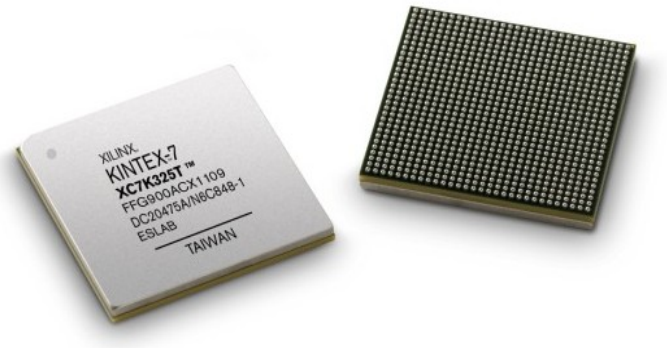
µTCA®

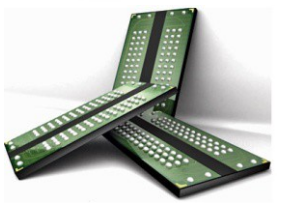
# MTCA.4 Chassis with AMC modules



# LLRF Controller Module - Requirements

- Provides computation power for LLRF algorithms
- Provides interface to VM, diagnostics, management
- **Module Requirements:**
  - PCIe - main parameters of the computation module, latency <50 us, throughput ~16 Gbps
  - LLL - data from DAQ modules and to Vector Modulator, latency <200 ns, throughput >6 Gbps
  - Optical connection for communication with other LLRF subsystems (master-slave system, LFD compensation, BAMs, etc...), latency <200 ns, throughput >6 Gbps
- Trigger and interlock signals provided on backplane
- Compliant with PICMG MTCA.4 specification
- Module management, diagnostics, high availability

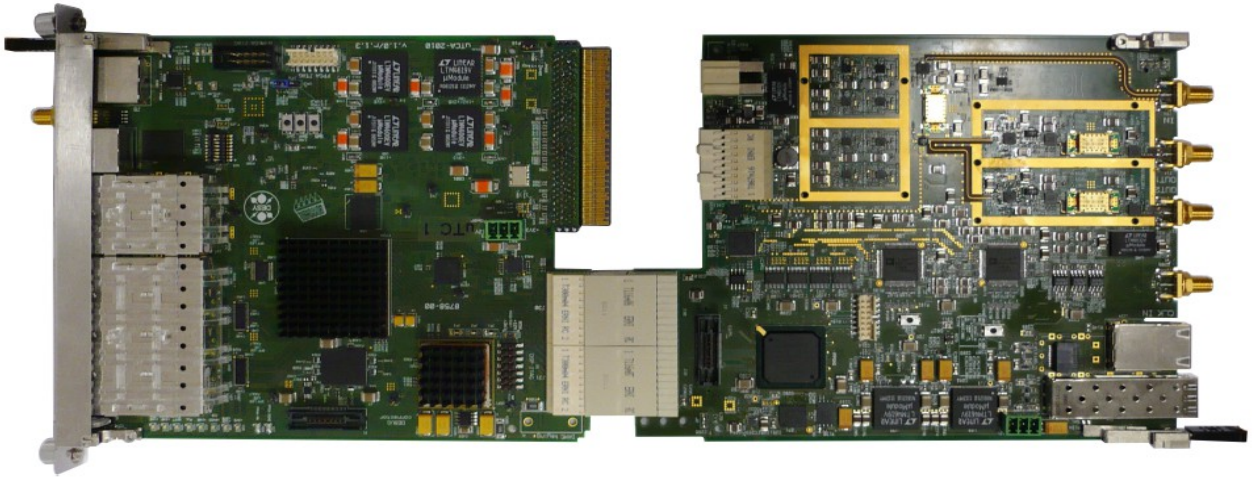


µTCA® RoHS COMPLIANT Pb Pb-Free Zone 3 Class D1.2 XILINX READY TO LICENSE DESY

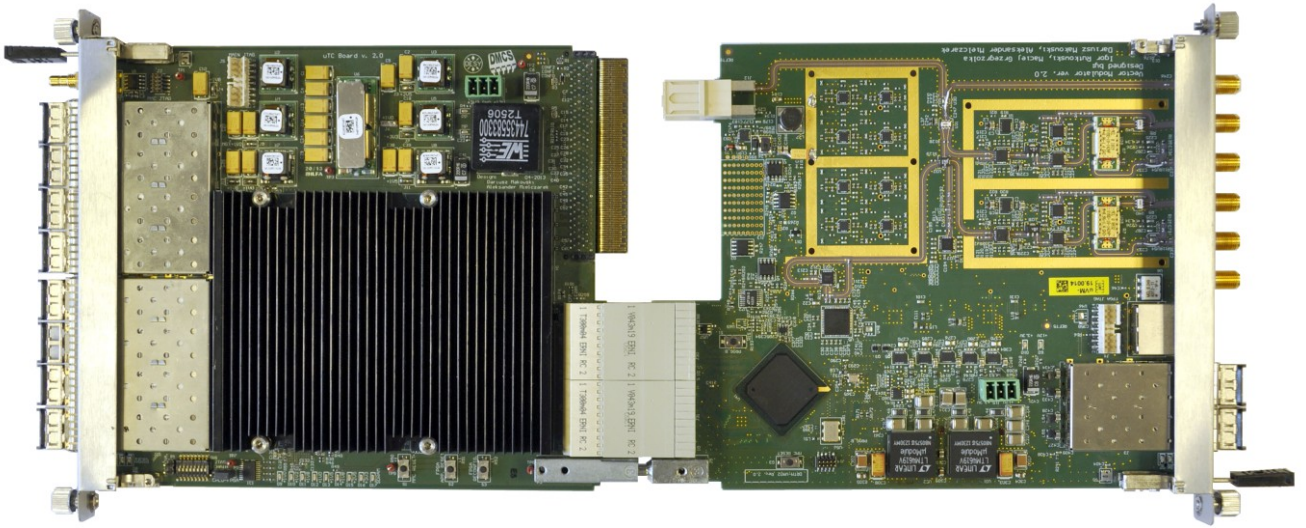
# LLRF Controller with Vector Modulator

**Virtex 5 SVX95T**

LLRF Controller (left) and Vector Modulator (right), version 1.0

**Kintex 7 XC7K355T**

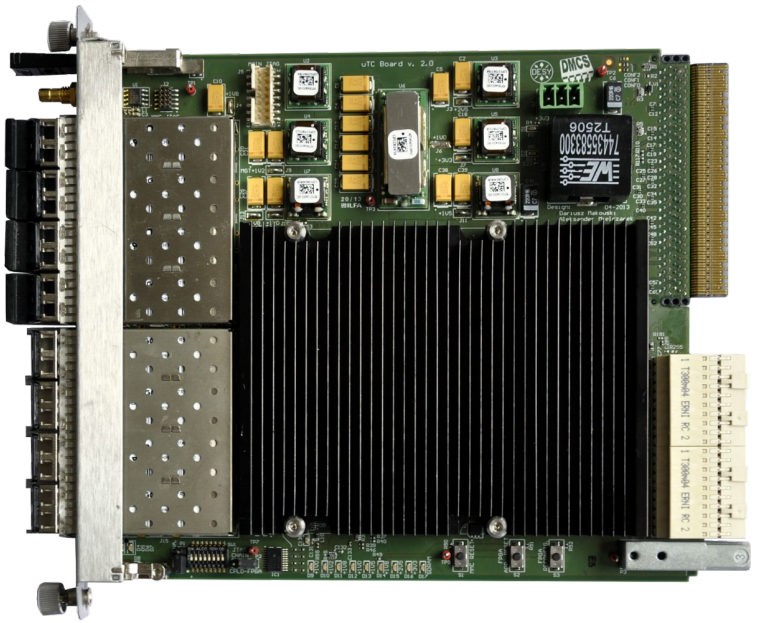



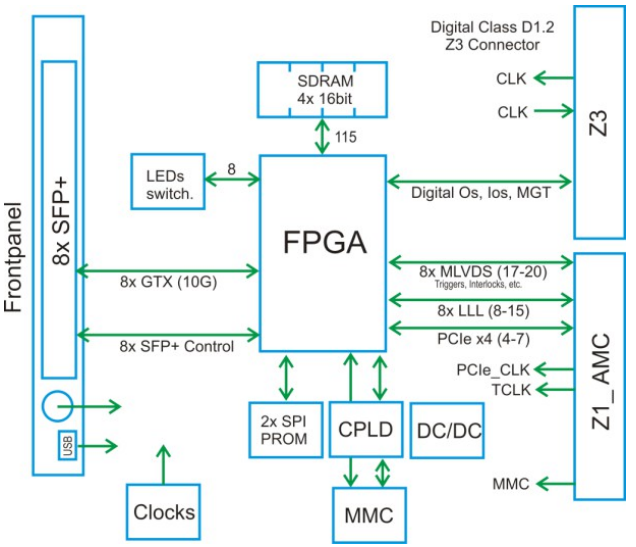
LLRF Controller (left) and Vector Modulator (right), version 2.0

# DAMC-TCK7 – Signal Processing Module, ver. 2

**Features:**

- Xilinx Kintex 7 XC7K355T/XC7K420T FPGA
- SDRAM: 16 Gb DDR3 SDRAM@533 MHz
- Connectivity:
  - 24 or 28 gigalinks, data rate max. 12.5 Gbps
  - PCIe x4, gen. 3 (32 Gbps)
  - Low-latency links:
    - Backplane: 10x 10 Gbps
    - Front panel: 8x 12.5 Gbps (SFP+)
    - Zone 3: D1.2 Digital Class (4x 10 Gbps)
- Flexible clock distribution and synchronization
- IPMI management and diagnostics
- FPGA firmware upgrade support
- Modules now available from Vadatech (CM045)





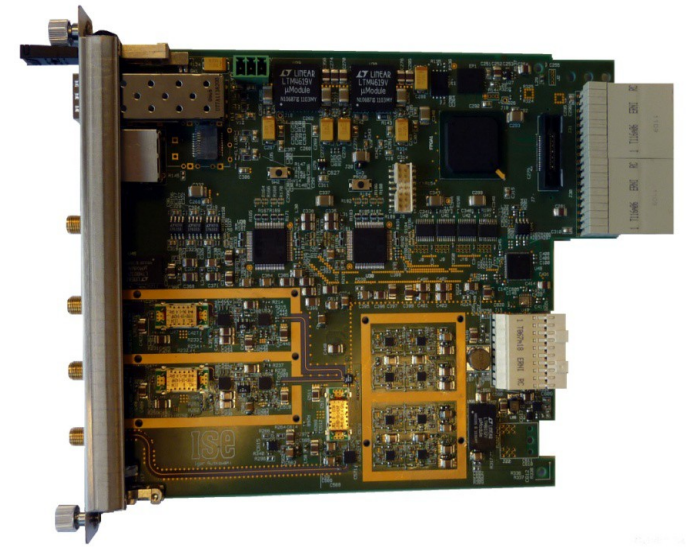
# DRTM-VM2 – Vector Modulator, ver. 1

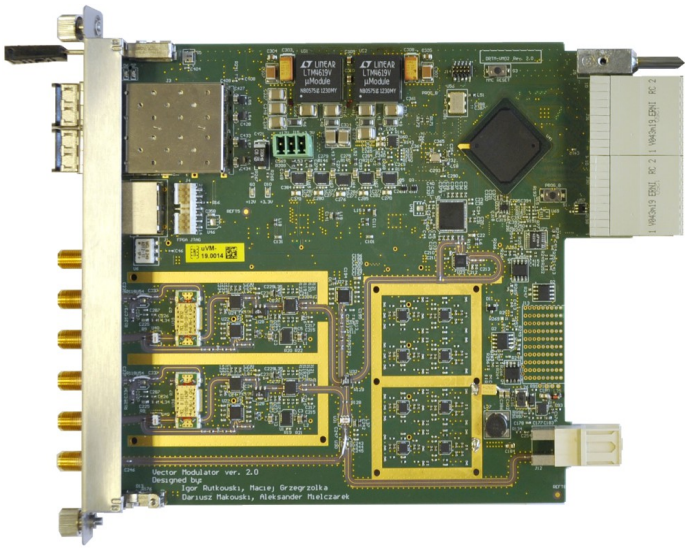
## Version 1

- No standardized Zone 3 connector
- Limited clock distribution
- Old version of RF backplane connectivity
- IPMI controller not compliant with MTCA.4

## Version 2

- Frequency range: 1-6 GHz (L and S-band)
- Better linearity, lower phase noise floor
- Improved reference power signal distribution scheme
- 16-bit, 160 MSps DACs
- Improved Interlock scheme
- Improved clock distribution circuit
- Power diagnostics
- RF backplane support

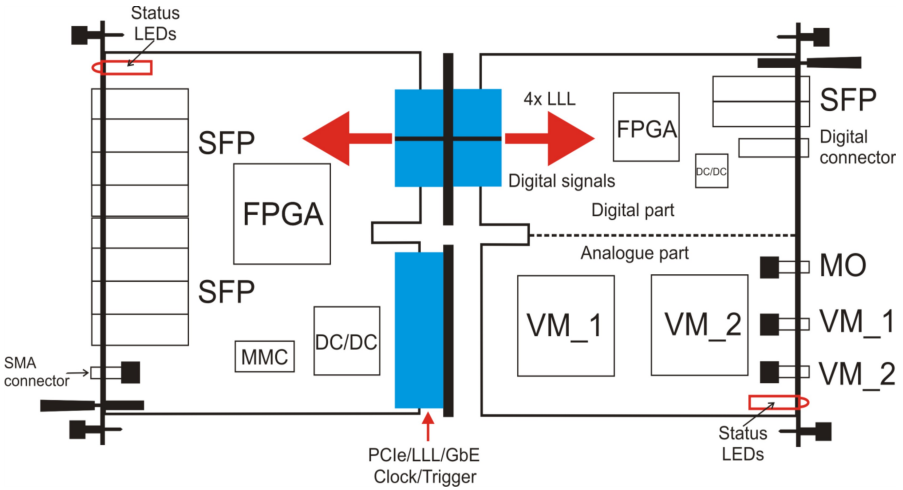




Designed with collaboration with WUT

# Zone 3 Connection – Should We Have Standard?

- Zone 3 connectivity was not standardised by MTCA.4 spec.
- Zone 3 – Proposed: Class A1.x and D1.x
- Simple vs Complex E-keying
- Software E-keying should be developed (...in progress)




| | a | b | c | d | e | f |
|---|---|---|---|---|---|---|
| 1 | PWR+12V | PWR+12V | PS# | AMC_SDA | RTM_TCK | RTM_TDO |
| 2 | PWR+12V | PWR+12V | MP+3.3V | AMC_SCL | RTM_TDI | RTM_TMS |
| 3 | SFP1-TX+ | SFP1-TX- | SFP_AMC_CLK+ | SFP_AMC_CLK- | SFP2-TX+ | SFP2-TX- |
| 4 | SFP1-RX+ | SFP1-RX- | SFP_RTM_CLK+ | SFP_RTM_CLK- | SFP2-RX+ | SFP2-RX- |
| 5 | INTERLOCK 1 | INTERLOCK 2 | P30_IO+ | P30_IO- | P30_IO+ | P30_IO- |
| 6 | P30_IO+ | P30_IO- | P30_IO+ | P30_IO- | P30_IO+ | P30_IO- |
| 7 | P30_IO+ | P30_IO- | P30_IO+ | P30_IO- | P30_IO+ | P30_IO- |
| 8 | AMC_CLK1+ | AMC_CLK1- | AMC_CLK2+ | AMC_CLK2- | AMC_CLK3+ | AMC_CLK3- |
| 9 | RTM_CLK1+ | RTM_CLK1- | RTM_CLK2+ | RTM_CLK2- | RTM_CLK3+ | RTM_CLK3- |
| 10 | P30_IO+ | P30_IO- | P30_IO+ | P30_IO- | P30_IO+ | P30_IO- |
| | | | | | | |
| 1 | P31_IO+ | P31_IO- | P31_IO+ | P31_IO- | P31_IO+ | P31_IO- |
| 2 | P31_IO+ | P31_IO- | P31_IO+ | P31_IO- | P31_IO+ | P31_IO- |
| 3 | P31_IO+ | P31_IO- | P31_IO+ | P31_IO- | P31_IO+ | P31_IO- |
| 4 | P31_IO+ | P31_IO- | P31_IO+ | P31_IO- | P31_IO+ | P31_IO- |
| 5 | P31_IO+ | P31_IO- | P31_IO+ | P31_IO- | P31_IO+ | P31_IO- |
| 6 | P31_IO+ | P31_IO- | P31_IO+ | P31_IO- | P31_IO+ | P31_IO- |
| 7 | P31_IO+ | P31_IO- | P31_IO+ | P31_IO- | P31_IO+ | P31_IO- |
| 8 | P31_IO+ | P31_IO- | P31_IO+ | P31_IO- | P31_IO+ | P31_IO- |
| 9 | P31_IO+ | P31_IO- | P31_IO+ | P31_IO- | P31_IO+ | P31_IO- |
| 10 | P31_IO+ | P31_IO- | P31_IO+ | P31_IO- | P31_IO+ | P31_IO- |

# Deliverables: Analog and Digital Classes

## Digital Class D1.2

| Class D1.2 / Zone | | | a | b | c | d | e | f |
|---|---|---|---|---|---|---|---|---|
| MTCA.4 management | J30 | 1 | PWRA1 | PWRB1 | PS# | SDA | TCK | TDO |
| | | 2 | PWRA2 | PWRB2 | MP | SCL | TDI | TMS |
| Digital clocks fixed I/O | | 3 | AMC_CLK1+ | AMC_CLK1- | RTM_CLK1+ | RTM_CLK1- | OUT2+ | OUT2- |
| | | 4 | AMC_TCLK+ | AMC_TCLK- | OUT0+ | OUT0- | OUT1+ | OUT1- |
| User -configuration | | 5 | P30_IO+ / CC * | P30_IO+ / CC * | P30_IO+ | P30_IO- | P30_IO+ | P30_IO- |
| | | 6 | P30_IO+ / CC * | P30_IO+ / CC * | P30_IO+ | P30_IO- | P30_IO+ | P30_IO- |
| | | 7 | P30_IO+ | P30_IO- | P30_IO+ | P30_IO- | P30_IO+ / CC | P30_IO+ / CC |
| | | 8 | P30_IO+ | P30_IO- | P30_IO+ | P30_IO- | P30_IO+ / CC | P30_IO+ / CC |
| | | 9 | P30_IO+ / CC* | P30_IO+ / CC* | P30_IO+ | P30_IO- | P30_IO+ | P30_IO- |
| | | 10 | P30_IO+ / CC* | P30_IO+ / CC* | P30_IO+ | P30_IO- | P30_IO+ | P30_IO- |
| | | | | | | | | |
| | J31 | 1 | P31_IO+ | P31_IO- | P31_IO+ | P31_IO- | P31_IO+ | P31_IO- |
| | | 2 | P31_IO+ | P31_IO- | P31_IO+ | P31_IO- | P31_IO+ | P31_IO- |

## Analog Class A1.1

| Class A1.1 / Zone | | | a | b | c | d | e | f |
|---|---|---|---|---|---|---|---|---|
| MTCA.4 management | J30 | 1 | PWRA1 | PWRB1 | PS# | SDA | TCK | TDO |
| | | 2 | PWRA2 | PWRB2 | MP | SCL | TDI | TMS |
| Standard Gbit-Link | | 3 | SFP-CLK+ | SFP-CLK- | SFP-RX+ | SFP-RX- | SFP-TX+ | SFP-TX- |
| User-configuration | | 4 | D3+ | D3- | D4+ | D4- | D5+ | D5- |
| | | 5 | D6+ | D6- | D7+ | D7- | D8+ | D8- |
| Digital fixed I/O | | 6 | AMC_TCLK+ | AMC_TCLK- | OUT0+ | OUT0- | OUT1+ | OUT1- |
| Shielding | | 7 | gnd | gnd | gnd | gnd | gnd | gnd |
| Digital clock inputs | | 8 | RTM_CLK4+ | RTM_CLK4- | RTM_CLK2+ | RTM_CLK2- | RTM_CLK5+ | RTM_CLK5+ |
| | | 9 | RTM_CLK0+ | RTM_CLK0- | RTM_CLK3+ | RTM_CLK3- | RTM_CLK1+ | RTM_CLK1- |
| Shielding | | 10 | gnd | gnd | gnd | gnd | gnd | gnd |
| | | | | | | | | |
| | J31 | 1 | CH9_PA+ | CH9_PA- | DAC0+ | DAC0- | CH9_TF+ | CH9_TF- |

Source: mtca.desy.de

# Management and Diagnostics in xTCA Systems

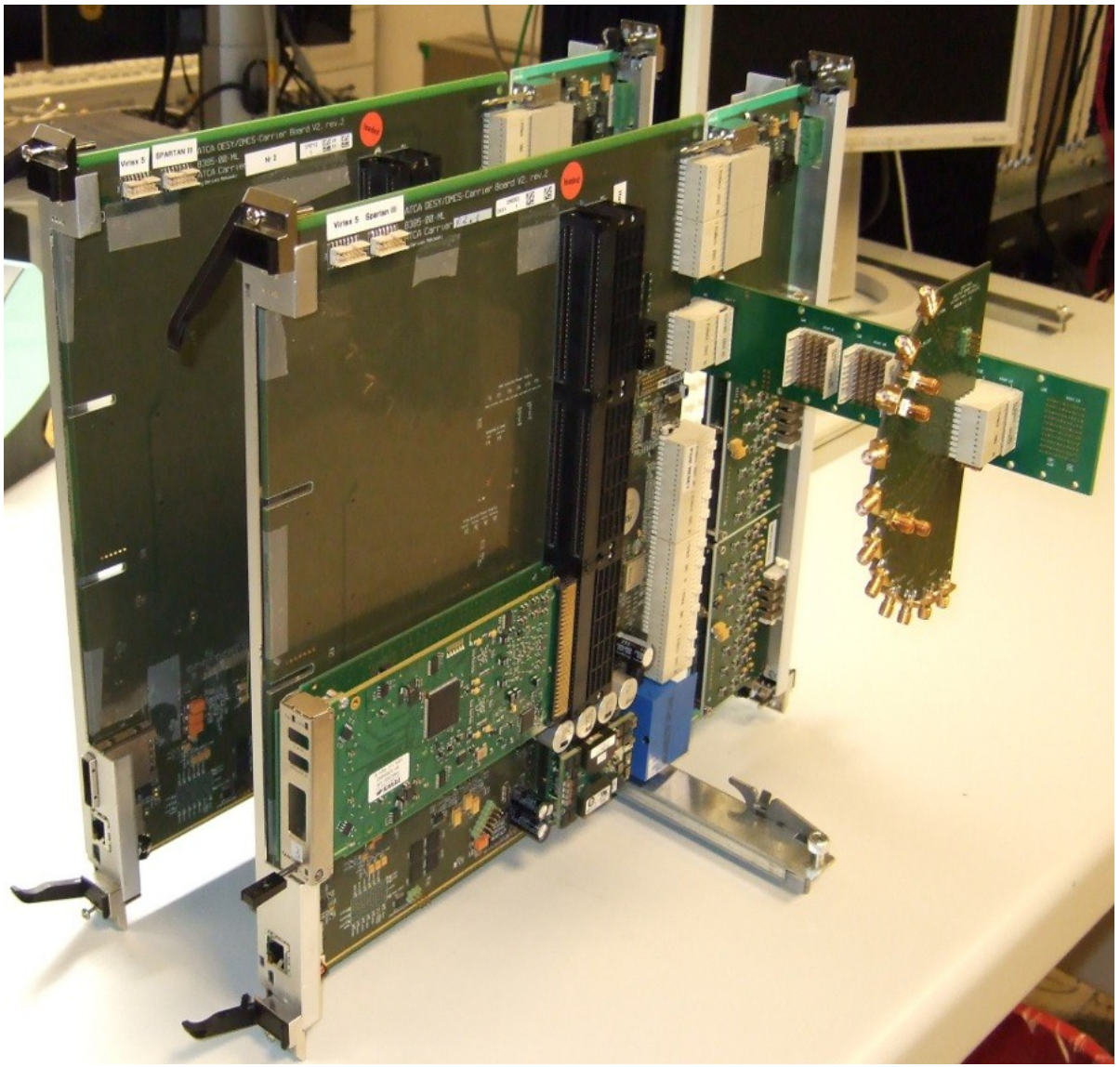
# IPMI at ATCA

## ATCA carrier module

- Developed IPMC based on Renesas uC
- Could manage 3 AMC modules
- FRU, E-keying and backplane management

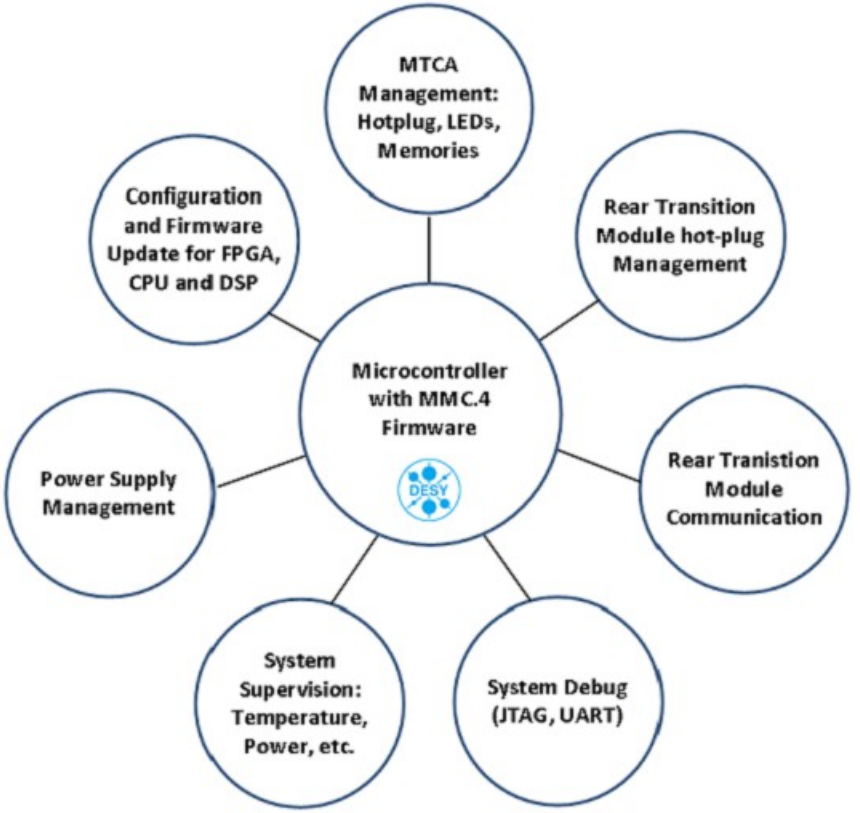
## Initial project for AMC

- Basic IPMI functions



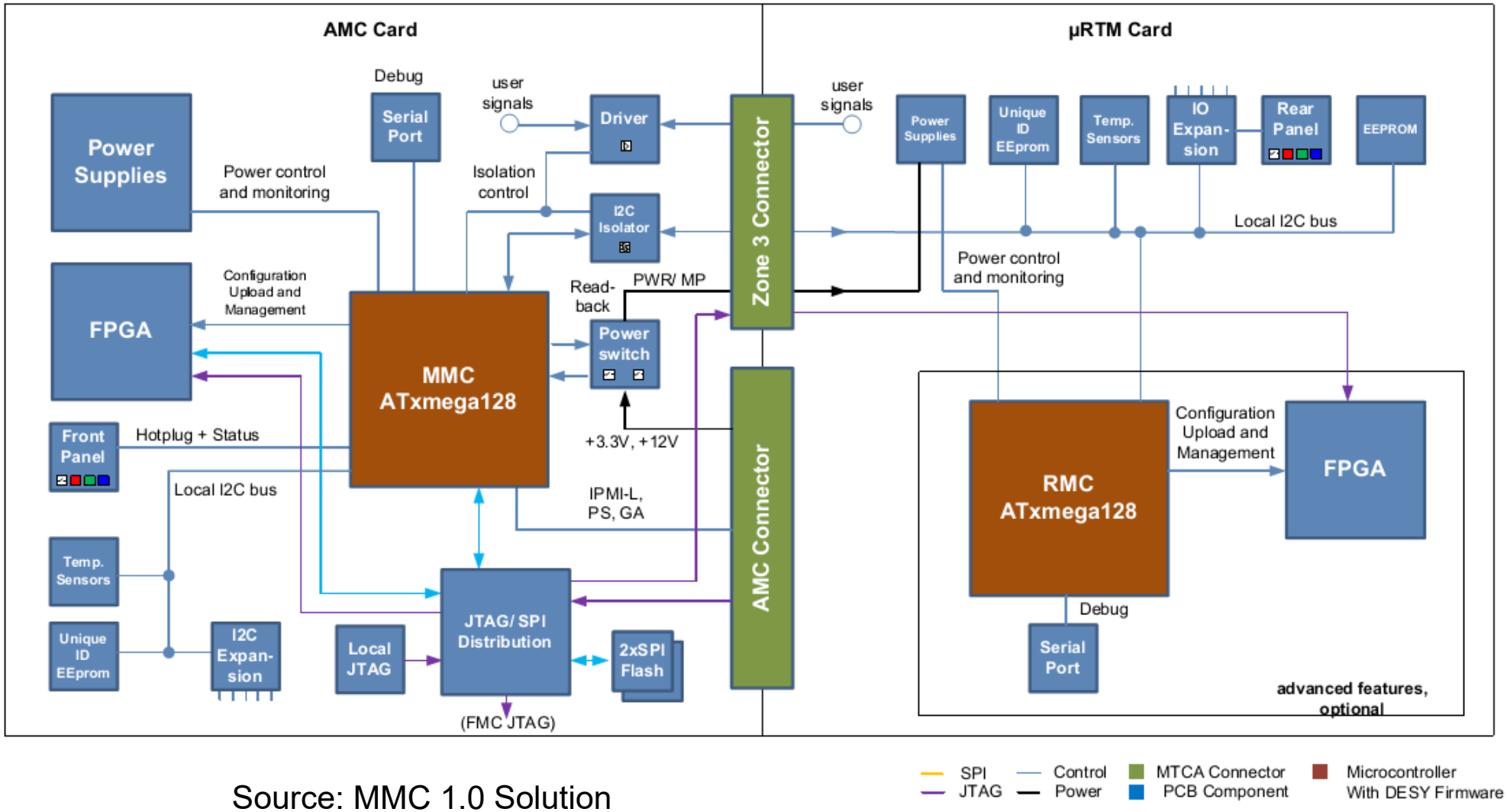
# MMC 1.0 - Smart and Easy MMC Solution

- DESY MMC V1.0 is a set of hardware and software building blocks
- Allows AMC/RTM designers to develop management for MTCA.4 cards
- Can be fully customized or used as a drop-in module based on fixed schematics and binary FW image
- Developed together with DESY collaboration partners
  - DMCS is responsible for hardware as well as supports firmware development
- Schematics and source code available → Starter Kit
- DESY Approach:
  - Idea: *Provide HW and FW building blocks, let user decide what to copy*
  - Philosophy: *„If you know better, modify it. If you don‘t know, copy it“*




Source: MMC 1.0 Evalkit datasheet

# MMC 1.0 – hardware structure




Source: MMC 1.0 Solution

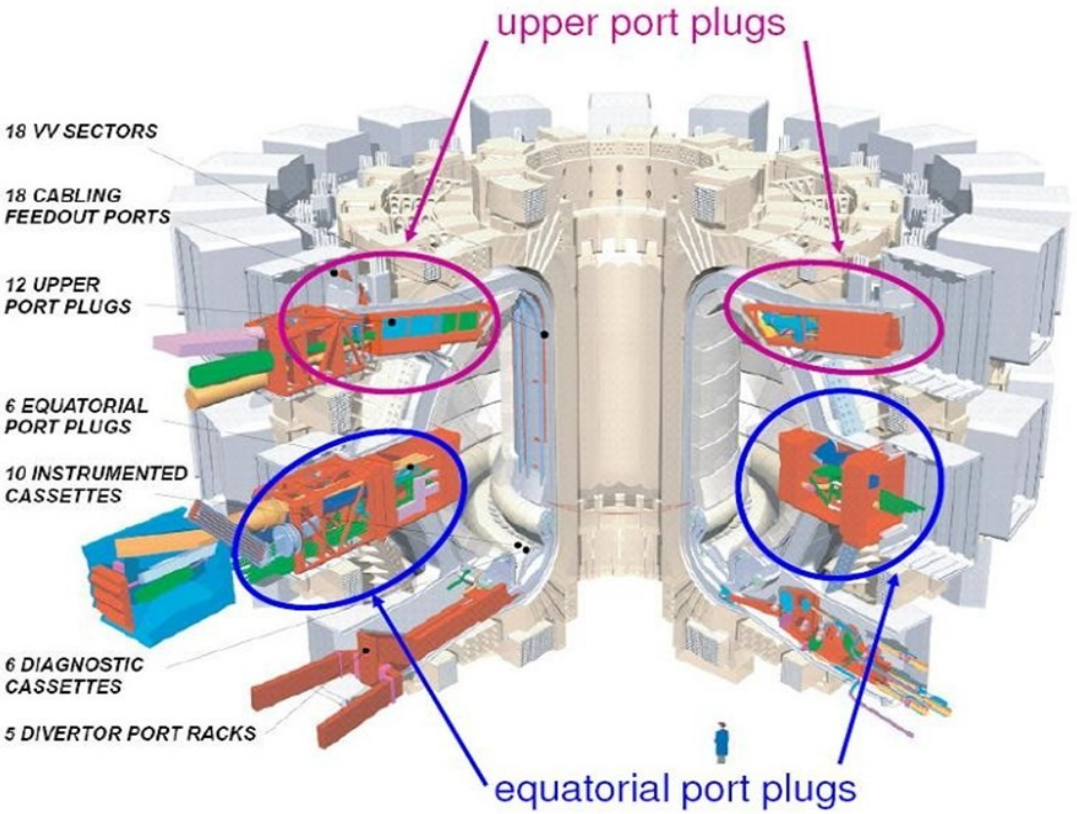
# Image Acquisition System

# ITER Project

**Challenges in design of imaging systems for plasma diagnostics:**

- Plasma diagnostics - monitor plasma temperature, density, radiative properties, first-wall resilience
- 200 cameras:

  1-8 Mpx @ 50-50000 FPS
- Throughput can easily exceed 8 Gb/s per camera
- Scalability and high reliability
- 50 ns synchronization accuracy

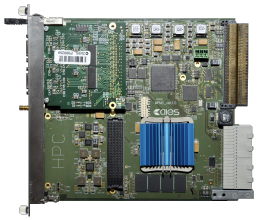



ITER Diagnostic Port Plugs

# Image Acquisition and Processing with MTCA.4



8-32 Gbps



Frame Grabber

32 Gbps

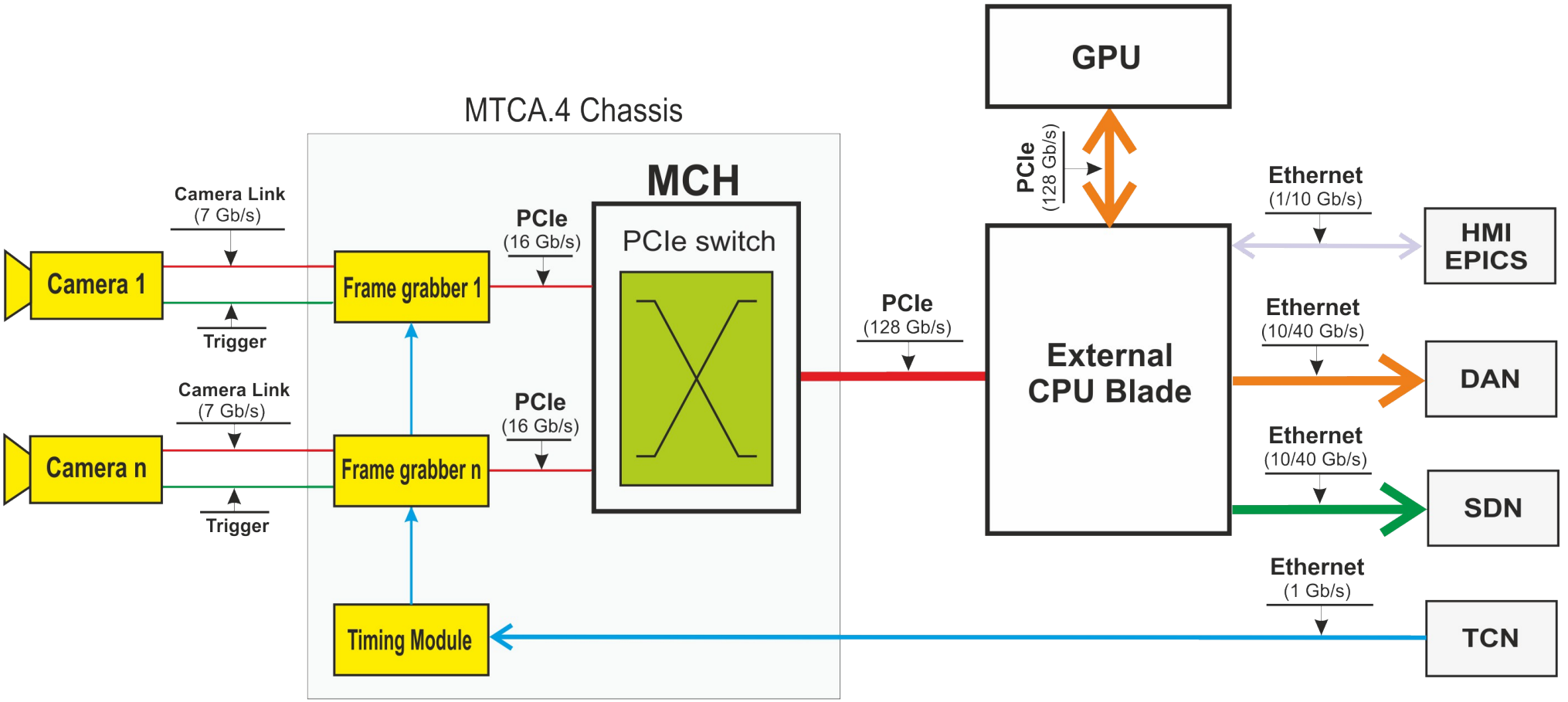
MTCA.4 12-slot Chassis

128 Gbps

High Performance CPU

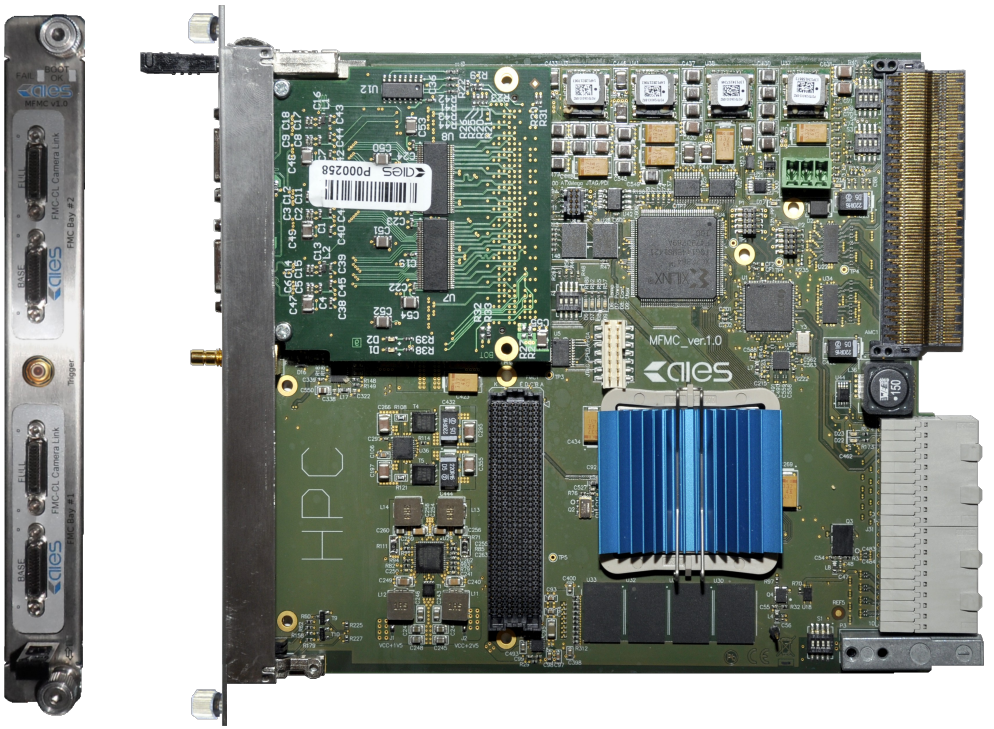
Timing module

# Image Acquisition – External CPU



# MFG4 - Frame Grabber Card for MTCA.4

- Cost-effective solution for high-performance image acquisition systems
- Designed as FMC carrier module (HPC and LPC) with FMC extension modules:
  - Camera Link (Base, Full, Ext-Full)
  - CoaXPress
  - Universal IO module
  - Firmware support for selected protocols
- Provides all resources for data acquisition and control systems (FPGA processing power, SDRAM, clocks distribution, trigger and interlock signals)
- Based on Xilinx Artix 7 (XC7A200T) FPGA
- RTM Zone 3 connector (D1.2 Digital Class)



# MPCIE-16 - PCIe Link for MTCA.4

- Allows to overcome the limitations of MTCA.4 PCIe connectivity
- More processing power using external CPU
- Possibility to use powerful GPU
- Supports PCIe x16, gen. 3 via copper cable
- Data throughput up to 128 Gbps
- Cost effective solution for MTCA.4 System
- No additional drivers or software needed

# Thank you for your attention