LATOME design @ LAPP

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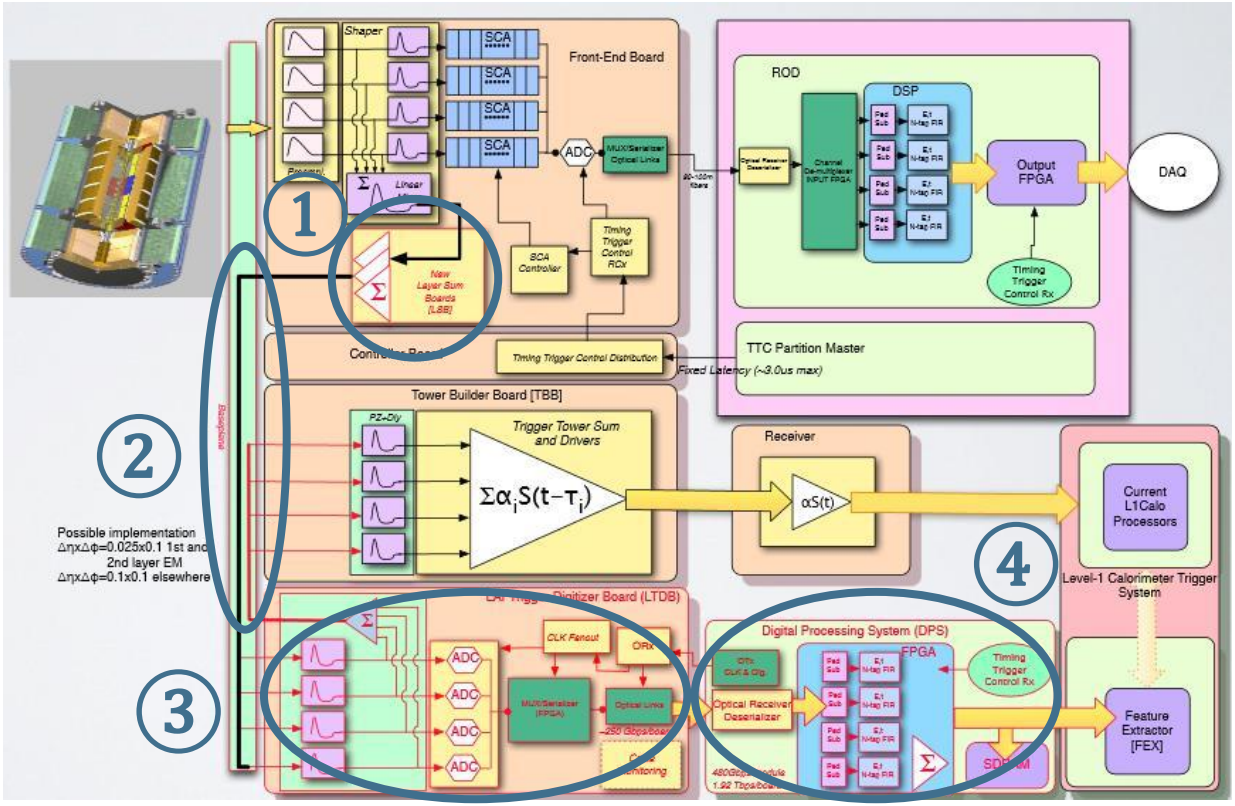
LATOME Design @ LAPP

1. ATLAS LAr Trigger Architecture
2. ATCA blade
3. AMC - LATOME
4. Functional tests
5. L1A Calo link tests
6. Status / Worries / Plans

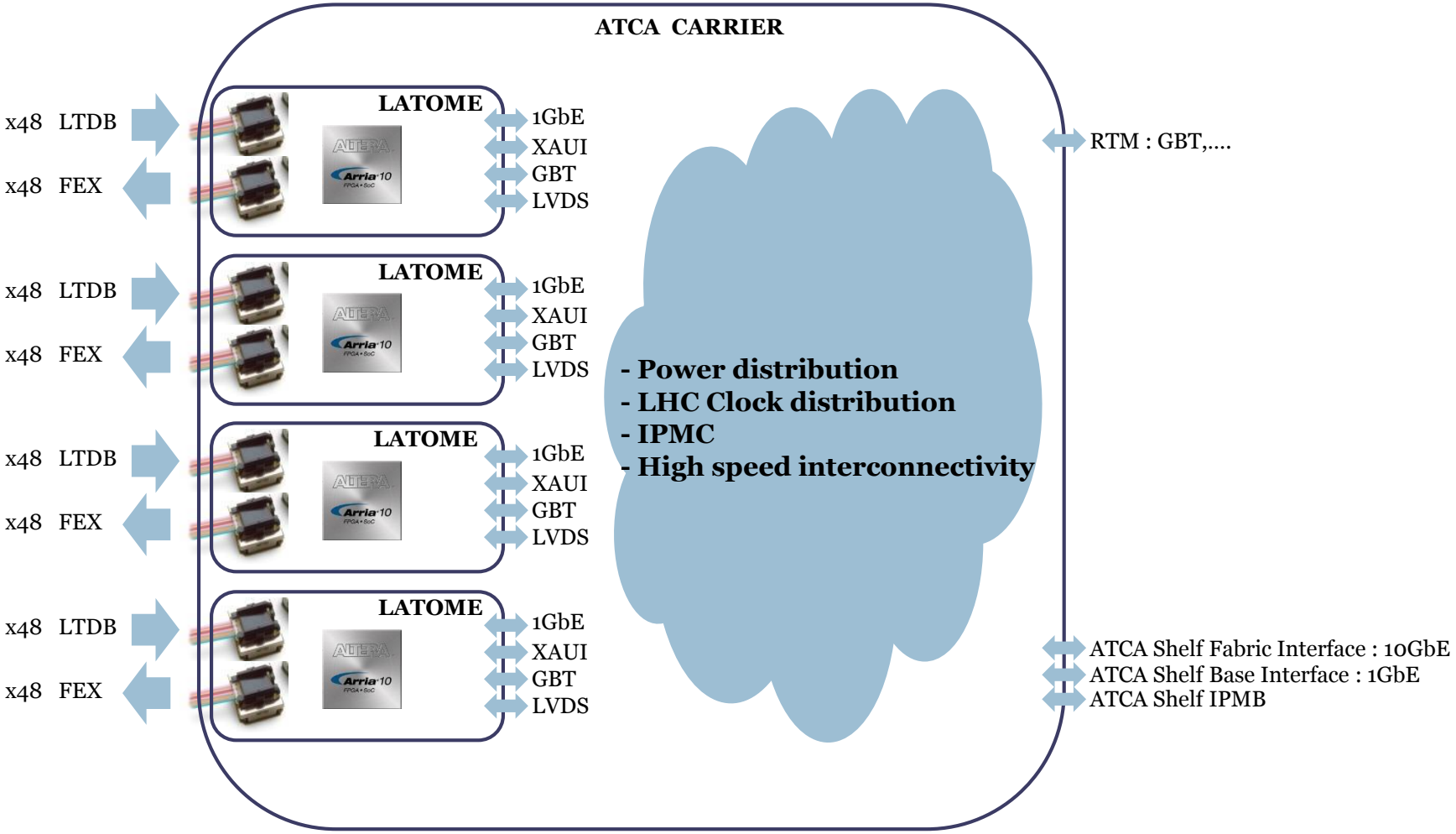
Trigger architecture – Upgrade system (digital)

- ① -> **Front End Boards form *Super Cell* (new segmentation of the detector)**
- ② -> **Backplane : transmits Super Cell to LArg Trigger Digital Board *(LTDB)***

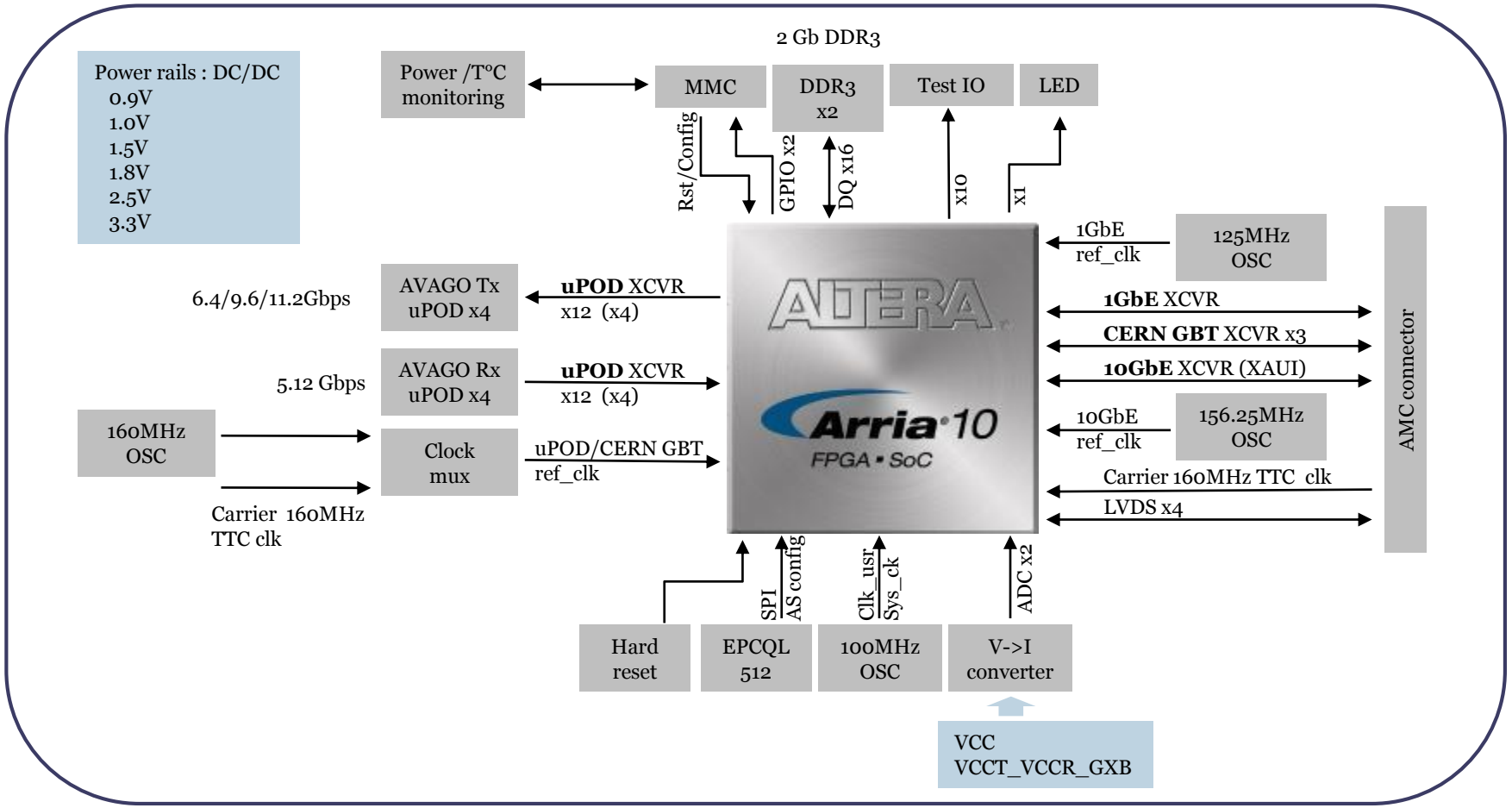


- ③ -> *LAr Trigger Digital Board (LTDB)* **: digitizes SC at 40MHz, generates analog sums**
- ④-> *LAr Digital Processing Board (LDPB)* **: reconstructs E_T for L1A Calo system**

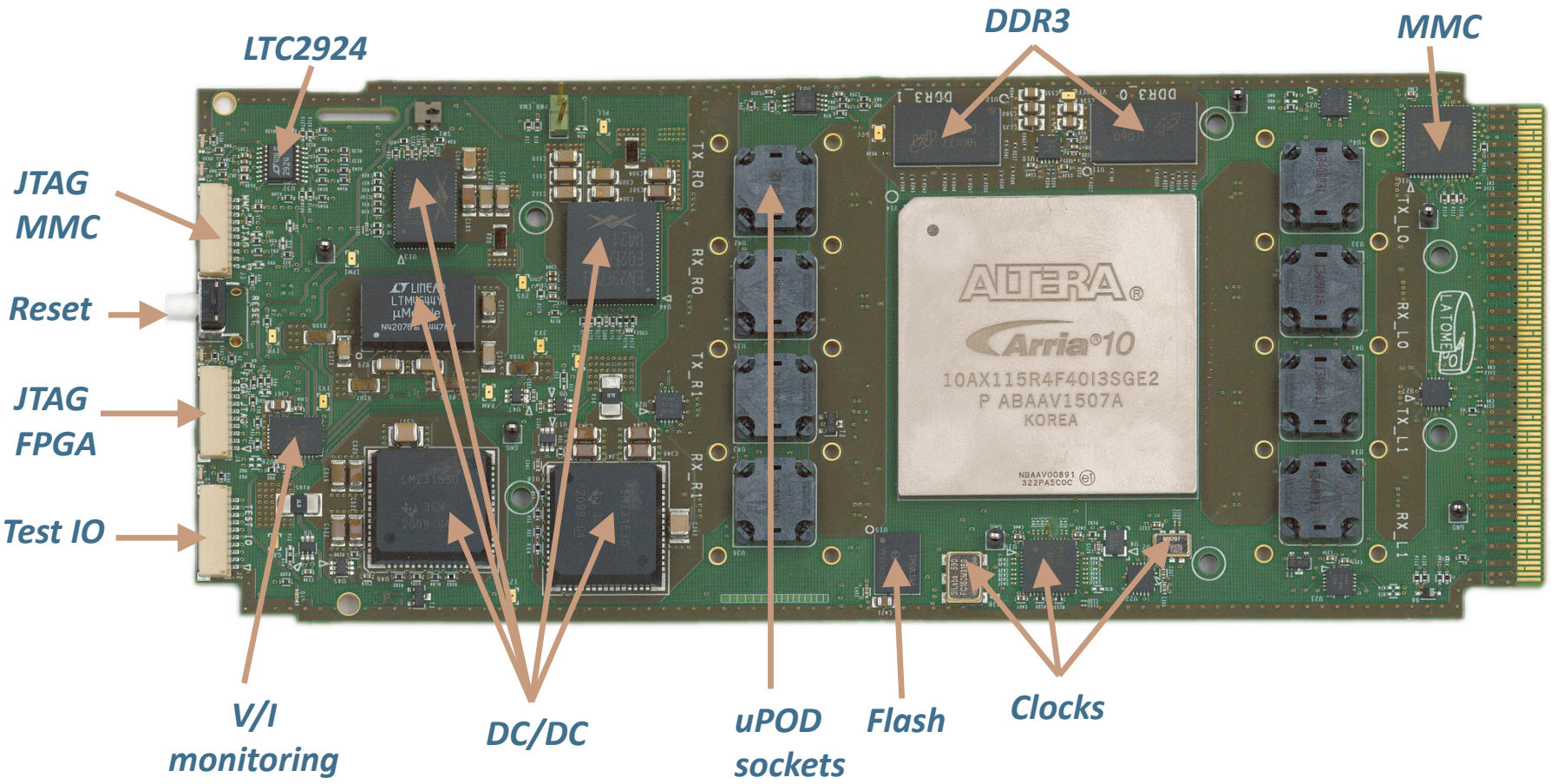
ATCA blade – LDPB = Carrier + LATOME



Synoptic - LATOME

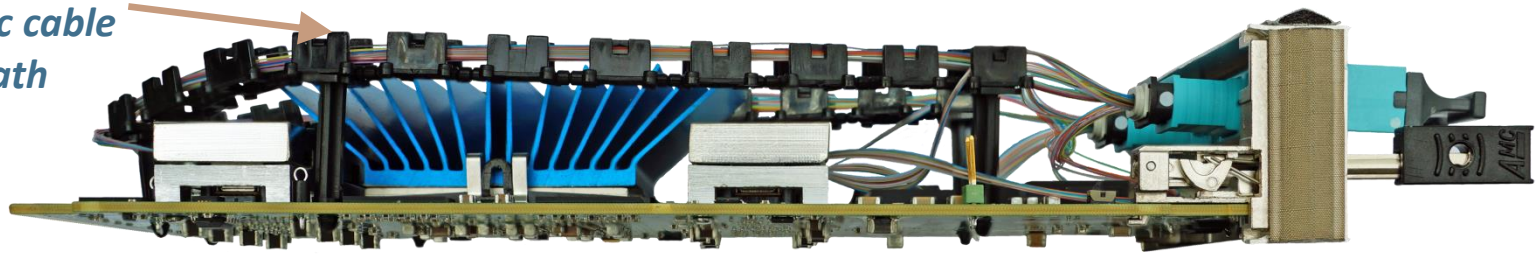


LATOME – With FPGA

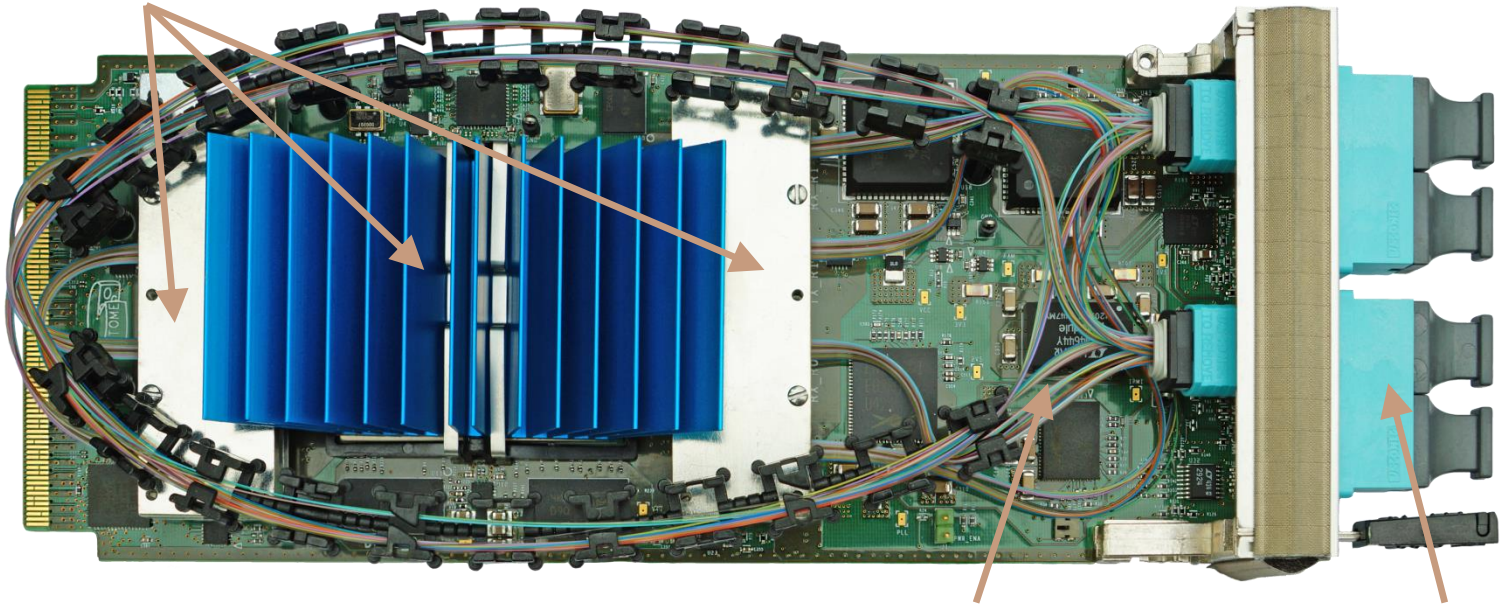


LATOME – With mechanics

Flexible plastic cable path



Heatsinks : uPOD + FPGA



48 -> 4x12 ribbons with individual fibers

Front panel with 4 MTP connectors

Functional tests

√ DDR3 :

- Power up calibration , R/W sequences : OK

√ uPOD optical links :

- OK @ 11.2 Gbps

√ uPOD monitoring :

- Scanning of all the monitors registers on all the uPOD : OK

√ Carrier board interfaces :

- High speed links, LVDS, clock : OK

√ Power :

- DC/DC sense signals connected to FPGA for better regulation
  - For FPGA core and FPGA transceivers power rails which need high current
  - Voltage drop measured on PCB with high current

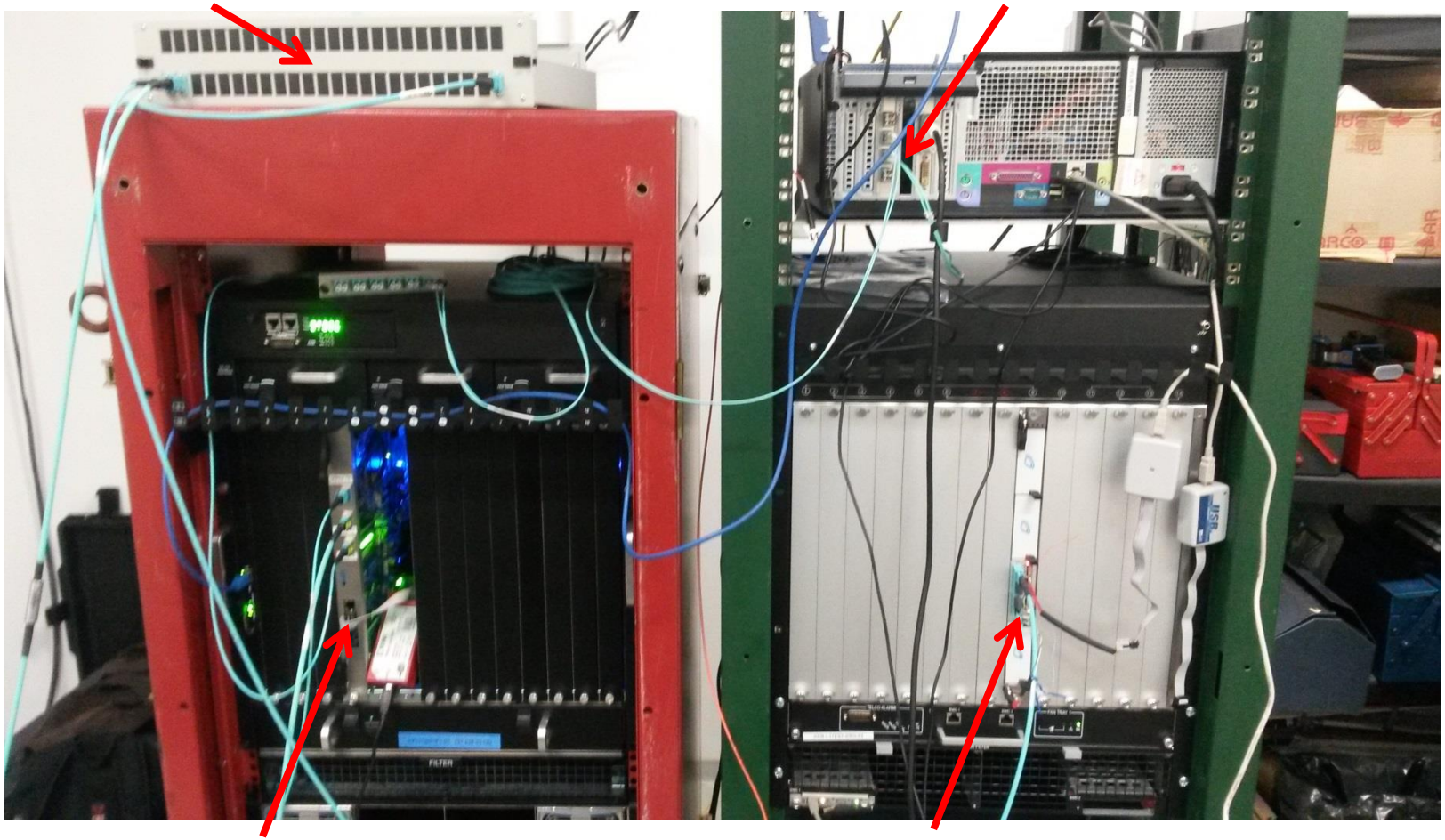
√ MMC :

- Tests on going

LATOME – Optical link tests with L1A gFEX

FOX box : Optical splitters

FELIX (PC+XILINX kit) : GBT links for clock

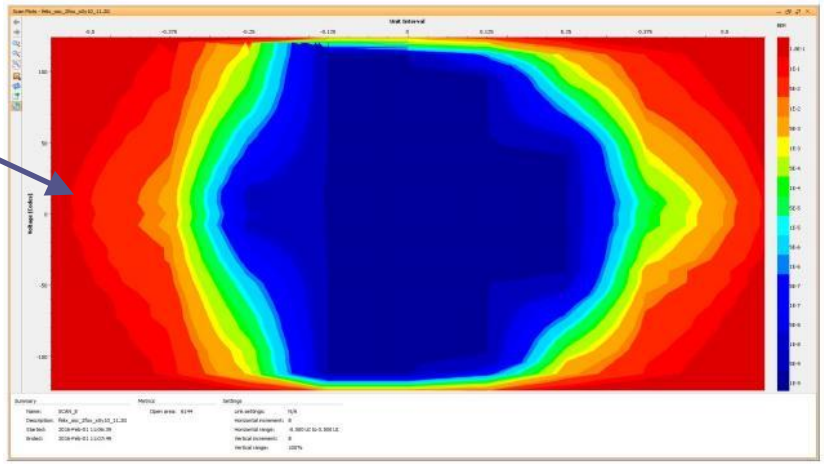


L1A Calo ATCA Shelf : gFEX

LArg ATCA Shelf : LDPB

LATOME – Optical link tests with L1A gFEX

- **Setup**
  - **LATOME** (ALTERA ARRIA10) :
    - PRBS generator = XILINX PRBS31 generator component
  - **gFEX** (XILINX KINTEX-7 Ultrascale) :
    - PRBS checker = iBERT design : BER, Eye diagram
  - **LATOME cooling in the Shelf**
    - ~49°C for FPGA
    - ~45°C for uPOD



Results @ 11.2Gbps

The 48 links work properly between the 2 boards

- BER < 10^{E}-14 (~3 hours)
- With all different clock architectures
- With different FOX configurations

Status / Worries / Plans

Status

- 3 LATOME version 1 mounted with ARRIA10 ES version
  - Boards used for Hardware tests and DAQ firmware tests

Worries

- uPOD :
  - uLGA springs seem to be fragile
  - uPOD not easy to mount for a production
- Power supply : high current measured on FPGA core, FPGA transceiver
  - Next version with new DC/DC and new power planes
  - FPGA version = Engineering Sample => Current should be reduced for Production Version

Plans

- Design of the LATOME version 2
  - New power supply design
- Integration tests should start this summer
  - Test with Front End board, TDAQ, GBT Synchronisation, Network (GbE, 10GbE), Cooling,…….