LATOME design @ LAPP

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LATOME Design @ LAPP

1. ATLAS LAr Trigger Architecture
2. ATCA blade
3. AMC - LATOME
4. Functional tests
5. L1A Calo link tests
6. Status / Worries / Plans
Trigger architecture – Upgrade system (digital)

1. Front End Boards form Super Cell (new segmentation of the detector)
2. Backplane: transmits Super Cell to LArg Trigger Digital Board (LTDB)

3. LAr Trigger Digital Board (LTDB): digitizes SC at 40MHz, generates analog sums
4. LAr Digital Processing Board (LDPB): reconstructs $E_T$ for L1A Calo system
**ATCA blade – LDPB = Carrier + LATOME**

**ATCA CARRIER**

- x48 LTDB
- x48 FEX

LATOME

- 1GbE
- XAUI
- GBT
- LVDS

- **Power distribution**
- **LHC Clock distribution**
- **IPMC**
- **High speed interconnectivity**

RTM : GBT,....

ATCA Shelf Fabric Interface : 10GbE
ATCA Shelf Base Interface : 1GbE
ATCA Shelf IPMB

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Synoptic - LATOME

Power rails: DC/DC
0.9V
1.0V
1.5V
1.8V
2.5V
3.3V

Power /T°C monitoring

MMC
DDR3
Test IO
LED

2 Gb DDR3

AVAGO Tx
uPOD x4

AVAGO Rx
uPOD x4

Clock
mux

uPOD XCVR
x12 (x4)

uPOD XCVR
x12 (x4)

uPOD/CERN GBT
ref_clk

ADC x2

Hard
reset

EPCQL 512

100MHz
OSC

V->I
converter

VCC
VCCT_VCCR_GXB

1GbE ref_clk

125MHz
OSC

1GbE XCVR

CERN GBT XCVR x3

10GbE XCVR (XAUI)

10GbE ref_clk

156-25MHz
OSC

Carrier 160MHz TTC clk

LVDS x4

6.4/9.6/11.2Gbps

5.12 Gbps

160MHz
OSC

Carrier 160MHz TTC clk
LATOME – With FPGA

- DC/DC
- uPOD sockets
- Flash
- Clocks
- JTAG
- MMC
- Reset
- Test IO
- V/I monitoring

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LATOME – With mechanics

Flexible plastic cable path

Heatsinks: uPOD + FPGA

48 -> 4x12 ribbons with individual fibers

Front panel with 4 MTP connectors
**Functional tests**

- **√ DDR3:**  
  - Power up calibration, R/W sequences: OK

- **√ uPOD optical links:**  
  - OK @ 11.2 Gbps

- **√ uPOD monitoring:**  
  - Scanning of all the monitors registers on all the uPOD: OK

- **√ Carrier board interfaces:**  
  - High speed links, LVDS, clock: OK

- **√ Power:**  
  - DC/DC sense signals connected to FPGA for better regulation  
    - For FPGA core and FPGA transceivers power rails which need high current  
    - Voltage drop measured on PCB with high current

- **√ MMC:**  
  - Tests on going
LATOME – Optical link tests with L1A gFEX

IFOX box: Optical splitters

FELIX (PC+XILINX kit): GBT links for clock

L1A Calo ATCA Shelf: gFEX

LArg ATCA Shelf: LDPB
LATOME – Optical link tests with L1A gFEX

- Setup
  - LATOME (ALTERA ARRIA10) :
    - PRBS generator = XILINX PRBS31 generator component
  - gFEX (XILINX KINTEX-7 Ultrascale) :
    - PRBS checker = iBERT design : BER, Eye diagram
  - LATOME cooling in the Shelf
    - ~49°C for FPGA
    - ~45°C for uPOD

Results @ 11.2Gbps
The 48 links work properly between the 2 boards
- BER < 10^{-14} (~3 hours)
- With all different clock architectures
- With different FOX configurations
Status / Worries / Plans

Status
- 3 LATOME version 1 mounted with ARRIA10 ES version
  - Boards used for Hardware tests and DAQ firmware tests

Worries
- uPOD:
  - uLGA springs seem to be fragile
  - uPOD not easy to mount for a production
- Power supply: high current measured on FPGA core, FPGA transceiver
  - Next version with new DC/DC and new power planes
  - FPGA version = Engineering Sample => Current should be reduced for Production Version

Plans
- Design of the LATOME version 2
  - New power supply design
- Integration tests should start this summer
  - Test with Front End board, TDAQ, GBT Synchronisation, Network (GbE, 10GbE), Cooling,.......