Neutron Measurements Using Time of Flight Calculations on FLexRIO

Contact info

ANTE Kft.
info@ante.hu
Building 6, KFKI Campus
Konkoly Thege 29-33, H-1121 Budapest
Phone: +36 1 392 2281

Péter HARMAT PhD
General Manager
Email: harmat@ante.hu
www.ante.hu

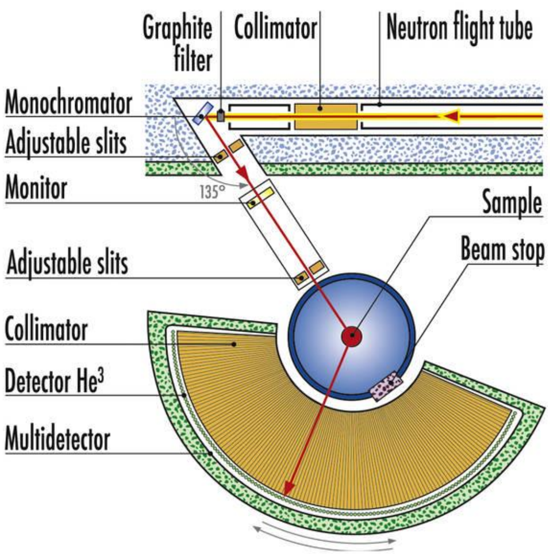
ANTE profile:
Instruments for neutron scattering

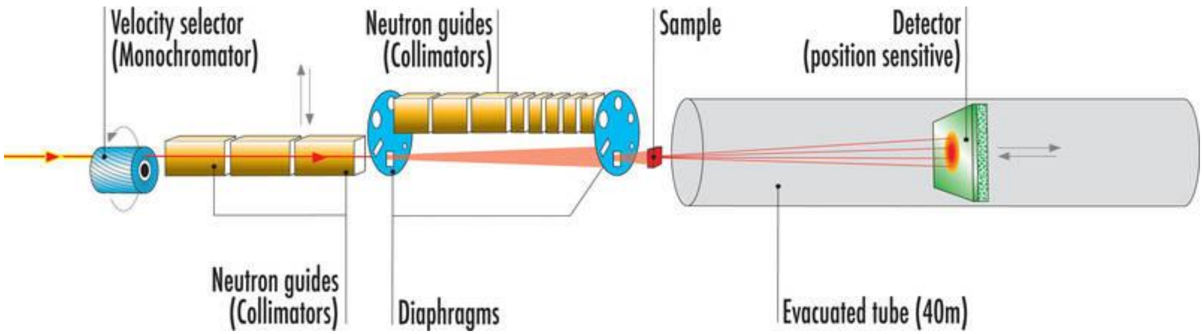
ANTE delivers new generation

signal processing and data acquisition with built-in **event recording** capability

Absolute timestamp:

- 100 ns (8 ns internally)
- 48 bit time resolution (1 year)





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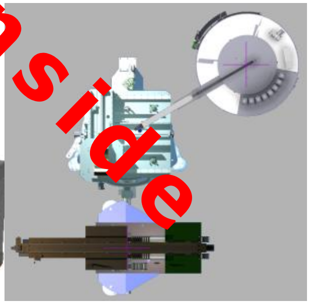
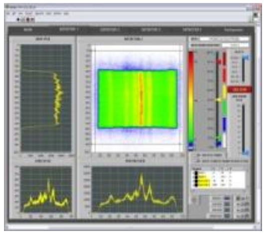
harmat@ante.hu

Summary of ANTE Neutron Scattering Products

- **SpecTDC Unit for 2D PSD detectors**
  - Detectors with delay line outputs
- **LisTDC Unit also for 2D PSD detectors**
  - with extra preferences for Time of Flight (TOF) measurements
- **LisTOF Unit with event recorder software**
  - For point detectors
- **Instrument Control**
  - Complete spectrometer control e.g. motion, temperature, magnetic fie
- **Motion Control**
  - hardware + software
- **Scientific Application**
  - Comprehensive scientific software for the users





FPGA inside

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harmat@ante.hu

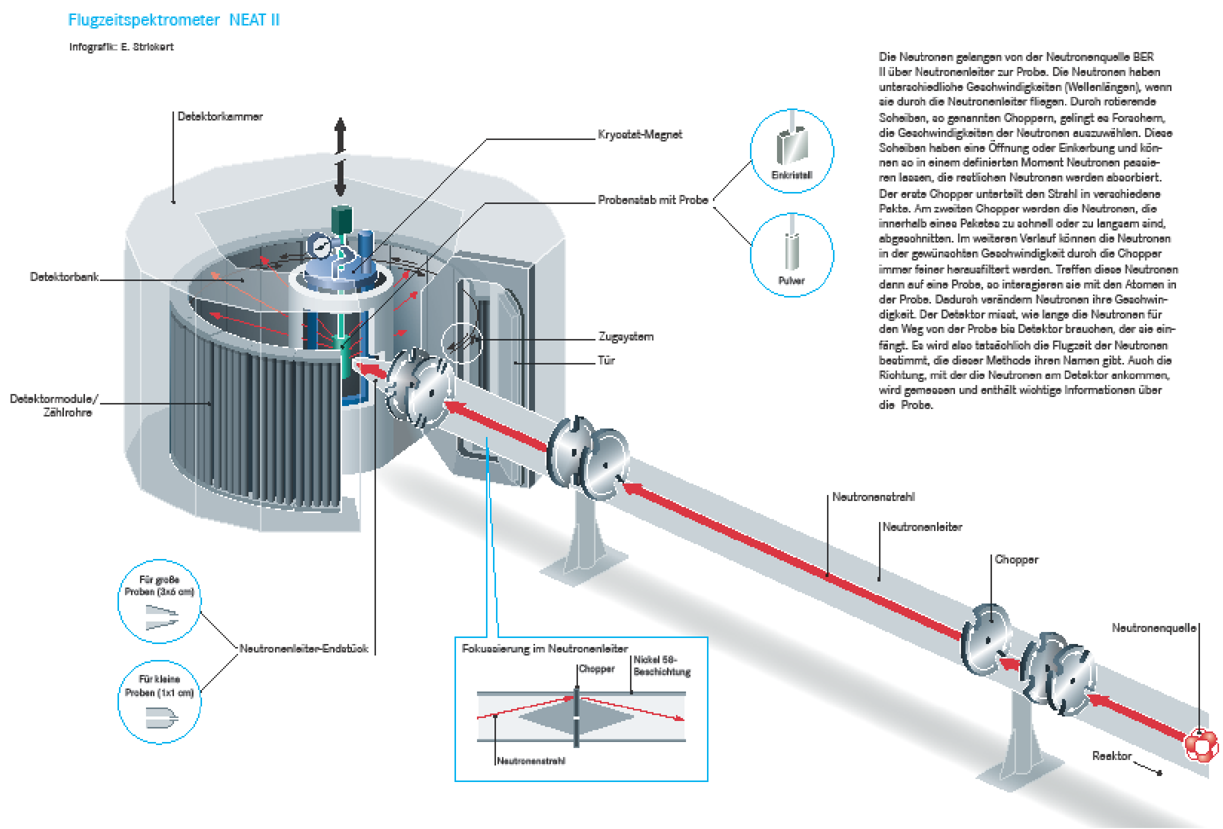
ANTE Innovative Technologies

Main professional relations

- BNC Budapest
- Atomki, Debrecen
- Wigner FK, Budapest
- Mirrotron, Budapest
- Chinese Academy of Sciences, Mianyang
- National Instruments
- ISIS UK (Signal processing)
- HZB Berlin (NEAT-II)
- IFE, Norway (Odin)
- ANSTO, Australia (SANS)

Worldwide Customers

The NEAT II Instrument at HZB



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harmat@ante.hu

Inside the vacuum chamber

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harmat@ante.hu

Requirements

- 416 Neutron detectors – ^{3}He tubes
- 20 mm resolution on 2000 mm detectors
- 50kS/s load per detector (!) with 10% dead time:
  - $T_{DAQ} < 0.1 * 1/50kHz = 2\mu s$
- 1MS/s load over all 416 detectors – uneven load
- TOF measurement with a 7 chopper system
- Minimizing the background
  - More detailed signal analysis than usual…

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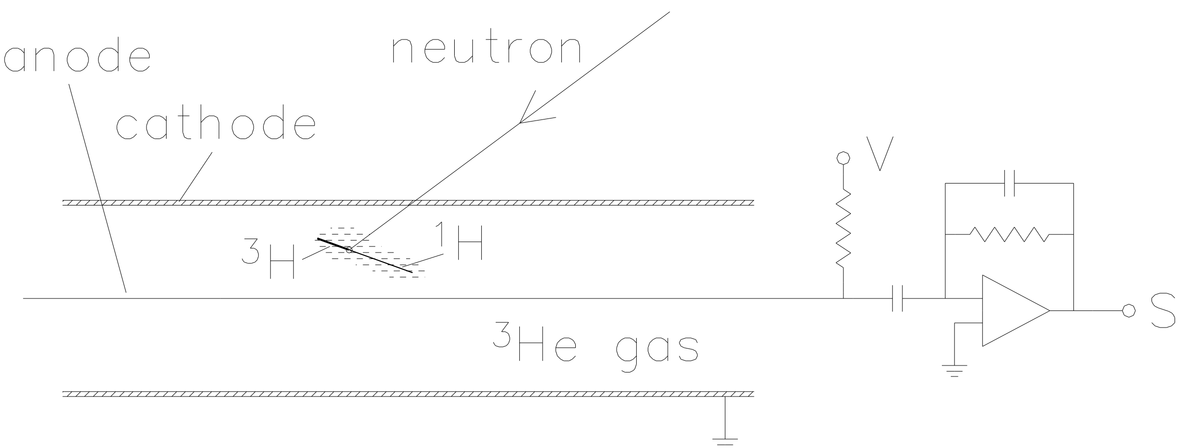
harmat@ante.hu

Neutron detection with ^{3}He tube

Basic operation

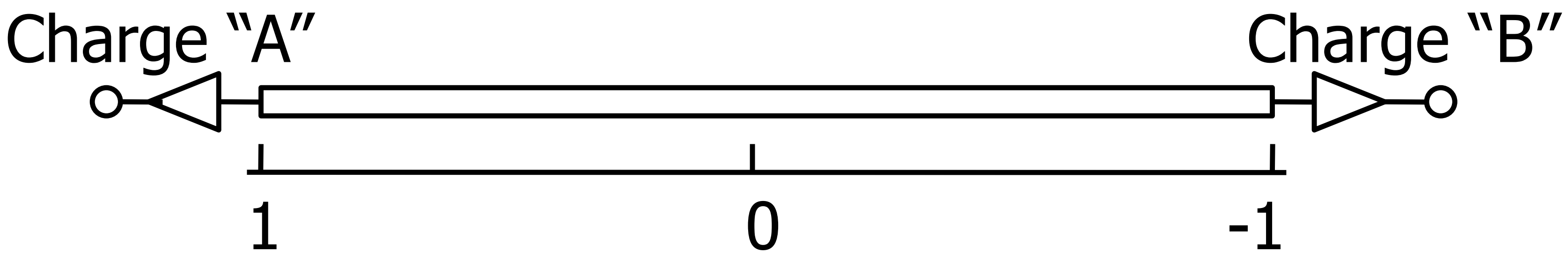


$$n + {}^3He \rightarrow {}^3H + {}^1H + 0.76\,MeV$$

Neutron detection with ^{3}He tube

Position sensitive detectors (PSD)

- Charge division method:



Position = (A-B)/(A+B)

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harmat@ante.hu

DAQ solution

Instead of old “integrating” (slow) electronic –

digital charge integration with quick analog electronics (T<60ns)

- Sampling ADC
  - 20ns sampling time
- FPGA
  - for continuous reading out of sampling ADC data
  - Trigger state detection („peak is coming”)

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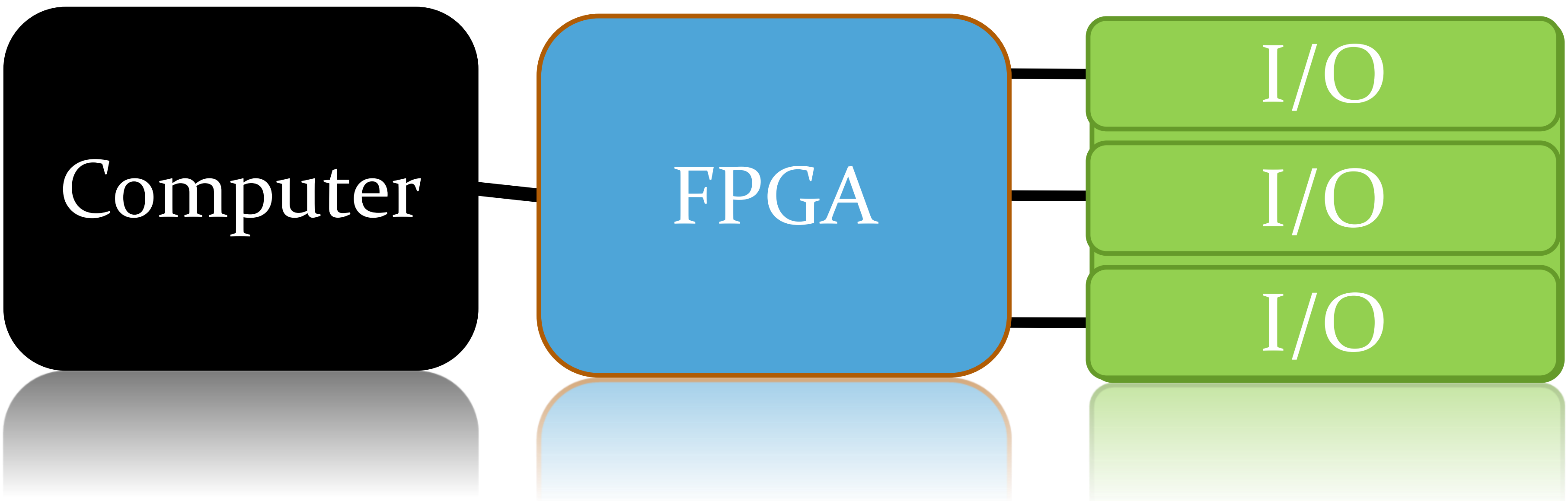
harmat@ante.hu

Summary of High Level Requirements



- Floating-point processing
- Communications GigE
- Synchronized time scale

- Continuous signal sampling
- Analog trigger condition
- Pre-triggering
- High-speed processing
- 100 ns accurate time stamp

- 832 analog input channels
- Sampling ADCs
- 12 bit resolution
- 50 k events/sec/channel
- max 1M event/system

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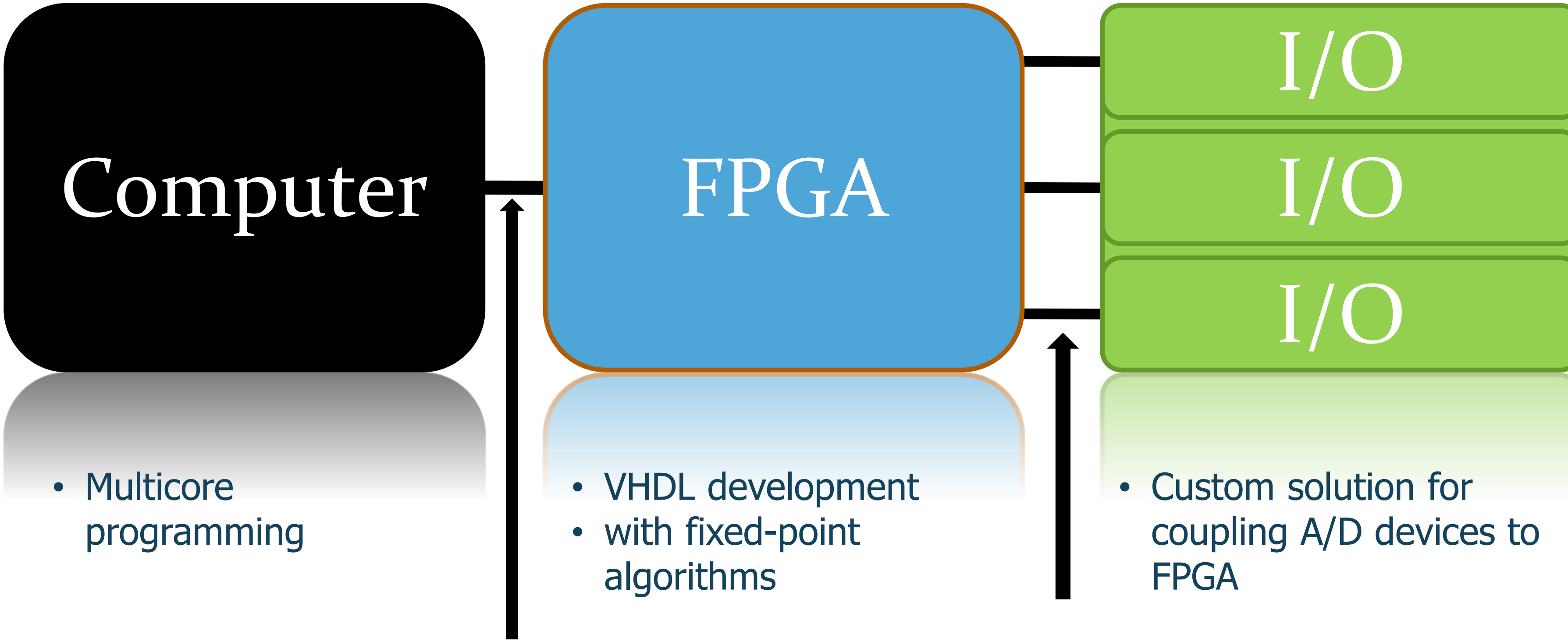
harmat@ante.hu

ANTE unique efforts vs. routine solutions from NI



- Multicore programming

- VHDL development
- with fixed-point algorithms

- Custom solution for coupling A/D devices to FPGA

- Custom digital interface/buses

- Custom timing for different types of I/O

Such a „usual way” of development needs much more effort, source allocation than ….

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harmat@ante.hu

ANTE unique efforts vs. routine solutions from NI

- LabView + C++ programming
- Predefined data communication by using DMA, interrupt and bus control drivers
- LabView only
- Predefined I/O drivers both for digital lines and ADCs
- Ready made hardware

… using LabVIEW Graphical Programming Environment for Computer and FPGA

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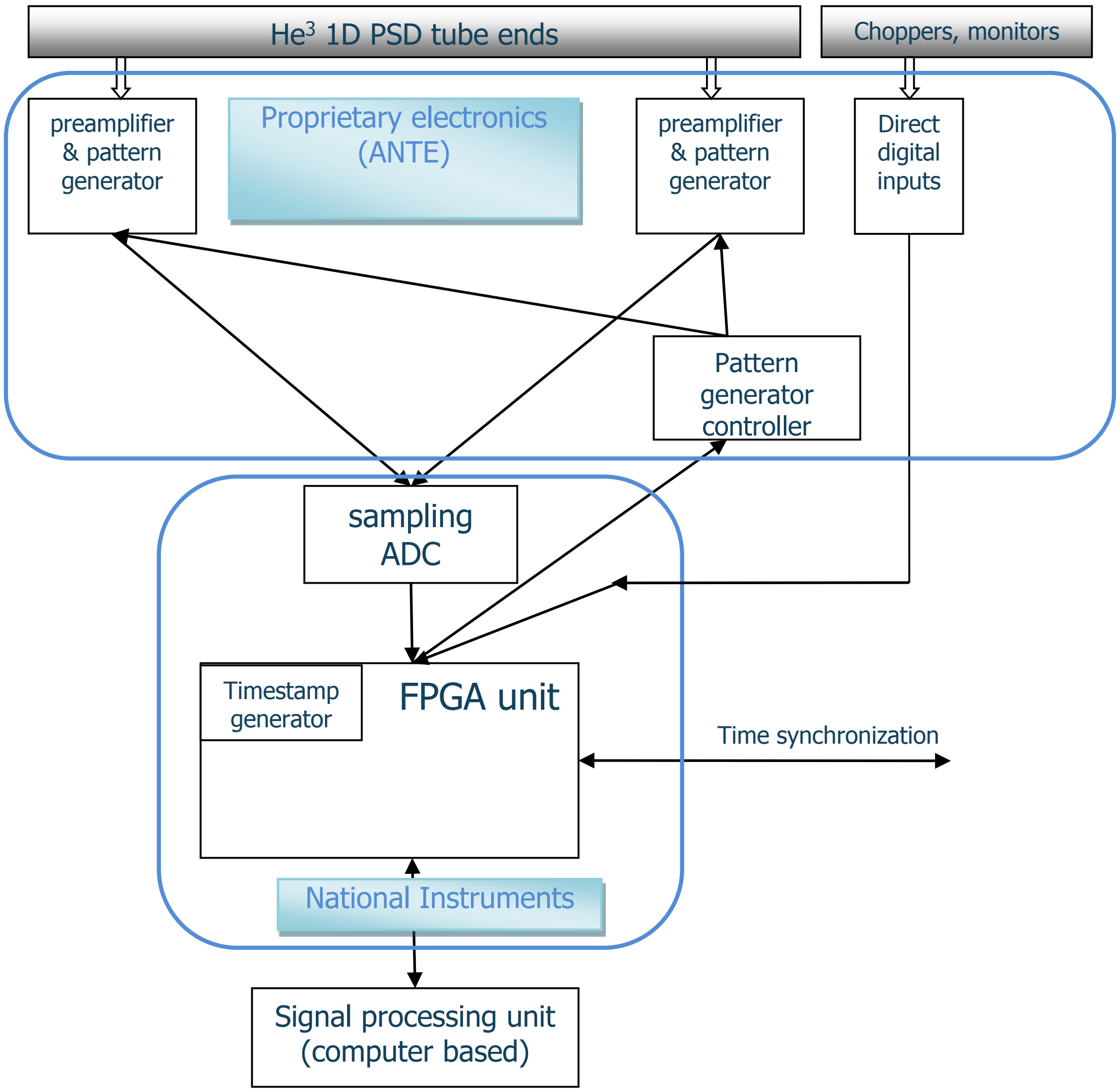
Electronics



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harmat@ante.hu

Choosing the right ADC card

model	resolution [bits]	channels	speed [MS/s]
NI 5731	12	2	40
NI 5732	14	2	80
NI 5733	16	2	120
NI 5734	16	4	120
NI 5751	14	16	50
NI 5752	12	32	50
NI 5761	14	4	250
NI 5762	16	2	250
NI 5771	8	1	3000
	8	2	1500
NI 5772	12	1	1600
	12	2	800

2 bits in resolution
vs. 2x channels

too low resolution

Péter HARMAT
harmat@ante.hu

NI FlexRIO Adapter Modules

Digital

Analog

100 Mbps
SE DIO

300 Mbps
LVDS DIO

100MHz BW,
4.4 GHz RF I/O

200MHz BW,
4.4 GHz RF Rx

200MHz BW,
4.4 GHz RF Tx

2 ch. 3 GS/s,
8-bit AI

2 ch. 1.6 GS/s,
12-bit AI

300 Mbps
SE/LVDS DIO

1 Gbps
LVDS DIO

2 ch. 250 MS/s,
14-bit AI/16-bit AO

2 ch. 250 MS/s,
16-bit AI

4 ch. 250 MS/s,
14-bit AI

32 ch.
50 MS/s, 12-bit AI

16 ch. 50 MS/s,
14-bit AI

2 GS/s
14-bit AO

Camera Link

RS-485/422

2 ch. 100 MS/s,
14-bit AI/16-bit AO

2 ch. 40 MS/s,
12-bit AI

2 ch. 80 MS/s, 14-bit AI

2 ch. 120 MS/s,
16-bit AI

4 ch. 120 MS/s,
16-bit AI

2 ch. 1.25 GS/s,
14-bit AO

NI 5752

- 32 simultaneous 50 MS/s, 12-bit channels
- Uses TI AFE5801 analog front end including variable gain amplifiers and ADCs
- 2 Vpp, 100 Ω differential inputs with AC coupling
- Built-in antialias filters and programmable time-variable gain control
- 2 digital input channels
- 16 digital outputs with per-channel phase control that can be coupled to pulser arrays

Péter HARMAT
harmat@ante.hu

Choosing the FPGA module

Model	Bus/Form Factor	FPGA	FPGA Slices	FPGA DSP Slices	FPGA Memory (Block RAM)	Onboard Memory (DRAM)
NI PXIe-7965R/7966R	PXI Express	Virtex-5 SX95T	14720	640	8,784 kbit	512 MB
NI PXIe-7962R	PXI Express	Virtex-5 SX50T	8160	288	4,752 kbit	512 MB
NI PXIe-7961R	PXI Express	Virtex-5 SX50T	8160	288	4,752 kbit	0 MB
NI PXI-7954R	PXI	Virtex-5 LX110	17280	64	4,608 kbit	128 MB
NI PXI-7953R	PXI	Virtex-5 LX85	12960	48	3,456 kbit	128 MB
NI PXI-7952R	PXI	Virtex-5 LX50	7200	48	1,728 kbit	128 MB
NI PXI-7951R	PXI	Virtex-5 LX30	4800	32	1,152 kbit	0 MB

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Device Utilization
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Total Slices: 100.0% (4798 out of 4800)
Slice Registers: 48.7% (9342 out of 19200)
Slice LUTs: 96.6% (18556 out of 19200)
Block RAMs: 6.2% (2 out of 32)
DSP48s: 0.0% (0 out of 32)
```


Péter HARMAT
harmat@ante.hu

DAQ solution using FlexRIO

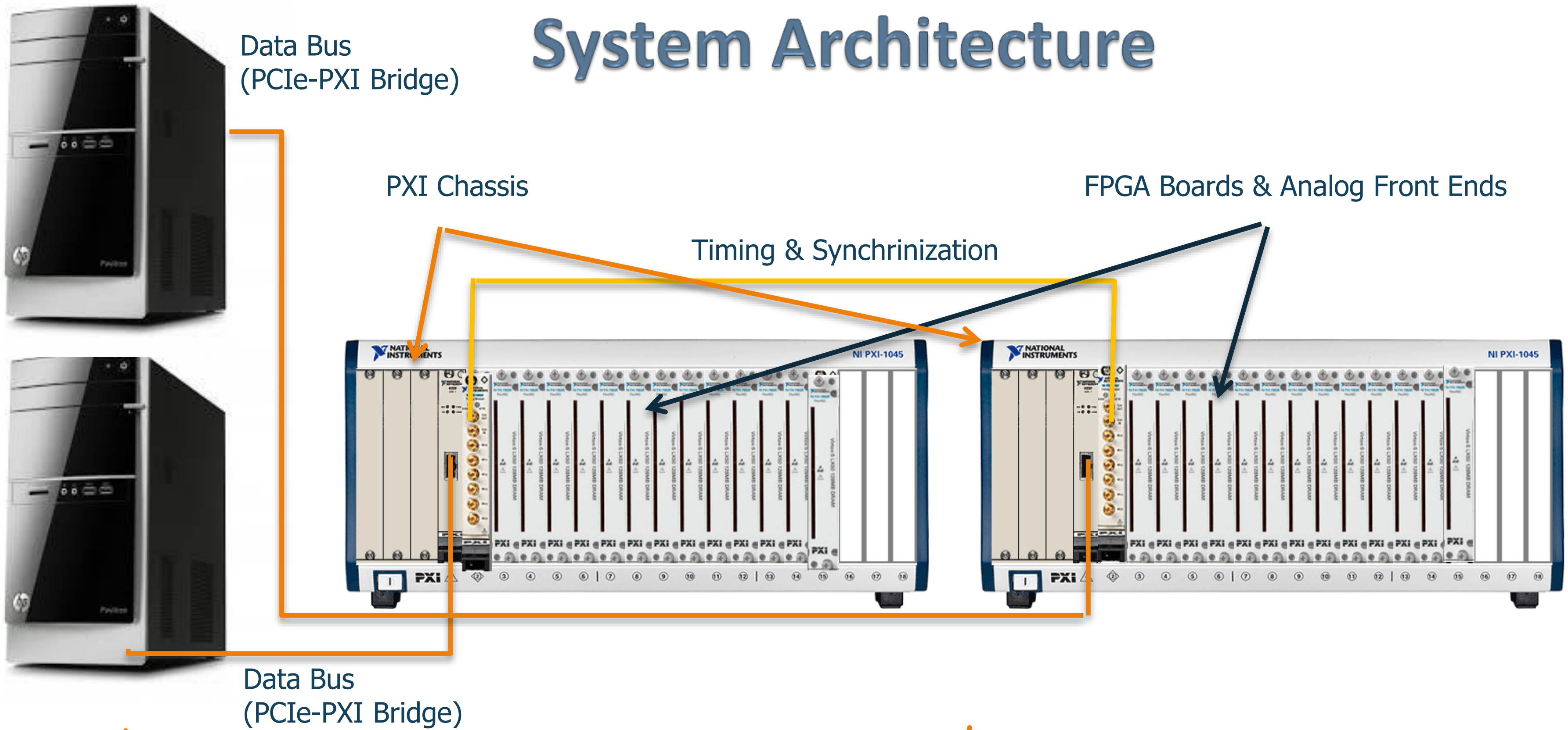
Digital charge integration with quick analog electronics (T<60ns) using sampling ADC:

- 26 pcs. NI 5752 12-bit, 50 MS/s, 32 Channel
- 20ns sampling time

- FPGA
  - 26 pcs. NI PXI-7951R FlexRIO FPGA (Virtex-5 LX30)
  - 16 tubes/32 channels per FPGA

Péter HARMAT
harmat@ante.hu

System Architecture



PC Functions:
Control of PXI Chassis
CPU Post processing
Data Storage
User Interface

PXI Functions:
Analog Data Acquistion
FPGA Preprocessing
Timming & Synchronization
Data Transfer to CPU

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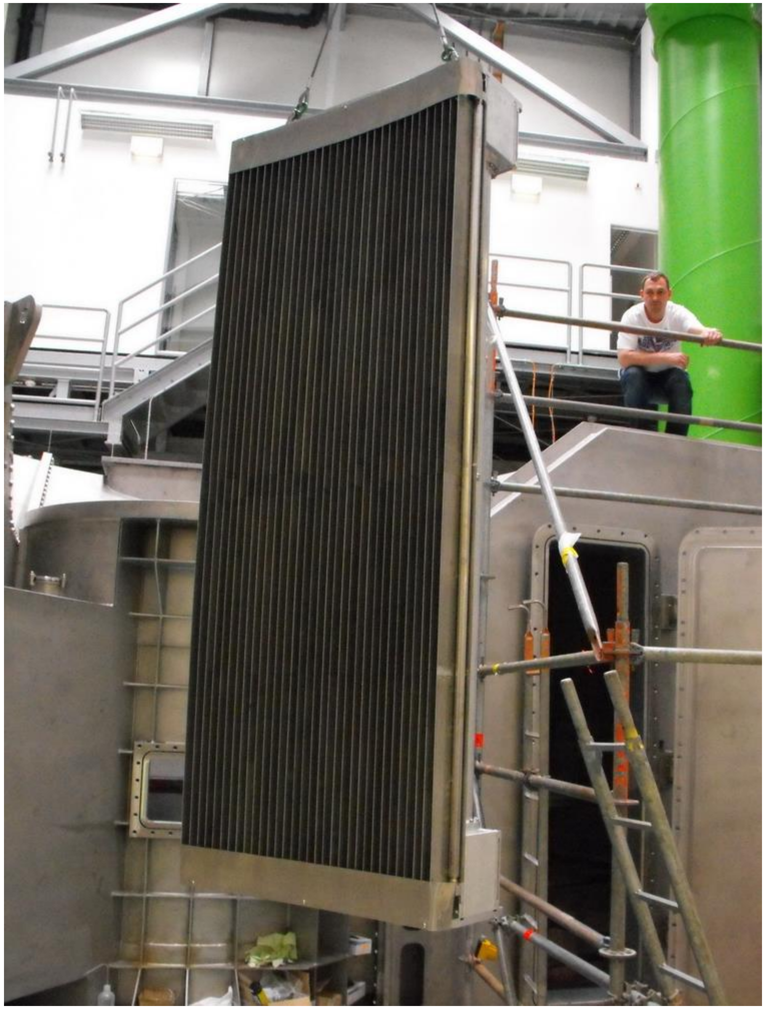
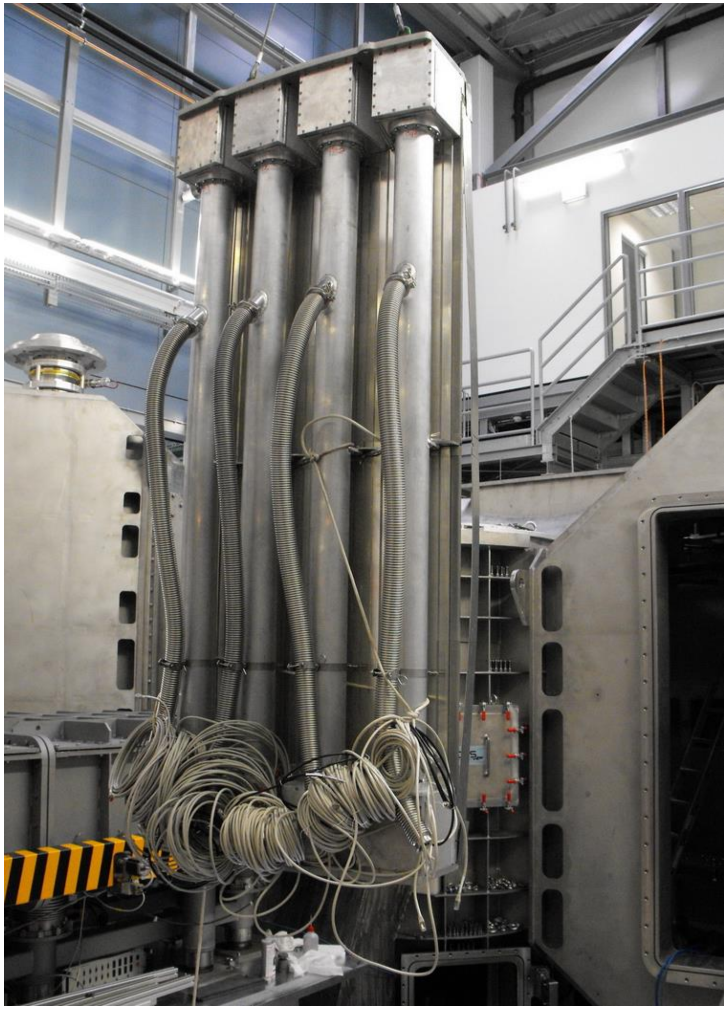
harmat@ante.hu

Manufacturing…





Péter HARMAT
harmat@ante.hu

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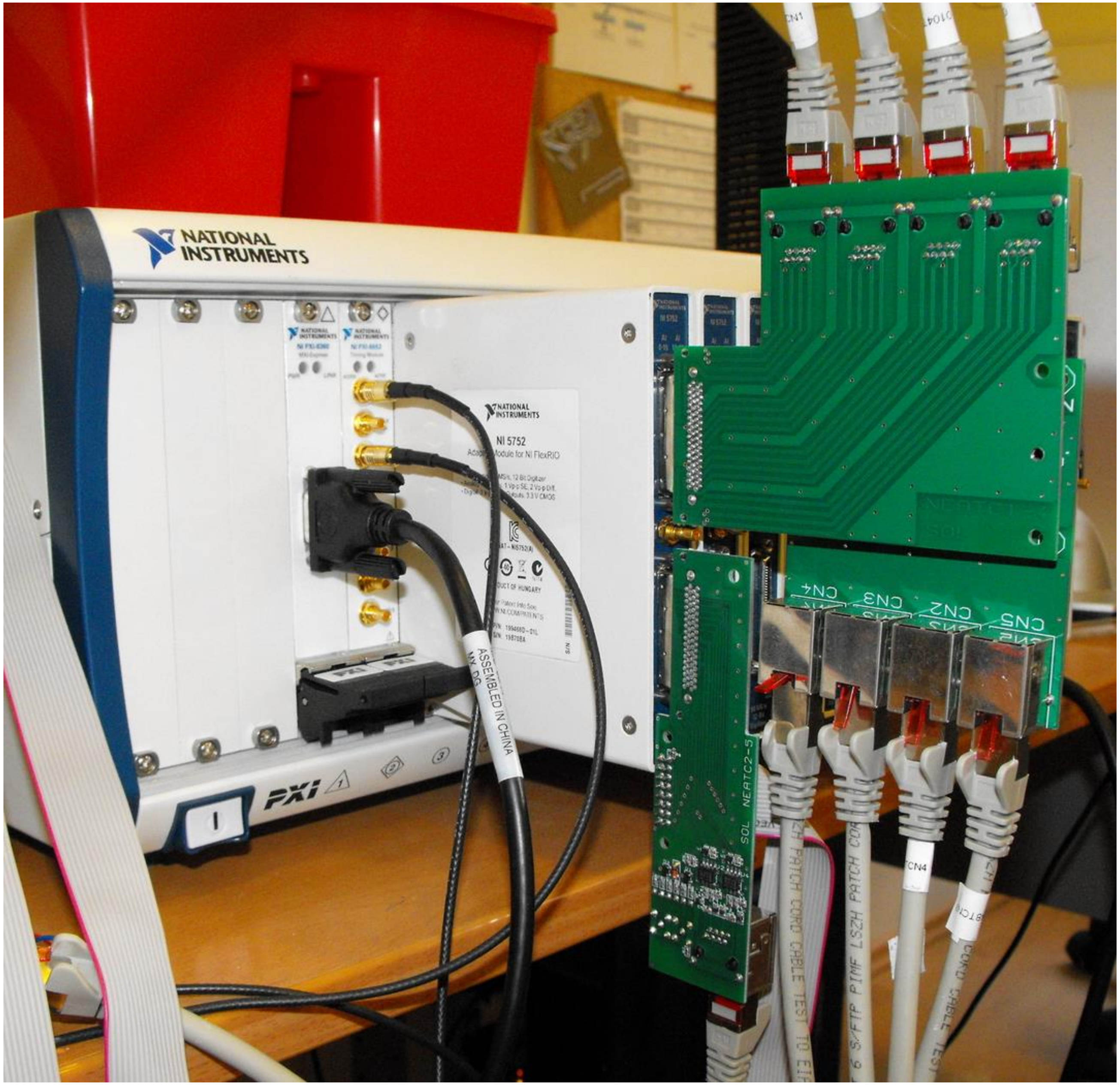
harmat@ante.hu



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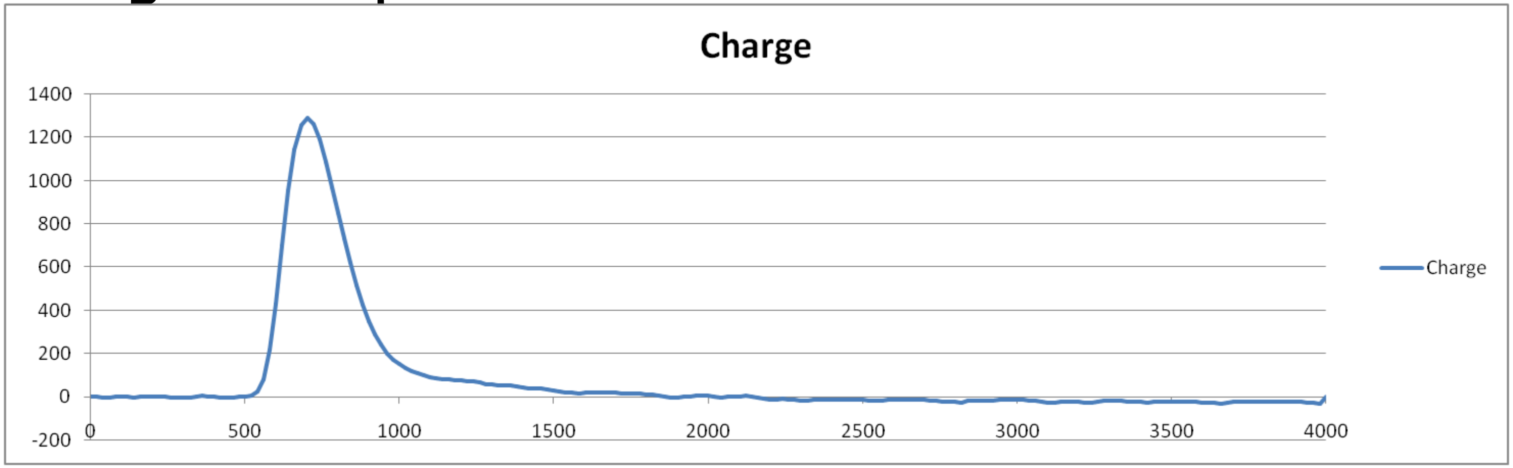
Neutron detection with ^{3}He tube
Typical signal shapes for sampling ADC

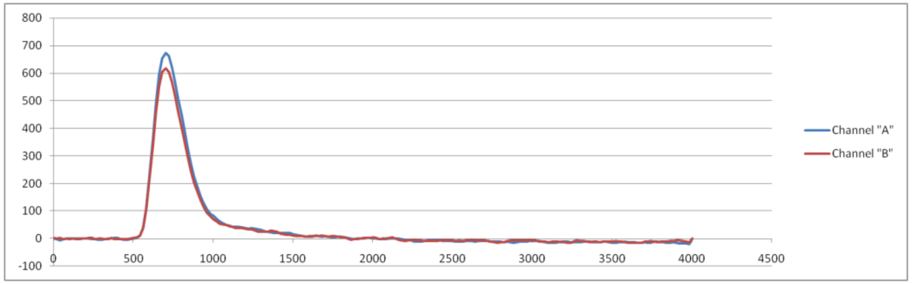
- "Single bump"
  - 1H-3H axis parallel to tube
- "Double bump"
  - 1H-3H axis perpendicular to tube
- "Gamma"
  - non-neutron signal – pulse shape discrimination (PSD)
- "Pileup"
  - more than one neutron during T_{DAQ}

Péter HARMAT
harmat@ante.hu

Signal shapes

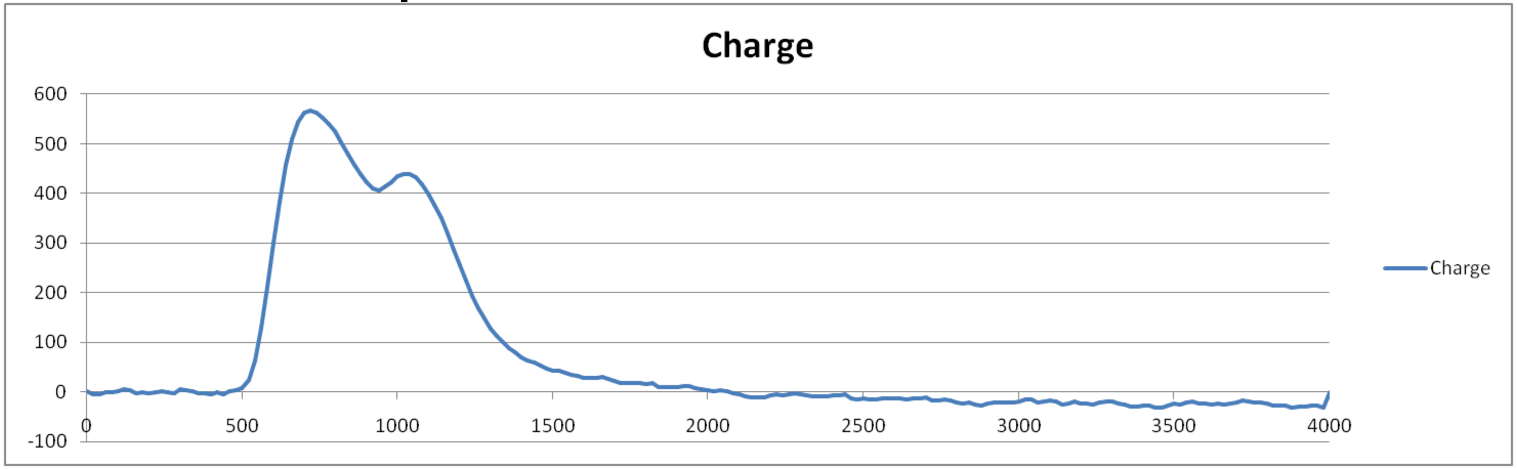
- "Single bump"

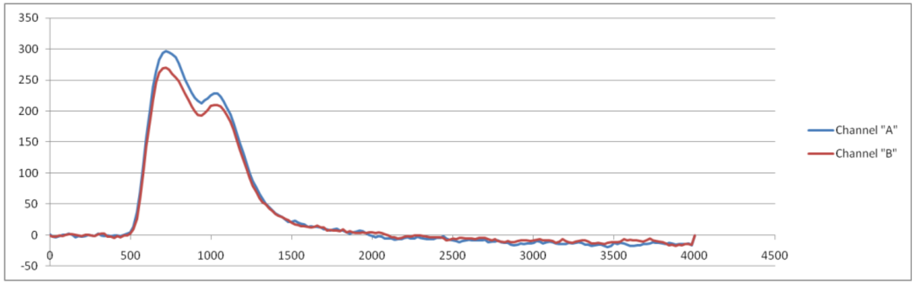




Signal shapes

- "Double bump"

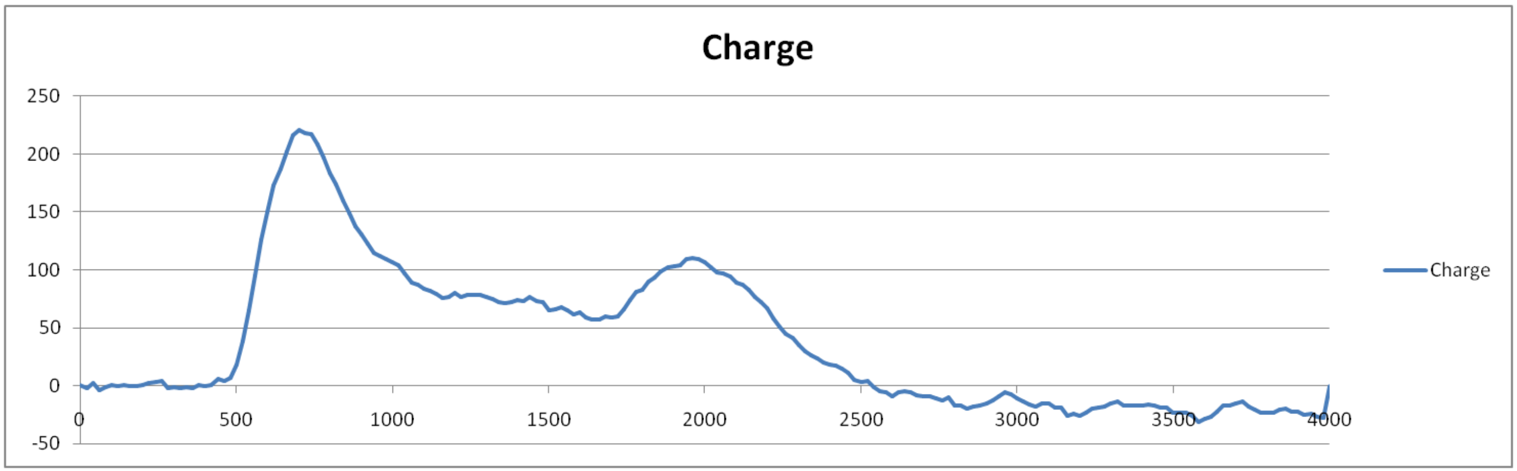


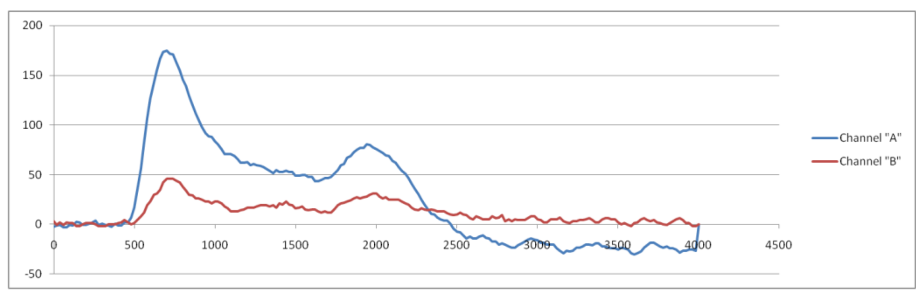


Péter HARMAT
harmat@ante.hu

Signal shapes

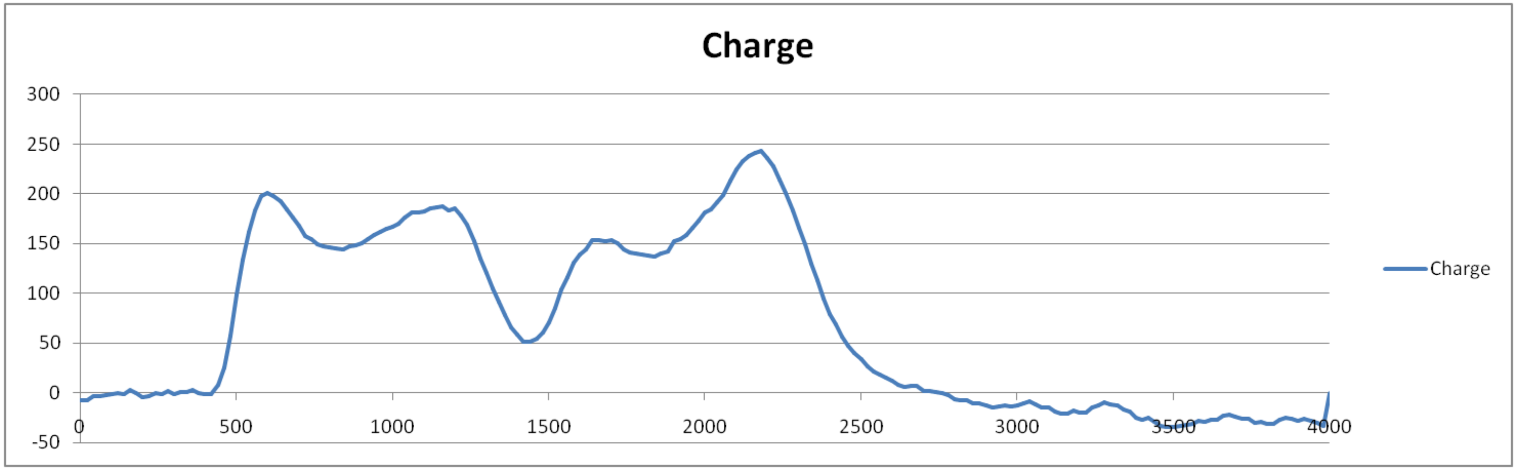
- "Gamma"

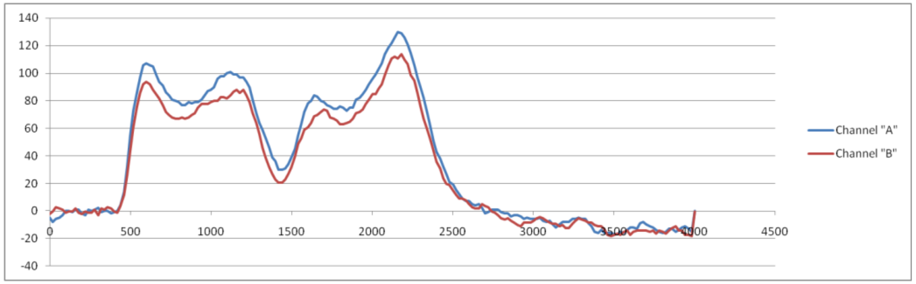




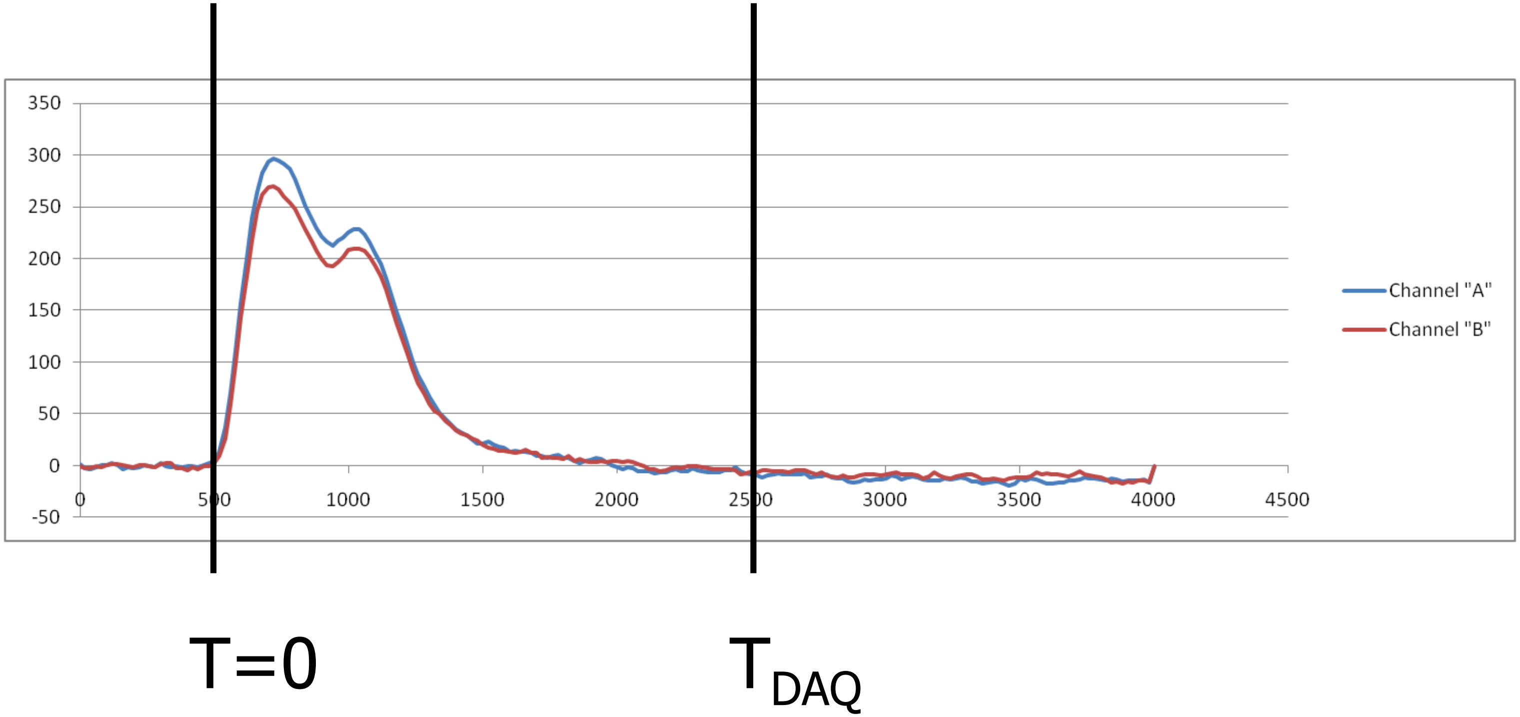
Signal shapes

- "Pileup"

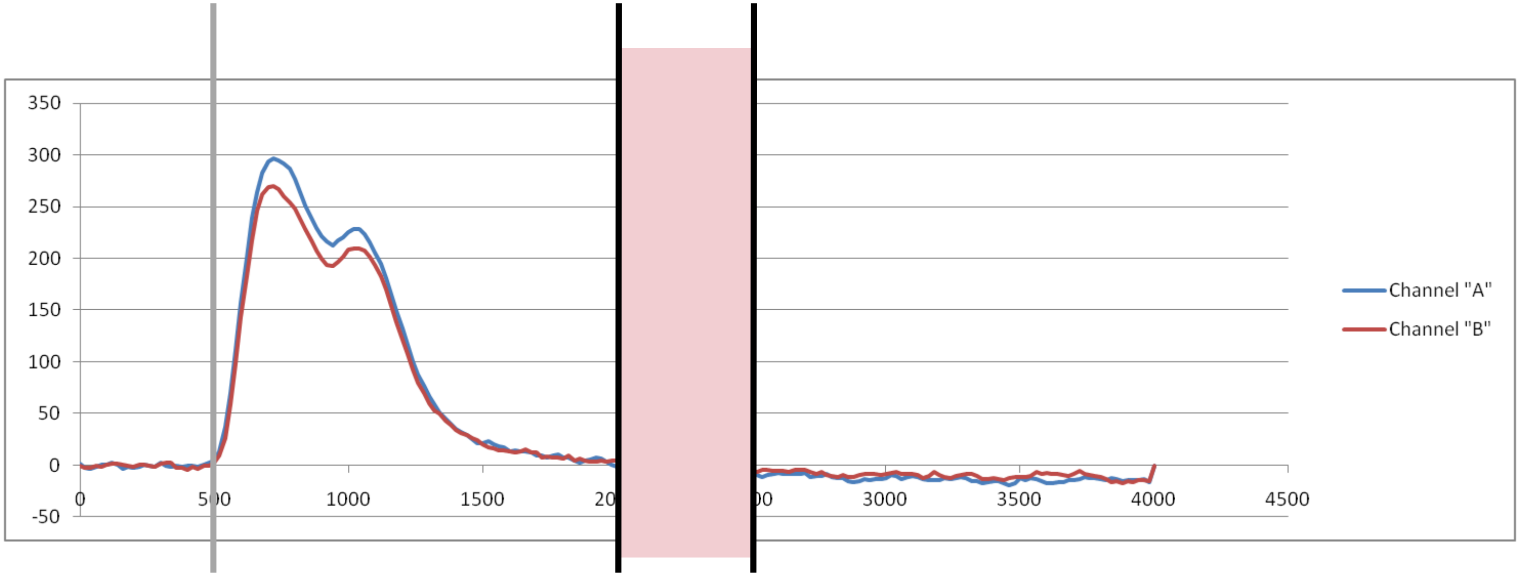




Signal processing

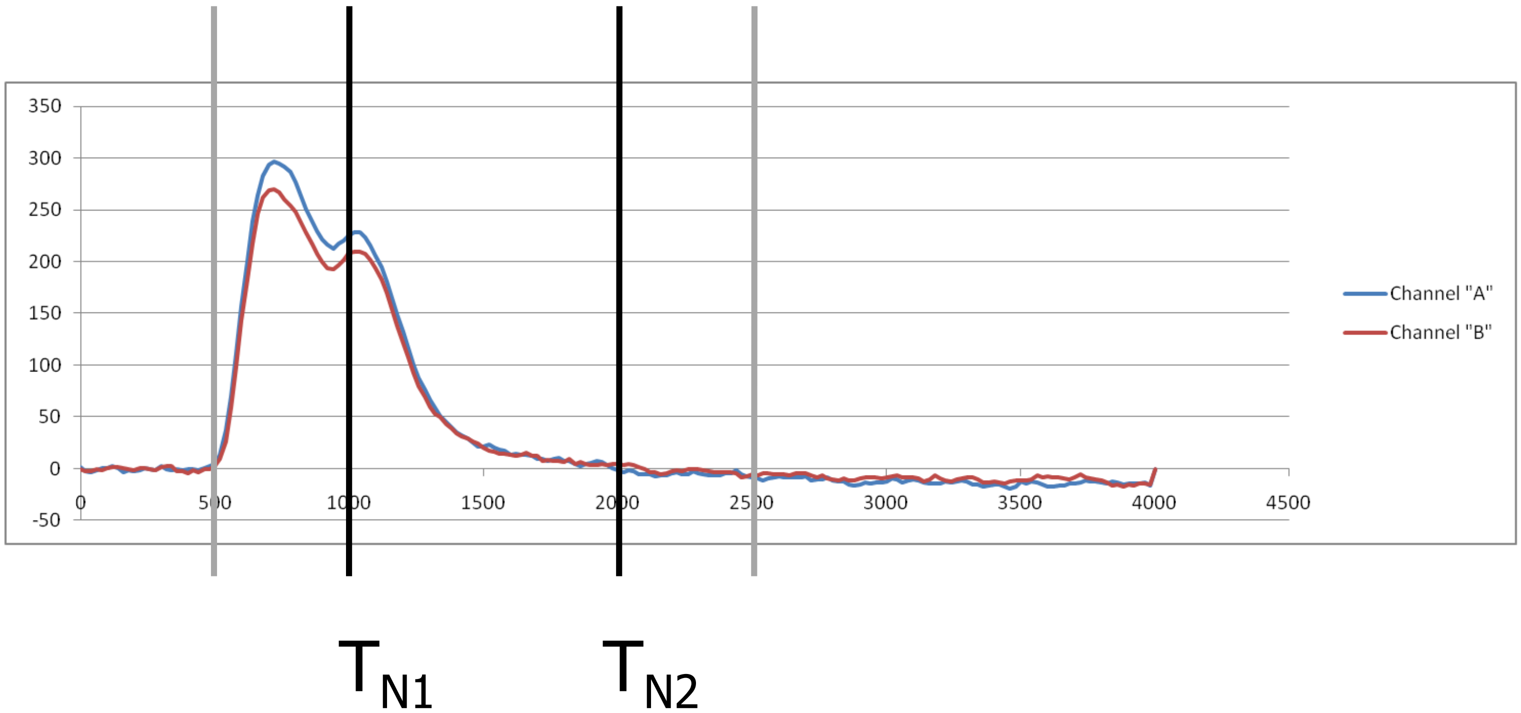


Signal processing



Reserved for baseline restore

Signal processing



Signal processing

- Position: (A-B)/(A+B)
  - From N1: better Signal to Noise Ratio
  - From N1+N2: full information

- Phase Shape Discrimination
  - Charge in N1 vs Charge in N2
  - PSHDISC = Ch_{N2} / Ch_{N1+N2}

Péter HARMAT
harmat@ante.hu

Signal processing – minimizing the background

- Position: (A-B)/(A+B)
  - From N1: better SNR
  - From N1+N2: full information
- Phase Shape Discrimination
  - Charge in N1 vs Charge in N2
  - PSHDISC = Ch_{N2} / Ch_{N1+N2}
- How to spot pileup
  - From PSD?
  - Other shape parameters?

Péter HARMAT
harmat@ante.hu

Conclusion

ANTE realized the following advantages by choosing NI solution both in the hardware and software:

- Construction efforts (hardware, firmware, software) have been minimized during the development
- Enough development capacity remained for concentrating to the substantial neutron detection specific problems like
  - Position calculation algorithms
  - Shape discrimination
  - Signal classification

for minimizing the background

Péter HARMAT
harmat@ante.hu

Thanks for the attention

Contact info

ANTE Kft.
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Konkoly Thege 29-33, H-1121 Budapest
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Péter HARMAT PhD
General Manager
Email: harmat@ante.hu
www.ante.hu